AMD Xilinx - XC3S500E-4PQG208C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1164
Number of Logic Elements/Cells	10476
Total RAM Bits	368640
Number of I/O	158
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s500e-4pqg208c

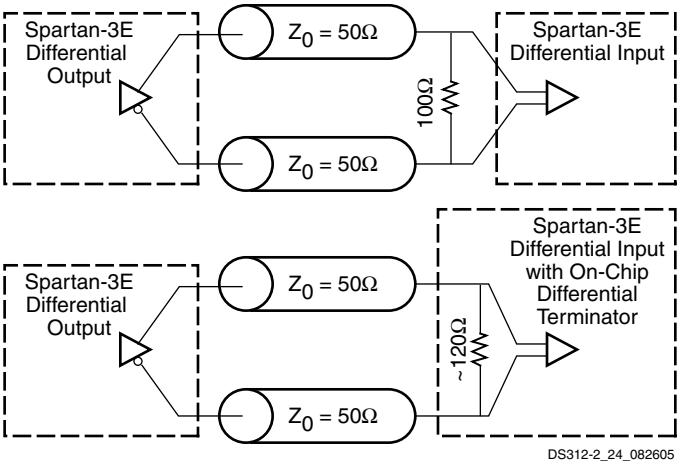

Figure 11: **Differential Inputs and Outputs**

Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors inside each IOB optionally force a floating I/O or Input-only pin to a determined state. Pull-up and pull-down resistors are commonly applied to unused I/Os, inputs, and three-state outputs, but can be used on any I/O or Input-only pin. The pull-up resistor connects an IOB to V_{CCO} through a resistor. The resistance value depends on the V_{CCO} voltage (see Module 3, DC and Switching Characteristics for the specifications). The pull-down resistor similarly connects an IOB to ground with a resistor. The PULLUP and PULLDOWN attributes and library primitives turn on these optional resistors.

By default, PULLDOWN resistors terminate all unused I/O and Input-only pins. Unused I/O and Input-only pins can alternatively be set to PULLUP or FLOAT. To change the unused I/O Pad setting, set the Bitstream Generator (BitGen) option ***UnusedPin*** to PULLUP, PULLDOWN, or FLOAT. The ***UnusedPin*** option is accessed through the Properties for Generate Programming File in ISE. See Bitstream Generator (BitGen) Options.

During configuration a Low logic level on the HSWAP pin activates pull-up resistors on all I/O and Input-only pins not actively used in the selected configuration mode.

Keeper Circuit

Each I/O has an optional keeper circuit (see Figure 12) that keeps bus lines from floating when not being actively driven. The KEEPER circuit retains the last logic level on a line after all drivers have been turned off. Apply the KEEPER attribute or use the KEEPER library primitive to use the KEEPER circuitry. Pull-up and pull-down resistors override the KEEPER settings.

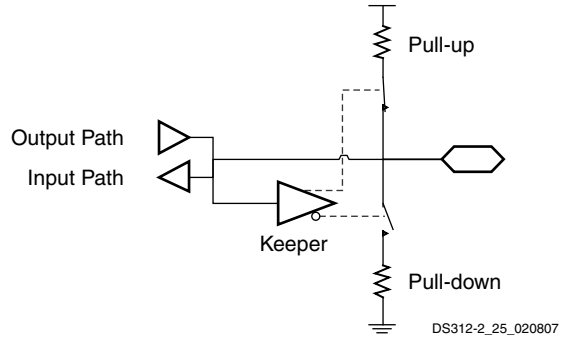

Figure 12: **Keeper Circuit**

Slew Rate Control and Drive Strength

Each IOB has a slew-rate control that sets the output switching edge-rate for LVCMOS and LVTTL outputs. The SLEW attribute controls the slew rate and can either be set to SLOW (default) or FAST.

Each LVCMOS and LVTTL output additionally supports up to six different drive current strengths as shown in Table 8. To adjust the drive strength for each output, the DRIVE attribute is set to the desired drive strength: 2, 4, 6, 8, 12, and 16. Unless otherwise specified in the FPGA application, the software default IOSTANDARD is LVCMOS25, SLOW slew rate, and 12 mA output drive.

Table 8: **Programmable Output Drive Current**

IOSTANDARD	Output Drive Current (mA)					
	2	4	6	8	12	16
LVTTL	✔	✔	✔	✔	✔	✔
LVCMOS33	✔	✔	✔	✔	✔	✔
LVCMOS25	✔	✔	✔	✔	✔	-
LVCMOS18	✔	✔	✔	✔	-	-
LVCMOS15	✔	✔	✔	-	-	-
LVCMOS12	✔	-	-	-	-	-

High output current drive strength and FAST output slew rates generally result in fastest I/O performance. However, these same settings generally also result in transmission line effects on the printed circuit board (PCB) for all but the shortest board traces. Each IOB has independent slew rate and drive strength controls. Use the slowest slew rate and lowest output drive current that meets the performance requirements for the end application.

Likewise, due to lead inductance, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Only use fast, high-drive outputs when required by the application.

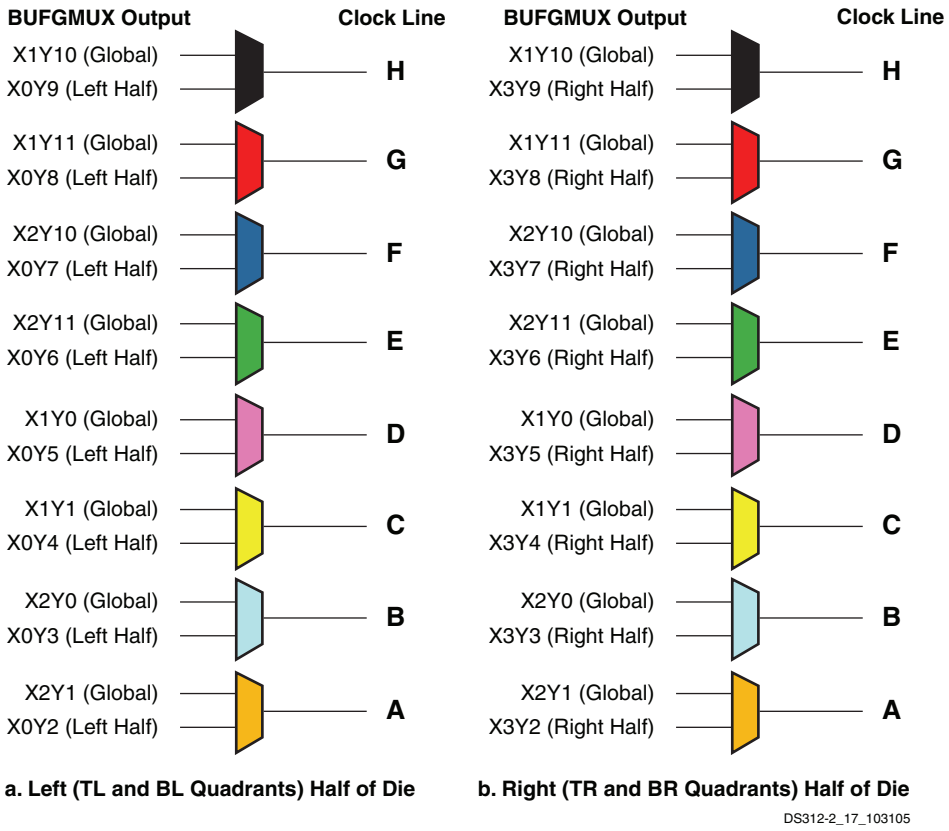

Figure 47: **Clock Sources for the Eight Clock Lines within a Clock Quadrant**

The outputs of the top or bottom BUFGMUX elements connect to two vertical spines, each comprising four vertical clock lines as shown in Figure 45. At the center of the die, these clock signals connect to the eight-line horizontal clock spine.

Outputs of the left and right BUFGMUX elements are routed onto the left or right horizontal spines, each comprising eight horizontal clock lines.

Each of the eight clock signals in a clock quadrant derives either from a global clock signal or a half clock signal. In other words, there are up to 24 total potential clock inputs to the FPGA, eight of which can connect to clocked elements in a single clock quadrant. Figure 47 shows how the clock lines in each quadrant are selected from associated BUFGMUX sources. For example, if quadrant clock ‘A’ in the bottom left (BL) quadrant originates from BUFGMUX_X2Y1, then the clock signal from BUFGMUX_X0Y2 is unavailable in the bottom left quadrant. However, the top left (TL) quadrant clock ‘A’ can still solely use the output from either BUFGMUX_X2Y1 or BUFGMUX_X0Y2 as the source.

To minimize the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock segments not in use.

Direct Connections

Direct connect lines route signals to neighboring tiles: vertically, horizontally, and diagonally. These lines most often drive a signal from a “source” tile to a double, hex, or long line and conversely from the longer interconnect back to a direct line accessing a “destination” tile.

Global Controls (STARTUP_SPARTAN3E)

In addition to the general-purpose interconnect, Spartan-3E FPGAs have two global logic control signals, as described in Table 43. These signals are available to the FPGA application via the STARTUP_SPARTAN3E primitive.

Table 43: **Spartan-3E Global Logic Control Signals**

Global Control Input	Description
GSR	**Global Set/Reset:** When High, asynchronously places all registers and flip-flops in their initial state (see Initialization, page 31). Asserted automatically during the FPGA configuration process (see Start-Up, page 105).
GTS	**Global Three-State:** When High, asynchronously forces all I/O pins to a high-impedance state (Hi-Z, three-state).

The Global Set/Reset (GSR) signal replaces the global reset signal included in many ASIC-style designs. Use the GSR control instead of a separate global reset signal in the design to free up CLB inputs, resulting in a smaller, more efficient design. Similarly, the GSR signal is asserted automatically during the FPGA configuration process, guaranteeing that the FPGA starts-up in a known state.

The STARTUP_SPARTAN3E primitive also includes two other signals used specifically during configuration. The MBT signals are for Dynamically Loading Multiple Configuration Images Using MultiBoot Option, page 91. The CLK input is an alternate clock for configuration Start-Up, page 105.

Voltage Compatibility

The PROM's V_{CCINT} supply must be either 3.3V for the serial XCFxxS Platform Flash PROMs or 1.8V for the serial/parallel XCFxxP PROMs.

Ⓥ The FPGA's VCCO_2 supply input and the Platform Flash PROM's V_{CCO} supply input must be the same voltage, ideally +2.5V. Both devices also support 1.8V and 3.3V interfaces but the FPGA's PROG_B and DONE pins require special attention as they are powered by the FPGA's V_{CCAUX} supply, nominally 2.5V. See application note XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Supported Platform Flash PROMs

Table 51 shows the smallest available Platform Flash PROM to program one Spartan-3E FPGA. A multiple-FPGA daisy-chain application requires a Platform Flash PROM large enough to contain the sum of the various FPGA file sizes.

Table 51: **Number of Bits to Program a Spartan-3E FPGA and Smallest Platform Flash PROM**

Spartan-3E FPGA	Number of Configuration Bits	Smallest Available Platform Flash
XC3S100E	581,344	XCF01S
XC3S250E	1,353,728	XCF02S
XC3S500E	2,270,208	XCF04S
XC3S1200E	3,841,184	XCF04S
XC3S1600E	5,969,696	XCF08P or 2 x XCF04S

The XC3S1600E requires an 8 Mbit PROM. Two solutions are possible: either a single 8 Mbit XCF08P parallel/serial PROM or two 4 Mbit XCF04S serial PROMs cascaded. The two XCF04S PROMs use a 3.3V V_{CCINT} supply while the XCF08P requires a 1.8V V_{CCINT} supply. If the board does not already have a 1.8V supply available, the two cascaded XCF04S PROM solution is recommended.

CCLK Frequency

In Master Serial mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's CLK input pin. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option. Table 52 shows the maximum ***ConfigRate*** settings, approximately equal to MHz, for various Platform Flash devices and I/O voltages. For the serial XCFxxS PROMs, the maximum frequency also depends on the interface voltage.

Table 52: **Maximum ConfigRate Settings for Platform Flash**

Platform Flash Part Number	I/O Voltage (VCCO_2, V_{CCO})	Maximum *ConfigRate* Setting
XCF01S XCF02S XCF04S	3.3V or 2.5V	25
	1.8V	12
XCF08P XCF16P XCF32P	3.3V, 2.5V, or 1.8V	25

SPI Serial Flash Mode

For additional information, refer to the “Master SPI Mode” chapter in UG332.

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 53 and Figure 54. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

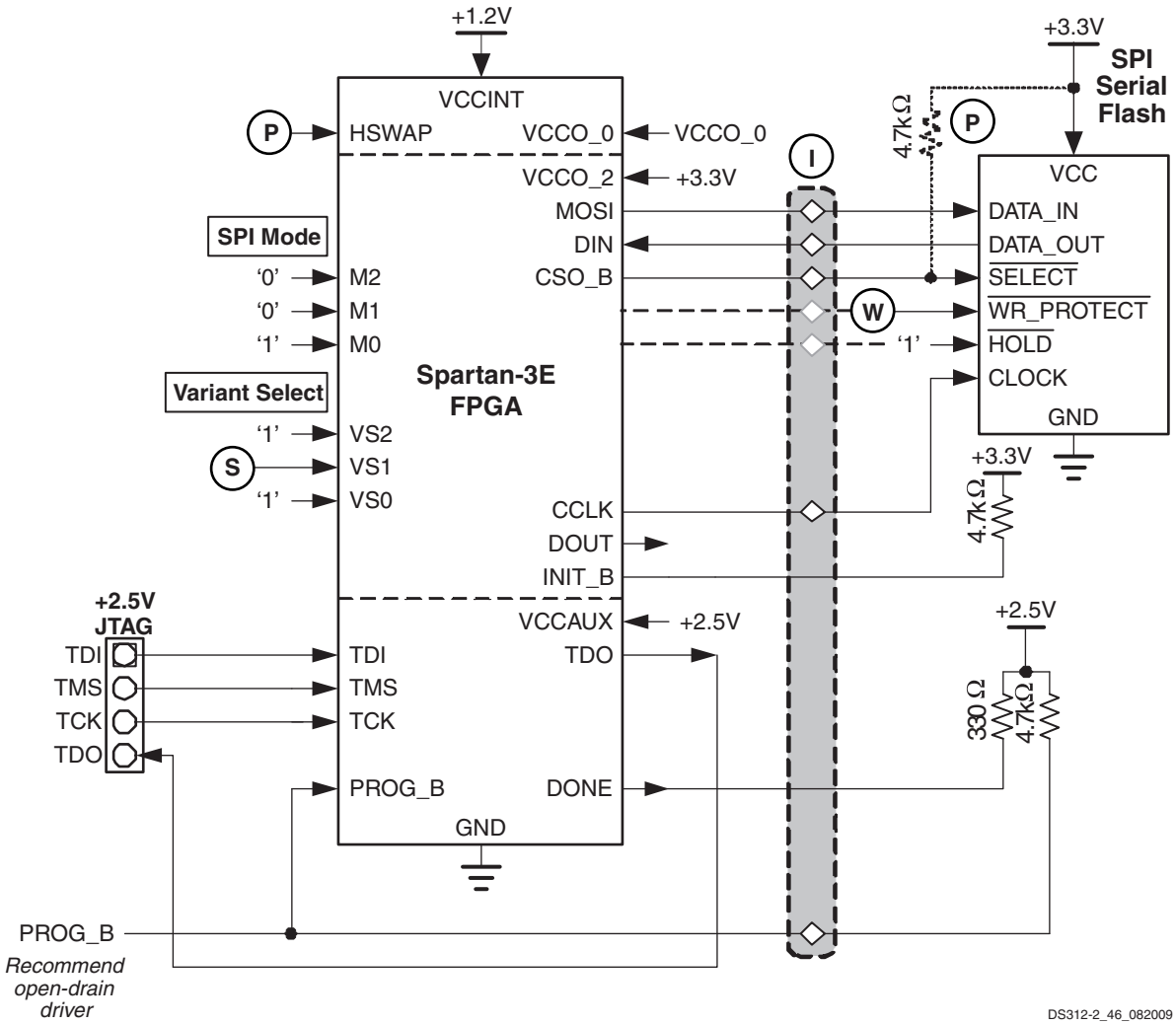

Figure 53: **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

S Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA’s variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 53 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in Serial Peripheral Interface (SPI) Configuration Timing in Module 3.

Figure 53 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 54 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. ‘B’-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use ‘C’- or ‘D’-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

(W) Table 54 shows the connections between the SPI Flash PROM and the FPGA's SPI configuration interface. Each SPI Flash PROM vendor uses slightly different signal naming. The SPI Flash PROM's write protect and hold controls are not used by the FPGA during configuration. However, the $\overline{\text{HOLD}}$ pin must be High during the configuration process. The PROM's write protect input must be High in order to write or program the Flash memory.

Table 54: **Example SPI Flash PROM Connections and Pin Naming**

SPI Flash Pin	FPGA Connection	STMicro	NexFlash	Silicon Storage Technology	Atmel DataFlash
DATA_IN	MOSI	D	DI	SI	SI
DATA_OUT	DIN	Q	DO	SO	SO
$\overline{\text{SELECT}}$	CSO_B	$\overline{\text{S}}$	$\overline{\text{CS}}$	CE#	$\overline{\text{CS}}$
CLOCK	CCLK	C	CLK	SCK	SCK
$\overline{\text{WR\_PROTECT}}$ (W)	Not required for FPGA configuration. Must be High to program SPI Flash. Optional connection to FPGA user I/O after configuration.	$\overline{\text{W}}$	$\overline{\text{WP}}$	WP#	$\overline{\text{WP}}$
$\overline{\text{HOLD}}$ (see Figure 53)	Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Not applicable to Atmel DataFlash.	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$	HOLD#	N/A
$\overline{\text{RESET}}$ (see Figure 54)	Only applicable to Atmel DataFlash. Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Do not connect to FPGA's PROG_B as this will prevent direct programming of the DataFlash.	N/A	N/A	N/A	$\overline{\text{RESET}}$
RDY/$\overline{\text{BUSY}}$ (see Figure 54)	Only applicable to Atmel DataFlash and only available on certain packages. Not required for FPGA configuration. Output from DataFlash PROM. Optional connection to FPGA user I/O after configuration.	N/A	N/A	N/A	RDY/$\overline{\text{BUSY}}$

The mode select pins, M[2:0], and the variant select pins, VS[2:0] are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, these pins are all available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 55: **Serial Peripheral Interface (SPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 1. Sampled when INIT_B goes High.	User I/O

can also be eliminated from the interface. However, RDWR_B must remain Low during configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Alternatively, the bidirectional SelectMAP configuration interface is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. The external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

The Slave Parallel mode is also used with BPI mode to create multi-FPGA daisy-chains. The lead FPGA is set for BPI mode configuration; all the downstream daisy-chain FPGAs are set for Slave Parallel configuration, as highlighted in Figure 59.

Table 65: **Slave Parallel Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 1, M1 = 1, M0 = 0 Sampled when INIT_B goes High.	User I/O
D[7:0]	Input	**Data Input**.	Byte-wide data provided by host. FPGA captures data on rising CCLK edge.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
BUSY	Output	**Busy Indicator**.	If CCLK frequency is < 50 MHz, this pin may be ignored. When High, indicates that the FPGA is not ready to receive additional configuration data. Host must hold data an additional clock cycle.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSI_B	Input	**Chip Select Input**. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	**Read/Write Control**. Active Low write enable.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CCLK	Input	**Configuration Clock**. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	External clock.	User I/O If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSO_B	Output	**Chip Select Output**. Active Low.	Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. Actively drives.	User I/O

Power Supply Specifications

Table 74: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 75: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 76: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

General Recommended Operating Conditions

Table 77: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.140	1.200	1.260	V
V_{CCO} (1)	Output driver supply voltage			1.100	-	3.465	V
V_{CCAUX}	Auxiliary supply voltage			2.375	2.500	2.625	V
V_{IN} (2,3)	Input voltage extremes to avoid turning on I/O protection diodes	I/O, Input-only, and Dual-Purpose pins (4)	IP or IO_#	–0.5	–	V_{CCO} + 0.5	V
			IO_Lxxy_# (5)	–0.5	–	V_{CCO} + 0.5	V
		Dedicated pins (6)		–0.5	–	V_{CCAUX} + 0.5	V
T_{IN}	Input signal transition time (7)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 80 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 82 lists that specific to the differential standards.
2. Input voltages outside the recommended range require the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Refer to Table 73.
3. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 73.
5. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
6. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
7. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Table 81: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
PCI33_3(4)		1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(4)		1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
SSTL18_I		6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475

Table 81: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61

Notes:

1. The numbers in this table are based on the conditions set forth in Table 77 and Table 80.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} – the output current condition under which VOL is tested
   I_{OH} – the output current condition under which VOH is tested
   V_{OL} – the output voltage that indicates a Low logic level
   V_{OH} – the output voltage that indicates a High logic level
   V_{CCO} – the supply voltage for output drivers
   V_{TT} – the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
4. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Table 90: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Propagation Times							
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	1.96	2.25	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	5.40	5.97	ns
			3	All Others	6.30	7.20	

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 91.

Table 91: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.42	0.43	ns
LVCMOS33	0.42	0.43	ns
LVCMOS25	0	0	ns
LVCMOS18	0.96	0.98	ns
LVCMOS15	0.62	0.63	ns
LVCMOS12	0.26	0.27	ns
PCI33_3	0.41	0.42	ns
PCI66_3	0.41	0.42	ns
HSTL_I_18	0.12	0.12	ns
HSTL_III_18	0.17	0.17	ns
SSTL18_I	0.30	0.30	ns
SSTL2_I	0.15	0.15	ns

Table 91: **Input Timing Adjustments by IOSTANDARD *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.48	0.49	ns
BLVDS_25	0.39	0.39	ns
MINI_LVDS_25	0.48	0.49	ns
LVPECL_25	0.27	0.27	ns
RSDS_25	0.48	0.49	ns
DIFF_HSTL_I_18	0.48	0.49	ns
DIFF_HSTL_III_18	0.48	0.49	ns
DIFF_SSTL18_I	0.30	0.30	ns
DIFF_SSTL2_I	0.32	0.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77, Table 80, and Table 82.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
Single-Ended Standards							
LVTTL	Slow	2	34	20	19	52	60
		4	17	10	10	26	41
		6	17	10	7	26	29
		8	8	6	6	13	22
		12	8	6	5	13	13
		16	5	5	5	6	11
	Fast	2	17	17	17	26	34
		4	9	9	9	13	20
		6	7	7	7	13	15
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	5	5	5	5	9
LVCMOS33	Slow	2	34	20	20	52	76
		4	17	10	10	26	46
		6	17	10	7	26	27
		8	8	6	6	13	20
		12	8	6	5	13	13
		16	5	5	5	6	10
	Fast	2	17	17	17	26	44
		4	8	8	8	13	26
		6	8	6	6	13	16
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	8	8	5	5	8
LVCMOS25	Slow	2	28	16	16	42	76
		4	13	10	10	19	46
		6	13	7	7	19	33
		8	6	6	6	9	24
		12	6	6	6	9	18
	Fast	2	17	16	16	26	42
		4	9	9	9	13	20
		6	9	7	7	13	15
		8	6	6	6	6	13
		12	5	5	5	6	11
LVCMOS18	Slow	2	19	11	8	29	64
		4	13	7	6	19	34
		6	6	5	5	9	22
		8	6	4	4	9	18
	Fast	2	13	8	8	19	36
		4	8	5	5	13	21
		6	4	4	4	6	13
		8	4	4	4	6	10

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
LVCMOS15	Slow	2	16	10	10	19	55
		4	8	7	7	9	31
		6	6	5	5	9	18
	Fast	2	9	9	9	13	25
		4	7	7	7	7	16
		6	5	5	5	5	13
LVCMOS12	Slow	2	17	11	11	16	55
	Fast	2	10	10	10	10	31
PCI33_3			8	8	8	16	16
PCI66_3			8	8	8	13	13
PCIX			7	7	7	11	11
HSTL_I_18			10	10	10	16	17
HSTL_III_18			10	10	10	16	16
SSTL18_I			9	9	9	15	15
SSTL2_I			12	12	12	18	18
Differential Standards (Number of I/O Pairs or Channels)							
LVDS_25			6	6	6	12	20
BLVDS_25			4	4	4	4	4
MINI_LVDS_25			6	6	6	12	20
LVPECL_25			Input Only				
RSDS_25			6	6	6	12	20
DIFF_HSTL_I_18			5	5	5	8	8
DIFF_HSTL_IIII_18			5	5	5	8	8
DIFF_SSTL18_I			4	4	4	7	7
DIFF_SSTL2_I			6	6	6	9	8

Notes:

1. The numbers in this table are recommendations that assume sound board layout practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per VCCO and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the VIL/VIH voltage limits for the respective I/O standard.
2. The PQ208 results are based on physical measurements of a PQ208 package soldered to a typical printed circuit board. All other results are based on worst-case simulation and an interpolation of the PQ208 physical results.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: Managing Ground Bounce in Large FPGAs for information on how to perform weighted average SSO calculations.

Serial Peripheral Interface (SPI) Configuration Timing

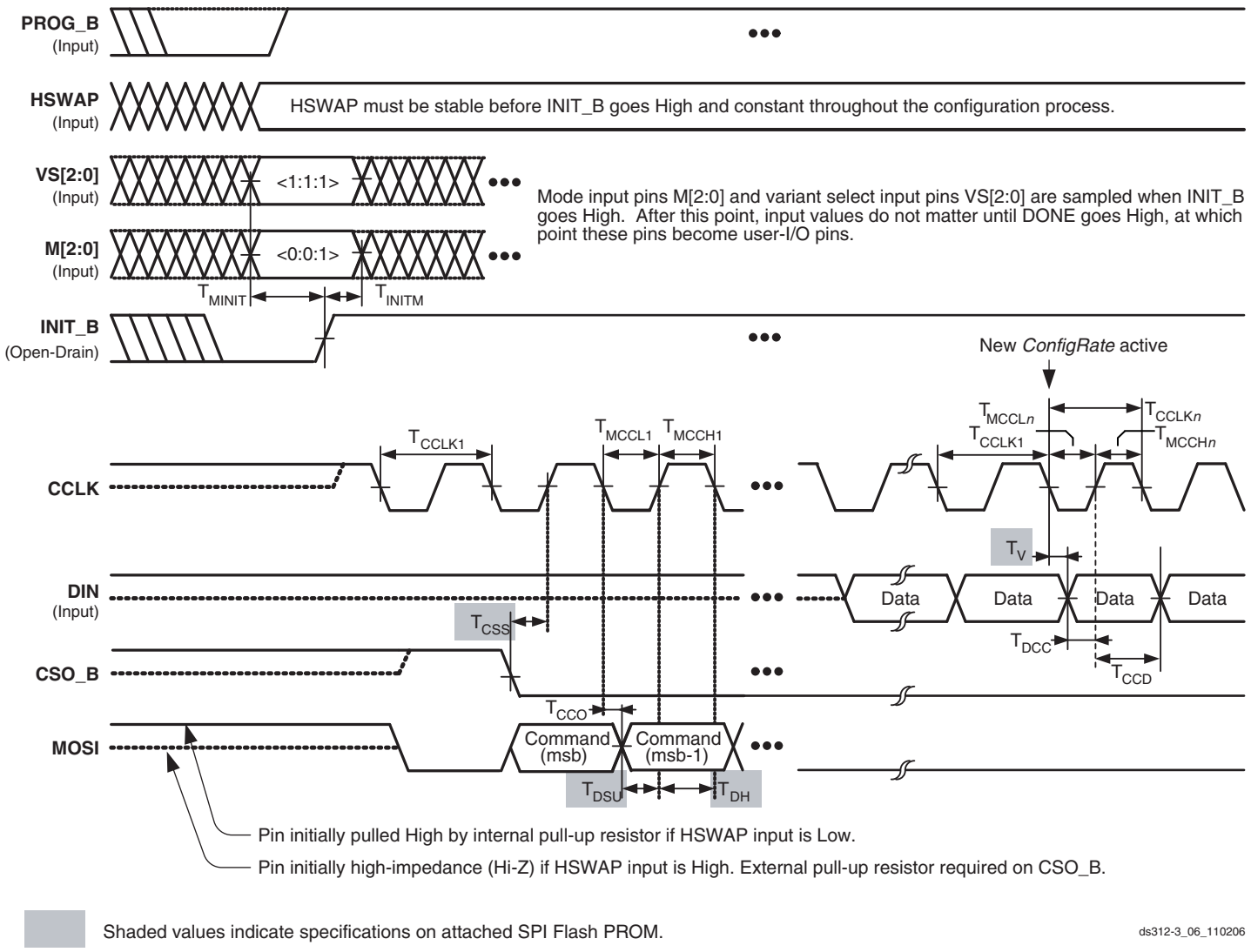

Figure 76: **Waveforms for Serial Peripheral Interface (SPI) Configuration**

Table 118: **Timing for Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 112		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 112		
T_{MINIT}	Setup time on VS[2:0] and M[2:0] mode pins before the rising edge of INIT_B	50	-	ns
T_{INITM}	Hold time on VS[2:0] and M[2:0]mode pins after the rising edge of INIT_B	0	-	ns
T_{CCO}	MOSI output valid after CCLK edge	See Table 116		
T_{DCC}	Setup time on DIN data input before CCLK edge	See Table 116		
T_{CCD}	Hold time on DIN data input after CCLK edge	See Table 116		

Date	Version	Revision
08/26/09	3.8	Added reference to XAPP459 in Table 73 note 2. Updated BPI timing in Figure 77, Table 119, and Table 120. Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 95. Added Spread Spectrum paragraph. Revised hold times for $T_{IOICKPD}$ in Table 88 and setup times for T_{DICK} in Table 98. Added note 4 to Table 106 and note 3 to Table 107, and updated note 6 for Table 107 to add input jitter.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Revised note 2 in Table 73. Revised note 2 and V_{IN} description in Table 77, and added note 5. Added note 3 to Table 78.

Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN (“PRODUCTS”) ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED IN THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

CRITICAL APPLICATIONS DISCLAIMER

XILINX PRODUCTS (INCLUDING HARDWARE, SOFTWARE AND/OR IP CORES) ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS IN LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, CLASS III MEDICAL DEVICES, NUCLEAR FACILITIES, APPLICATIONS RELATED TO THE DEPLOYMENT OF AIRBAGS, OR ANY OTHER APPLICATIONS THAT COULD LEAD TO DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (INDIVIDUALLY AND COLLECTIVELY, “CRITICAL APPLICATIONS”). FURTHERMORE, XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN ANY APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE OR AIRCRAFT, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR. CUSTOMER AGREES, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE XILINX PRODUCTS, TO THOROUGHLY TEST THE SAME FOR SAFETY PURPOSES. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN CRITICAL APPLICATIONS.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.

VQ100: 100-lead Very-thin Quad Flat Package

The XC3S100E, XC3S250E, and the XC3S500E devices are available in the 100-lead very-thin quad flat package, VQ100. All devices share a common footprint for this package as shown in Table 131 and Figure 80.

Table 131 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 package does not support the Byte-wide Peripheral Interface (BPI) configuration mode. Consequently, the VQ100 footprint has fewer DUAL-type pins than other packages.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 131 shows the pinout for production Spartan-3E FPGAs in the VQ100 package.

Table 131: **VQ100 Package Pinout**

Bank	XC3S100E XC3S250E XC3S500E Pin Name	VQ100 Pin Number	Type
0	IO	P92	I/O
0	IO_L01N_0	P79	I/O
0	IO_L01P_0	P78	I/O
0	IO_L02N_0/GCLK5	P84	GCLK
0	IO_L02P_0/GCLK4	P83	GCLK
0	IO_L03N_0/GCLK7	P86	GCLK
0	IO_L03P_0/GCLK6	P85	GCLK
0	IO_L05N_0/GCLK11	P91	GCLK
0	IO_L05P_0/GCLK10	P90	GCLK
0	IO_L06N_0/VREF_0	P95	VREF
0	IO_L06P_0	P94	I/O
0	IO_L07N_0/HSWAP	P99	DUAL
0	IO_L07P_0	P98	I/O
0	IP_L04N_0/GCLK9	P89	GCLK
0	IP_L04P_0/GCLK8	P88	GCLK
0	VCCO_0	P82	VCCO
0	VCCO_0	P97	VCCO
1	IO_L01N_1	P54	I/O
1	IO_L01P_1	P53	I/O
1	IO_L02N_1	P58	I/O
1	IO_L02P_1	P57	I/O
1	IO_L03N_1/RHCLK1	P61	RHCLK
1	IO_L03P_1/RHCLK0	P60	RHCLK
1	IO_L04N_1/RHCLK3	P63	RHCLK
1	IO_L04P_1/RHCLK2	P62	RHCLK
1	IO_L05N_1/RHCLK5	P66	RHCLK
1	IO_L05P_1/RHCLK4	P65	RHCLK
1	IO_L06N_1/RHCLK7	P68	RHCLK
1	IO_L06P_1/RHCLK6	P67	RHCLK
1	IO_L07N_1	P71	I/O
1	IO_L07P_1	P70	I/O
1	IP/VREF_1	P69	VREF
1	VCCO_1	P55	VCCO
1	VCCO_1	P73	VCCO
2	IO/D5	P34	DUAL
2	IO/M1	P42	DUAL
2	IO_L01N_2/INIT_B	P25	DUAL
2	IO_L01P_2/CSO_B	P24	DUAL
2	IO_L02N_2/MOSI/CSI_B	P27	DUAL
2	IO_L02P_2/DOUT/BUSY	P26	DUAL
2	IO_L03N_2/D6/GCLK13	P33	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	P32	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	P36	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	P35	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	P41	DUAL/GCLK
2	IO_L06P_2/D2/GCLK2	P40	DUAL/GCLK
2	IO_L07N_2/DIN/D0	P44	DUAL
2	IO_L07P_2/M0	P43	DUAL
2	IO_L08N_2/VS1	P48	DUAL
2	IO_L08P_2/VS2	P47	DUAL
2	IO_L09N_2/CCLK	P50	DUAL
2	IO_L09P_2/VS0	P49	DUAL
2	IP/VREF_2	P30	VREF
2	IP_L05N_2/M2/GCLK1	P39	DUAL/GCLK
2	IP_L05P_2/RDWR_B/ GCLK0	P38	DUAL/GCLK
2	VCCO_2	P31	VCCO
2	VCCO_2	P45	VCCO
3	IO_L01N_3	P3	I/O
3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	P5	VREF

Table 131: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S100E XC3S250E XC3S500E Pin Name	VQ100 Pin Number	Type
3	IO_L02P_3	P4	I/O
3	IO_L03N_3/LHCLK1	P10	LHCLK
3	IO_L03P_3/LHCLK0	P9	LHCLK
3	IO_L04N_3/LHCLK3	P12	LHCLK
3	IO_L04P_3/LHCLK2	P11	LHCLK
3	IO_L05N_3/LHCLK5	P16	LHCLK
3	IO_L05P_3/LHCLK4	P15	LHCLK
3	IO_L06N_3/LHCLK7	P18	LHCLK
3	IO_L06P_3/LHCLK6	P17	LHCLK
3	IO_L07N_3	P23	I/O
3	IO_L07P_3	P22	I/O
3	IP	P13	INPUT
3	VCCO_3	P8	VCCO
3	VCCO_3	P20	VCCO
GND	GND	P7	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P29	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P59	GND
GND	GND	P64	GND
GND	GND	P72	GND
GND	GND	P81	GND
GND	GND	P87	GND
GND	GND	P93	GND
VCCAUX	DONE	P51	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P77	JTAG
VCCAUX	TDI	P100	JTAG
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P75	JTAG
VCCAUX	VCCAUX	P21	VCCAUX
VCCAUX	VCCAUX	P46	VCCAUX
VCCAUX	VCCAUX	P74	VCCAUX
VCCAUX	VCCAUX	P96	VCCAUX
VCCINT	VCCINT	P6	VCCINT
VCCINT	VCCINT	P28	VCCINT
VCCINT	VCCINT	P56	VCCINT
VCCINT	VCCINT	P80	VCCINT

PQ208 Footprint (Left)

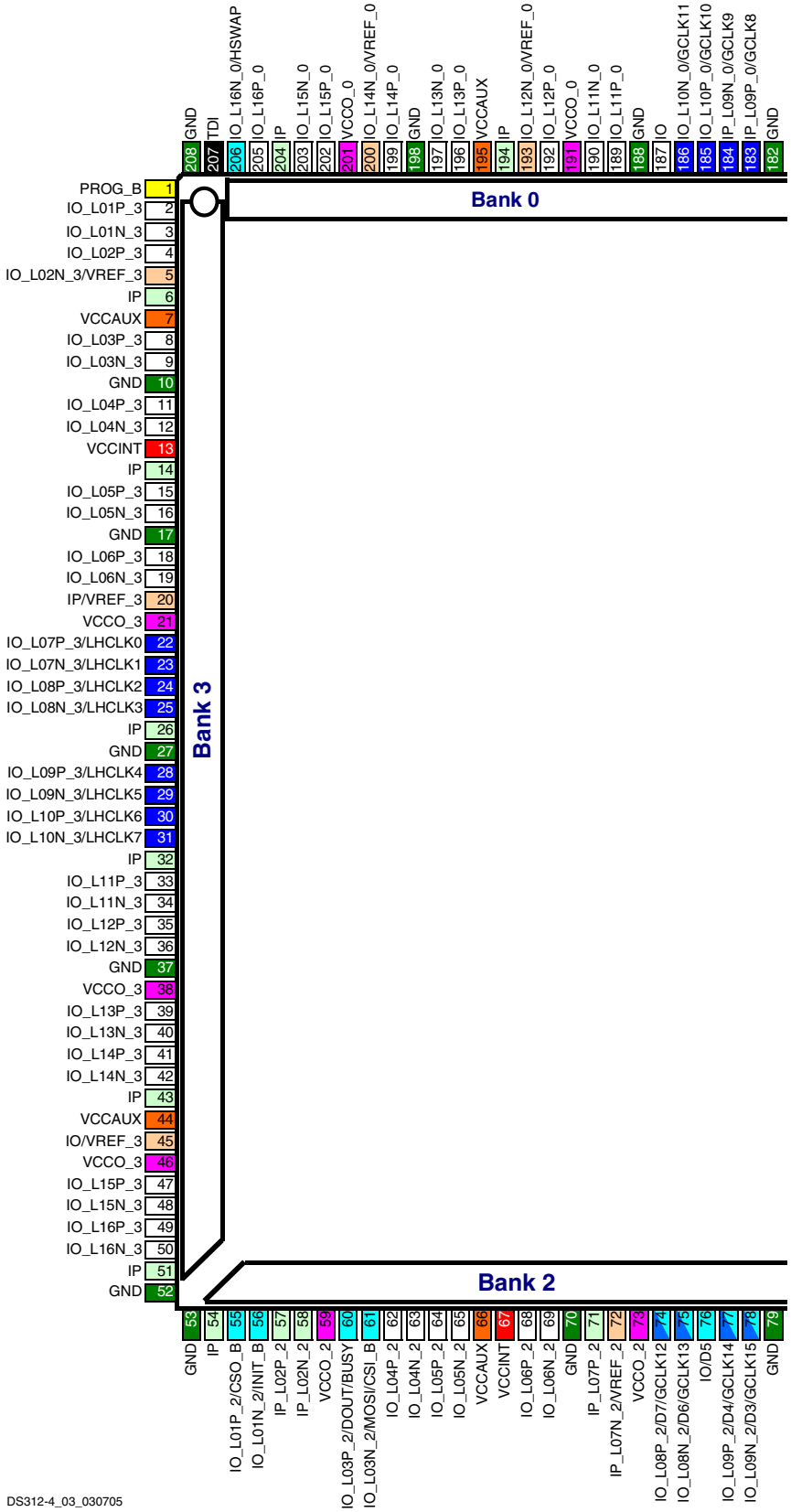

Figure 83: **PQ208 Footprint (Left)**

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	N.C. (◆)	IO_L04N_3	IO_L04N_3	E3	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	E4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	F2	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	F1	I/O
3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	G4	VREF
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G3	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G5	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G6	I/O
3	IO_L08N_3	IO_L08N_3	IO_L08N_3	H5	I/O
3	IO_L08P_3	IO_L08P_3	IO_L08P_3	H6	I/O
3	IO_L09N_3	IO_L09N_3	IO_L09N_3	H3	I/O
3	IO_L09P_3	IO_L09P_3	IO_L09P_3	H4	I/O
3	IO_L10N_3	IO_L10N_3	IO_L10N_3	H1	I/O
3	IO_L10P_3	IO_L10P_3	IO_L10P_3	H2	I/O
3	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	J4	LHCLK
3	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	J5	LHCLK
3	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	J2	LHCLK
3	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	J1	LHCLK
3	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	K4	LHCLK
3	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	K3	LHCLK
3	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	K5	LHCLK
3	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	K6	LHCLK
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L2	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	L1	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	L4	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	L3	I/O
3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	L5	VREF
3	IO_L17P_3	IO_L17P_3	IO_L17P_3	L6	I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	M3	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	M4	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	M6	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	M5	I/O
3	IO_L20N_3	IO_L20N_3	IO_L20N_3	N5	I/O
3	IO_L20P_3	IO_L20P_3	IO_L20P_3	N4	I/O
3	IO_L21N_3	IO_L21N_3	IO_L21N_3	P1	I/O
3	IO_L21P_3	IO_L21P_3	IO_L21P_3	P2	I/O
3	N.C. (◆)	IO_L22N_3	IO_L22N_3	P4	**500E:** N.C. **1200E:** I/O **1600E:** I/O

Footprint Migration Differences

Table 151 summarizes any footprint and functionality differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs that may affect easy migration between devices available in the FG320 package. There are 26 such balls. All other pins not listed in Table 151 unconditionally migrate between Spartan-3E devices available in the FG320 package.

The XC3S500E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S1200E and the XC3S1600E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 151: **FG320 Footprint Migration Differences**

Pin	Bank	XC3S500E	Migration	XC3S1200E	Migration	XC3S1600E	Migration	XC3S500E
A7	0	INPUT	→	I/O	←→	I/O	←	INPUT
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
D4	3	N.C.	→	I/O	←→	I/O	←	N.C.
D6	0	N.C.	→	I/O	←→	I/O	←	N.C.
D13	0	INPUT	→	I/O	←→	I/O	←	INPUT
E3	3	N.C.	→	I/O	←→	I/O	←	N.C.
E4	3	N.C.	→	I/O	←→	I/O	←	N.C.
E6	0	N.C.	→	I/O	←→	I/O	←	N.C.
E15	1	N.C.	→	I/O	←→	I/O	←	N.C.
E16	1	N.C.	→	I/O	←→	I/O	←	N.C.
E17	1	I/O	←	INPUT	←→	INPUT	→	I/O
F4	3	I/O	←	INPUT	←→	INPUT	→	I/O
N12	2	N.C.	→	I/O	←→	I/O	←	N.C.
N14	1	N.C.	→	I/O	←→	I/O	←	N.C.
N15	1	N.C.	→	I/O	←→	I/O	←	N.C.
P3	3	N.C.	→	I/O	←→	I/O	←	N.C.
P4	3	N.C.	→	I/O	←→	I/O	←	N.C.
P12	2	N.C.	→	I/O	←→	I/O	←	N.C.
P15	1	I/O	←	INPUT	←→	INPUT	→	I/O
P16	1	N.C.	→	I/O	←→	I/O	←	N.C.
R4	3	VREF(I/O)	←	VREF(INPUT)	←→	VREF(INPUT)	→	VREF(I/O)
U6	2	INPUT	→	I/O	←→	I/O	←	INPUT
U13	2	INPUT	→	I/O	←→	I/O	←	INPUT
V5	2	N.C.	→	I/O	←→	I/O	←	N.C.
V6	2	N.C.	→	VREF	←→	VREF	←	N.C.
V7	2	N.C.	→	I/O	←→	I/O	←	N.C.
DIFFERENCES			**26**		**0**		**26**	

Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.