AMD Xilinx - XC3S500E-4PQG208I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1164
Number of Logic Elements/Cells	10476
Total RAM Bits	368640
Number of I/O	158
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s500e-4pqg208i

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3E devices use register pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB's Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (ODDR2). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. DDR operation requires two clock signals (usually 50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 7. The Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, and then shifting it 180 degrees. This approach ensures minimal skew between the two signals. Alternatively, the inverter inside the IOB can be used to invert the clock signal, thus only using one clock line and both rising and falling edges of that clock line as the two clocks for the DDR flip-flops.

The storage-element pair on the Three-State path (TFF1 and TFF2) also can be combined with a local multiplexer to form a DDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register, and the inverted clock signal triggers the other register. The registers take turns capturing bits of the incoming DDR data signal. The primitive to allow this functionality is called IDDR2.

Aside from high bandwidth data transfers, DDR outputs also can be used to reproduce, or *mirror*, a clock signal on the output. This approach is used to transmit clock and data signals together (source synchronously). A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs is minimal.

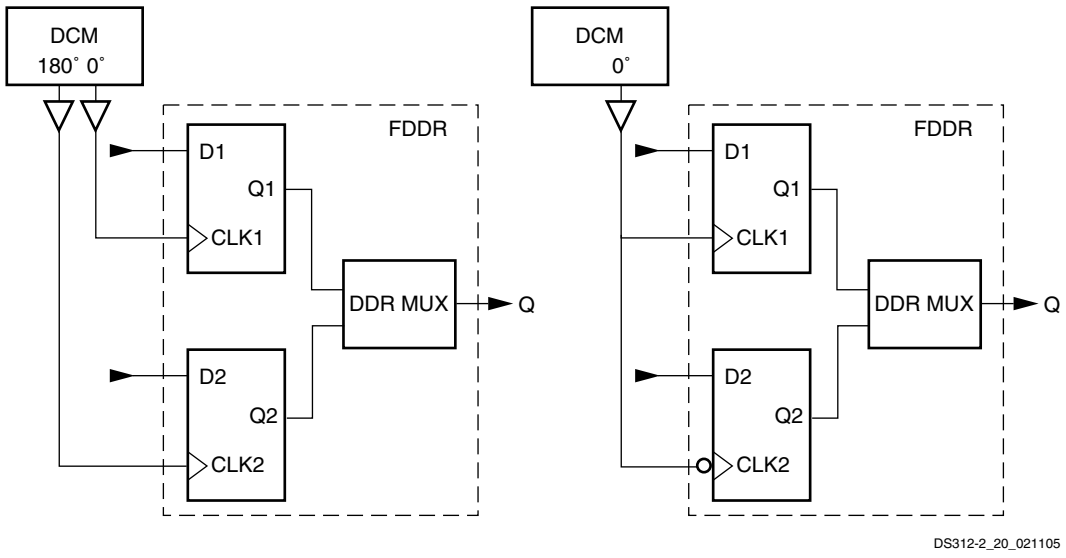

Figure 7: **Two Methods for Clocking the DDR Register**

Register Cascade Feature

In the Spartan-3E family, one of the IOBs in a differential pair can cascade its input storage elements with those in the other IOB as part of a differential pair. This is intended to make DDR operation at high speed much simpler to implement. The new DDR connections that are available are shown in Figure 5 (dashed lines), and are only available for routing between IOBs and are not accessible to the FPGA fabric. Note that this feature is only available when using the differential I/O standards LVDS, RSDS, and MINI_LVDS.

IDDR2

As a DDR input pair, the master IOB registers incoming data on the rising edge of ICLK1 (= D1) and the rising edge of ICLK2 (= D2), which is typically the same as the falling edge of ICLK1. This data is then transferred into the FPGA fabric. At some point, both signals must be brought into the same clock domain, typically ICLK1. This can be difficult at high frequencies because the available time is only one half of a clock cycle assuming a 50% duty cycle. See Figure 8 for a graphical illustration of this function.

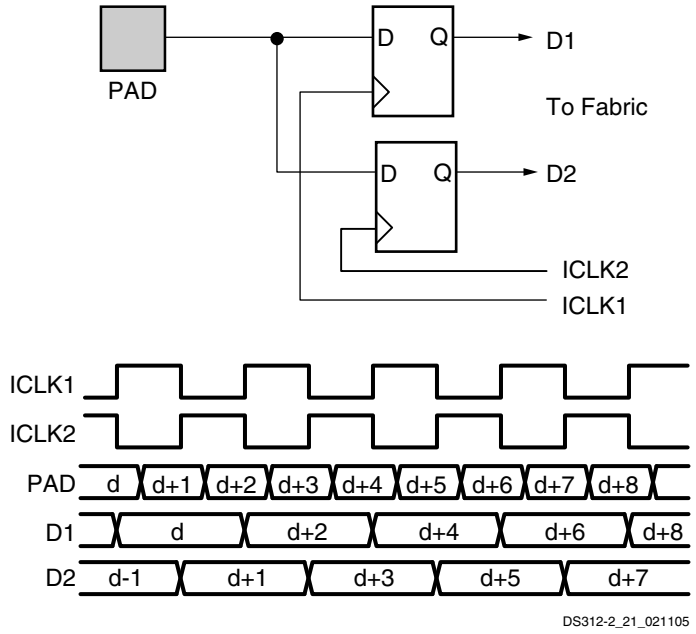

Figure 8: **Input DDR (without Cascade Feature)**

In the Spartan-3E device, the signal D2 can be cascaded into the storage element of the adjacent slave IOB. There it is re-registered to ICLK1, and only then fed to the FPGA fabric where it is now already in the same time domain as D1. Here, the FPGA fabric uses only the clock ICLK1 to process the received data. See Figure 9 for a graphical illustration of this function.

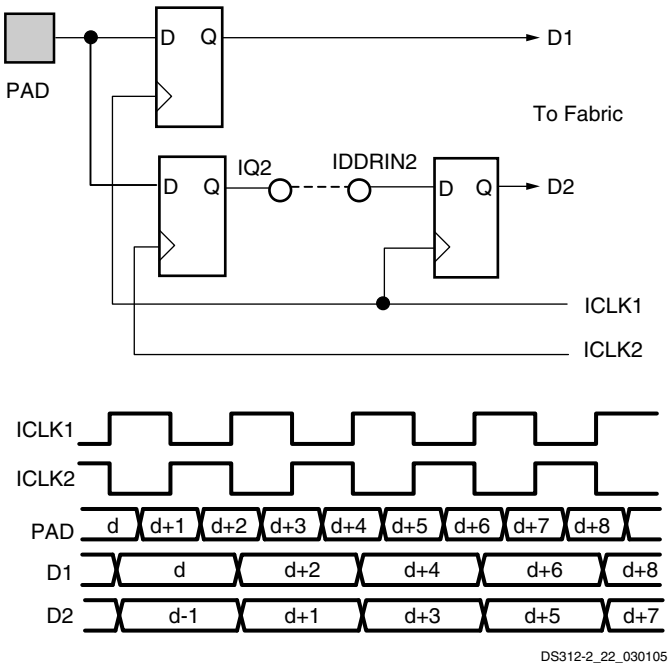

Figure 9: **Input DDR Using Spartan-3E Cascade Feature**

ODDR2

As a DDR output pair, the master IOB registers data coming from the FPGA fabric on the rising edge of OCLK1 (= D1) and the rising edge of OCLK2 (= D2), which is typically the same as the falling edge of OCLK1. These two bits of data are multiplexed by the DDR mux and forwarded to the output pin. The D2 data signal must be re-synchronized from the OCLK1 clock domain to the OCLK2 domain using FPGA slice flip-flops. Placement is critical at high frequencies, because the time available is only one half a clock cycle. See Figure 10 for a graphical illustration of this function.

The C0 or C1 alignment feature of the ODDR2 flip-flop, originally introduced in the Spartan-3E FPGA family, is not recommended or supported in the ISE development software. The ODDR2 flip-flop without the alignment feature remains fully supported. Without the alignment feature, the ODDR2 feature behaves equivalent to the ODDR flip-flop on previous Xilinx FPGA families.

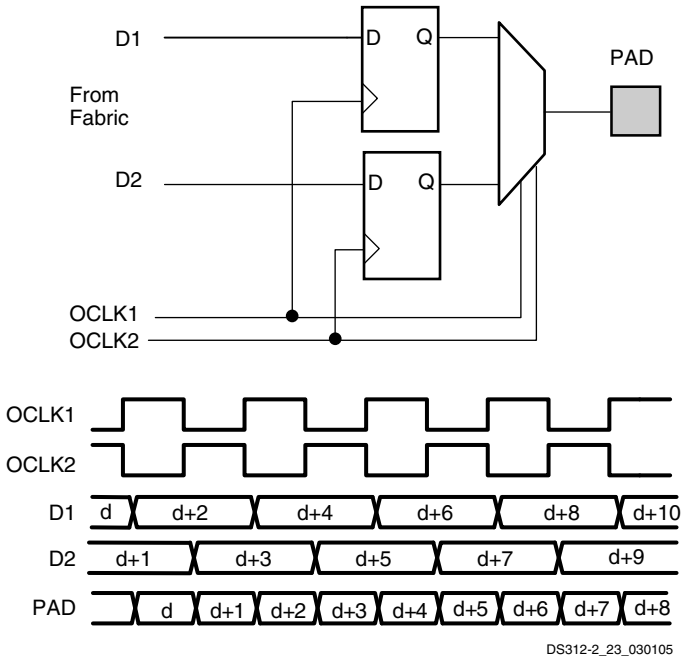

Figure 10: **Output DDR**

SelectIO Signal Standards

The Spartan-3E I/Os feature inputs and outputs that support a wide range of I/O signaling standards (Table 6 and Table 7). The majority of the I/Os also can be used to form differential pairs to support any of the differential signaling standards (Table 7).

To define the I/O signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the Xilinx Software Manuals and Help.

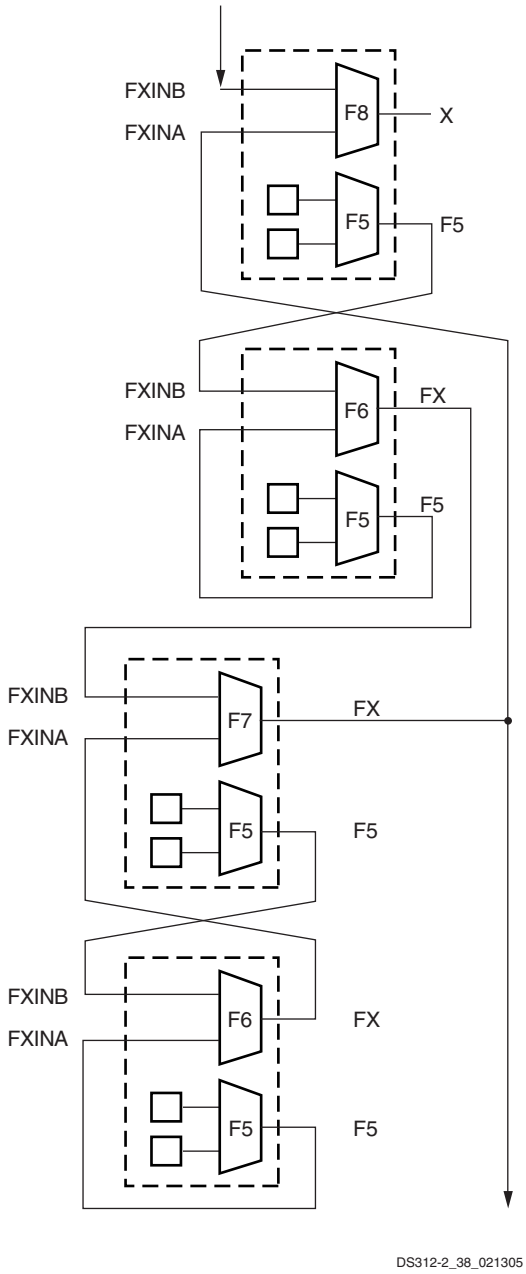

Figure 20: **MUXes and Dedicated Feedback in Spartan-3E CLB**

Table 11: **MUX Capabilities**

MUX	Usage	Input Source	Total Number of Inputs per Function		
			For Any Function	For MUX	For Limited Functions
F5MUX	F5MUX	LUTs	5	6 (4:1 MUX)	9
FiMUX	F6MUX	F5MUX	6	11 (8:1 MUX)	19
	F7MUX	F6MUX	7	20 (16:1 MUX)	39
	F8MUX	F7MUX	8	37 (32:1 MUX)	79

Block RAM Attribute Definitions

A block RAM has a number of attributes that control its behavior as shown in Table 24.

Table 24: **Block RAM Attributes**

Function	Attribute	Possible Values
Initial Content for Data Memory, Loaded during Configuration	INITxx (INIT_00 through INIT3F)	Each initialization string defines 32 hex values of the 16384-bit data memory of the block RAM.
Initial Content for Parity Memory, Loaded during Configuration	INITPxx (INITP_00 through INITP0F)	Each initialization string defines 32 hex values of the 2048-bit parity data memory of the block RAM.
Data Output Latch Initialization	INIT (single-port) INITA, INITB (dual-port)	Hex value the width of the chosen port.
Data Output Latch Synchronous Set/Reset Value	SRVAL (single-port) SRVAL_A, SRVAL_B (dual-port)	Hex value the width of the chosen port.
Data Output Latch Behavior during Write (see Block RAM Data Operations)	WRITE_MODE	WRITE_FIRST, READ_FIRST, NO_CHANGE

Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports. Table 25 describes the data operations of each port as a result of the block RAM control signals in their default active-High edges.

The waveforms for the write operation are shown in the top half of Figure 33, Figure 34, and Figure 35. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

Table 25: **Block RAM Function Table**

Input Signals								Output Signals		RAM Data	
GSR	EN	SSR	WE	CLK	ADDR	DIP	DI	DOP	DO	Parity	Data
Immediately After Configuration											
Loaded During Configuration								X	X	INITP_xx	INIT_xx
Global Set/Reset Immediately After Configuration											
1	X	X	X	X	X	X	X	INIT	INIT	No Chg	No Chg
RAM Disabled											
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
Synchronous Set/Reset											
0	1	1	0	↑	X	X	X	SRVAL	SRVAL	No Chg	No Chg
Synchronous Set/Reset During Write RAM											
0	1	1	1	↑	addr	pdata	Data	SRVAL	SRVAL	RAM(addr) ← pdata	RAM(addr) ← data
Read RAM, no Write Operation											
0	1	0	0	↑	addr	X	X	RAM(pdata)	RAM(data)	No Chg	No Chg
Write RAM, Simultaneous Read Operation											
0	1	0	1	↑	addr	pdata	Data	WRITE_MODE = WRITE_FIRST			
								pdata	data	RAM(addr) ← pdata	RAM(addr) ← data
								WRITE_MODE = READ_FIRST			
								RAM(data)	RAM(data)	RAM(addr) ← pdata	RAM(addr) ← pdata
								WRITE_MODE = NO_CHANGE			
								No Chg	No Chg	RAM(addr) ← pdata	RAM(addr) ← pdata

Table 31: **Direct Clock Input and Optional External Feedback to Left-Edge DCMs (XC3S1200E and XC3S1600E)**

Diff. Clock		Single-Ended Pin Number by Package Type								Left Edge		
		VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484	LHCLK	DCM/BUFGMUX	
											BUFGMUX_X0Y5	D
											BUFGMUX_X0Y4	C
Pair	P	P9	F3	P14	P22	H5	J5	K3	M5	LHCLK0	DCM_X0Y2	Clock Lines
	N	P10	F2	P15	P23	H6	J4	K2	L5	LHCLK1		
Pair	P	P11	F1	P16	P24	H3	J1	K7	L8	LHCLK2		
	N	P12	G1	P17	P25	H4	J2	L7	M8	LHCLK3		
											BUFGMUX_X0Y3	B
											BUFGMUX_X0Y2	A
											BUFGMUX_X0Y9	H
											BUFGMUX_X0Y8	G
Pair	P	P15	G3	P20	P28	J2	K3	M1	M1	LHCLK4	DCM_X0Y1	Clock Lines
	N	P16	H1	P21	P29	J3	K4	L1	N1	LHCLK5		
Pair	P	P17	H2	P22	P30	J5	K6	M3	M3	LHCLK6		
	N	P18	H3	P23	P31	J4	K5	L3	M4	LHCLK7		
											BUFGMUX_X0Y7	F
											BUFGMUX_X0Y6	E

Table 32: **Direct Clock Input and Optional External Feedback to Right-Edge DCMs (XC3S1200E and XC3S1600E)**

	Right Edge		Single-Ended Pin Number by Package Type								Diff. Clock	
	DCM/BUFGMUX	RHCLK	VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484		
D	BUFGMUX_X3Y5											
C	BUFGMUX_X3Y4											
Clock Lines	DCM_X3Y2	RHCLK7	P68	G13	P94	P135	H11	J14	J20	L19	N	Pair
		RHCLK6	P67	G14	P93	P134	H12	J15	K20	L18	P	
		RHCLK5	P66	H12	P92	P133	H14	J16	K14	L21	N	Pair
		RHCLK4	P65	H13	P91	P132	H15	J17	K13	L20	P	
B	BUFGMUX_X3Y3											
A	BUFGMUX_X3Y2											
H	BUFGMUX_X3Y9											
G	BUFGMUX_X3Y8											
Clock Lines	DCM_X3Y1	RHCLK3	P63	J14	P88	P129	J13	K14	L14	M16	N	Pair
		RHCLK2	P62	J13	P87	P128	J14	K15	L15	M15	P	
		RHCLK1	P61	J12	P86	P127	J16	K12	L16	M22	N	Pair
		RHCLK0	P60	K14	P85	P126	K16	K13	M16	N22	P	
F	BUFGMUX_X3Y7											
E	BUFGMUX_X3Y6											

Every FPGA input provides a possible DCM clock input, but the path is not temperature and voltage compensated like the GCLKs. Alternatively, clock signals within the FPGA optionally provide a DCM clock input via a Global Clock Multiplexer Buffer (BUFGMUX). The global clock net connects directly to the CLKIN input. The internal and external connections are shown in Figure 42a and Figure 42c, respectively.

The connections for the bottom-edge BUFGMUX elements are similar to the top-edge connections (see Figure 46).

On the left and right edges, only two clock inputs feed each pair of BUFGMUX elements.

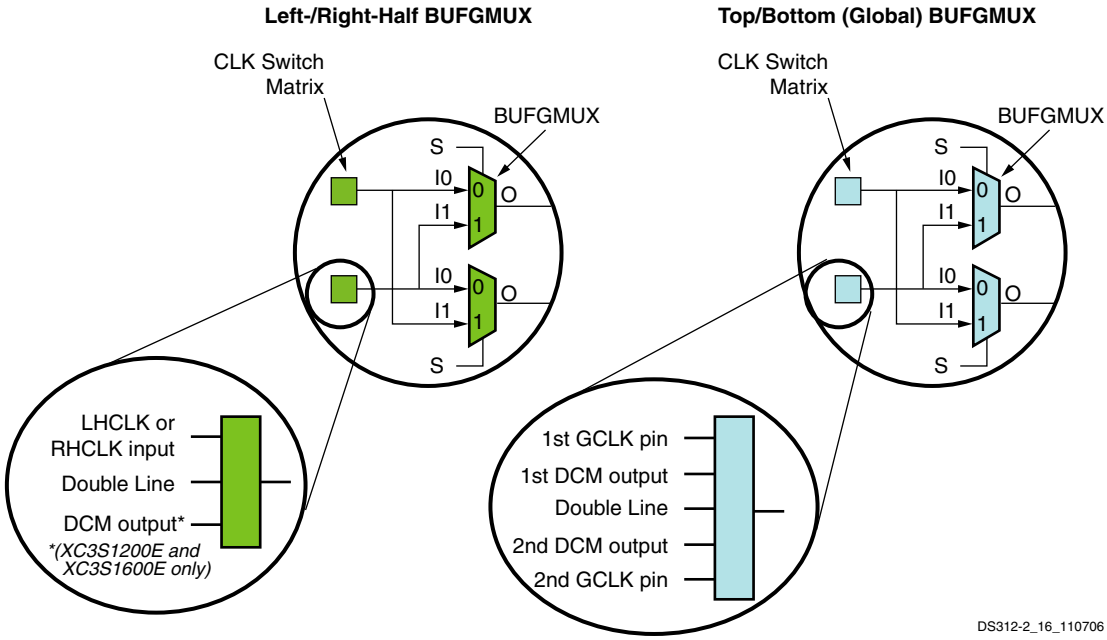

Figure 46: **Clock Switch Matrix to BUFGMUX Pair Connectivity**

Quadrant Clock Routing

The clock routing within the FPGA is quadrant-based, as shown in Figure 45. Each clock quadrant supports eight total clock signals, labeled 'A' through 'H' in Table 41 and Figure 47. The clock source for an individual clock line originates either from a global BUFGMUX element along the top and bottom edges or from a BUFGMUX element along the associated edge, as shown in Figure 47. The clock lines feed the synchronous resource elements (CLBs, IOBs, block RAM, multipliers, and DCMs) within the quadrant.

The four quadrants of the device are:

- Top Right (TR)
- Bottom Right (BR)
- Bottom Left (BL)
- Top Left (TL)

Note that the quadrant clock notation (TR, BR, BL, TL) is separate from that used for similar IOB placement constraints.

To estimate the quadrant location for a particular I/O, see the footprint diagrams in Module 4, Pinout Descriptions. For exact quadrant locations, use the floorplanning tool. In the QFP packages (VQ100, TQ144 and PQ208) the quadrant borders fall in the middle of each side of the package, at a GND pin. The clock inputs fall on the quadrant boundaries, as indicated in Table 42.

Table 42: **QFP Package Clock Quadrant Locations**

Clock Pins	Quadrant
GCLK[3:0]	BR
GCLK[7:4]	TR
GCLK[11:8]	TL
GCLK[15:12]	BL
RHCLK[3:0]	BR
RHCLK[7:4]	TR
LHCLK[3:0]	TL
LHCLK[7:4]	BL

In a few cases, a dedicated input is physically in one quadrant of the device but connects to a different clock quadrant:

- FT256, H16 is in clock quadrant BR
- FG320, K2 is in clock quadrant BL
- FG400, L8 is in clock quadrant TL and the I/O at N11 is in clock quadrant BL
- FG484, M2 is in clock quadrant TL and L15 is in clock quadrant BR

Compatible Flash Families

The Spartan-3E BPI configuration interface operates with a wide variety of x8 or x8/x16 parallel NOR Flash devices. Table 61 provides a few Flash memory families that operate with the Spartan-3E BPI interface. Consult the data sheet for the desired parallel NOR Flash to determine its suitability The basic timing requirements and waveforms are provided in Byte Peripheral Interface (BPI) Configuration Timing (Module 3).

Table 61: **Compatible Parallel NOR Flash Families**

Flash Vendor	Flash Memory Family
Numonyx	M29W, J3D StrataFlash
Atmel	AT29 / AT49
Spansion	S29
Macronix	MX29

CCLK Frequency

In BPI mode, the FPGA's internal oscillator generates the configuration clock frequency that controls all the interface timing. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option.

Table 62: **Maximum ConfigRate Settings for Parallel Flash PROMs (Commercial Temperature Range)**

Flash Read Access Time	Maximum *ConfigRate* Setting
250 ns	3
115 ns	6
45 ns	12

Table 62 shows the maximum ***ConfigRate*** settings for various typical PROM read access times over the Commercial temperature operating range. See Byte Peripheral Interface (BPI) Configuration Timing (Module 3) and UG332 for more detailed information. Despite using slower ***ConfigRate*** settings, BPI mode is equally fast as the other configuration modes. In BPI mode, data is accessed at the ***ConfigRate*** frequency and internally serialized with an 8X clock frequency.

Using the BPI Interface after Configuration

After the FPGA successfully completes configuration, all pins connected to the parallel Flash PROM are available as user I/Os.

If not using the parallel Flash PROM after configuration, drive LDC0 High to disable the PROM's chip-select input. The remainder of the BPI pins then become available to the FPGA application, including all 24 address lines, the eight data lines, and the LDC2, LDC1, and HDC control pins.

Because all the interface pins are user I/Os after configuration, the FPGA application can continue to use the interface pins to communicate with the parallel Flash PROM. Parallel Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits and beyond. However, a single Spartan-3E FPGA requires less than 6 Mbits for configuration. If desired, use a larger parallel Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data, such as serial numbers and Ethernet MAC IDs. In such an example, the FPGA configures from parallel Flash PROM. Then using FPGA logic after configuration, a MicroBlaze processor embedded within the FPGA can either execute code directly from parallel Flash PROM or copy the code to external DDR SDRAM and execute from DDR SDRAM. Similarly, the FPGA application can store non-volatile application data within the parallel Flash PROM.

The FPGA configuration data is stored starting at either at location 0 or the top of memory (addresses all ones) or at both locations for MultiBoot mode. Store any additional data beginning in other available parallel Flash PROM sectors. Do not mix configuration data and user data in the same sector.

Similarly, the parallel Flash PROM interface can be expanded to additional parallel peripherals.

The address, data, and LDC1 (OE#) and HDC (WE#) control signals are common to all parallel peripherals. Connect the chip-select input on each additional peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the chip-select line High via an internal pull-up resistor. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired peripheral. Refer to the individual peripheral data sheet for specific interface and communication protocol requirements.

The FPGA optionally supports a 16-bit peripheral interface by driving the LDC2 (BYTE#) control pin High after configuration. See Precautions Using x8/x16 Flash PROMs for additional information.

The FPGA provides up to 24 address lines during configuration, addressing up to 128 Mbits (16 Mbytes). If using a larger parallel PROM, connect the upper address lines to FPGA user I/O. During configuration, the upper address lines will be pulled High if HSWAP = 0. Otherwise, use external pull-up or pull-down resistors on these address lines to define their values during configuration.

Precautions Using x8/x16 Flash PROMs

(D) Most low- to mid-density PROMs are byte-wide (x8) only. Many higher-density Flash PROMs support both byte-wide (x8) and halfword-wide (x16) data paths and include a mode input called BYTE# that switches between x8 or x16. During configuration, Spartan-3E FPGAs only

support byte-wide data. However, after configuration, the FPGA supports either x8 or x16 modes. In x16 mode, up to eight additional user I/O pins are required for the upper data bits, D[15:8].

Connecting a Spartan-3E FPGA to a x8/x16 Flash PROM is simple, but does require a precaution. Various Flash PROM vendors use slightly different interfaces to support both x8 and x16 modes. Some vendors (Intel, Micron, some STMicroelectronics devices) use a straightforward interface with pin naming that matches the FPGA connections. However, the PROM's A0 pin is wasted in x16 applications and a separate FPGA user-I/O pin is required for the D15 data line. Fortunately, the FPGA A0 pin is still available as a user I/O after configuration, even though it connects to the Flash PROM.

Other vendors (AMD, Atmel, Silicon Storage Technology, some STMicroelectronics devices) use a pin-efficient interface but change the function of one pin, called IO15/A-1, depending if the PROM is in x8 or x16 mode. In x8 mode, BYTE# = 0, this pin is the least-significant address line. The A0 address line selects the halfword location. The A-1 address line selects the byte location. When in x16 mode, BYTE# = 1, the IO15/A-1 pin becomes the most-significant data bit, D15 because byte addressing is not required in this mode. Check to see if the Flash PROM has a pin named "IO15/A-1" or "DQ15/A-1". If so, be careful to connect x8/x16 Flash PROMs correctly, as shown in Table 63. Also, remember that the D[14:8] data connections require FPGA user I/O pins but that the D15 data is already connected for the FPGA's A0 pin.

Table 63: **FPGA Connections to Flash PROM with IO15/A-1 Pin**

FPGA Pin	Connection to Flash PROM with IO15/A-1 Pin	x8 Flash PROM Interface After FPGA Configuration	x16 Flash PROM Interface After FPGA Configuration
LDC2	BYTE#	Drive LDC2 Low or leave unconnected and tie PROM BYTE# input to GND	Drive LCD2 High
LDC1	OE#	Active-Low Flash PROM output-enable control	Active-Low Flash PROM output-enable control
LDC0	CS#	Active-Low Flash PROM chip-select control	Active-Low Flash PROM chip-select control
HDC	WE#	Flash PROM write-enable control	Flash PROM write-enable control
A[23:1]	A[n:0]	A[n:0]	A[n:0]
A0	IO15/A-1	IO15/A-1 is the least-significant address input	IO15/A-1 is the most-significant data line, IO15
D[7:0]	IO[7:0]	IO[7:0]	IO[7:0]
User I/O	Upper data lines IO[14:8] not required unless used as x16 Flash interface after configuration	Upper data lines IO[14:8] not required	IO[14:8]

Some x8/x16 Flash PROMs have a long setup time requirement on the BYTE# signal. For the FPGA to configure correctly, the PROM must be in x8 mode with BYTE# = 0 at power-on or when the FPGA's PROG_B pin is pulsed Low. If required, extend the BYTE# setup time for a 3.3V PROM using an external 680 Ω pull-down resistor on the FPGA's LDC2 pin or by delaying assertion of the CSI_B select input to the FPGA.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 59. Use BPI mode (M[2:0] = <0:1:0> or <0:1:1>) for the FPGA connected to the parallel NOR Flash PROM and Slave Parallel mode (M[2:0] = <1:1:0>) for all downstream FPGAs in the daisy-chain. If there are more than two FPGAs in the chain, then last FPGA in the chain can be from any Xilinx FPGA family. However, all intermediate FPGAs located in the chain between the first and last FPGAs must from either the Spartan-3E or Virtex®-5 FPGA families.

After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the parallel Flash PROM, the master device continues generating addresses to the Flash PROM and asserts its CSO_B output Low, enabling the next FPGA in the daisy-chain. The next FPGA then receives parallel configuration data from the Flash PROM. The master FPGA's CCLK output synchronizes data capture.

If HSWAP = 1, an external 4.7kΩ pull-up resistor must be added on the CSO_B pin. If HSWAP = 0, no external pull-up is necessary.

Design Note

BPI mode daisy chain software support is available starting in ISE 8.2i.

http://www.xilinx.com/support/answers/23061.htm

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

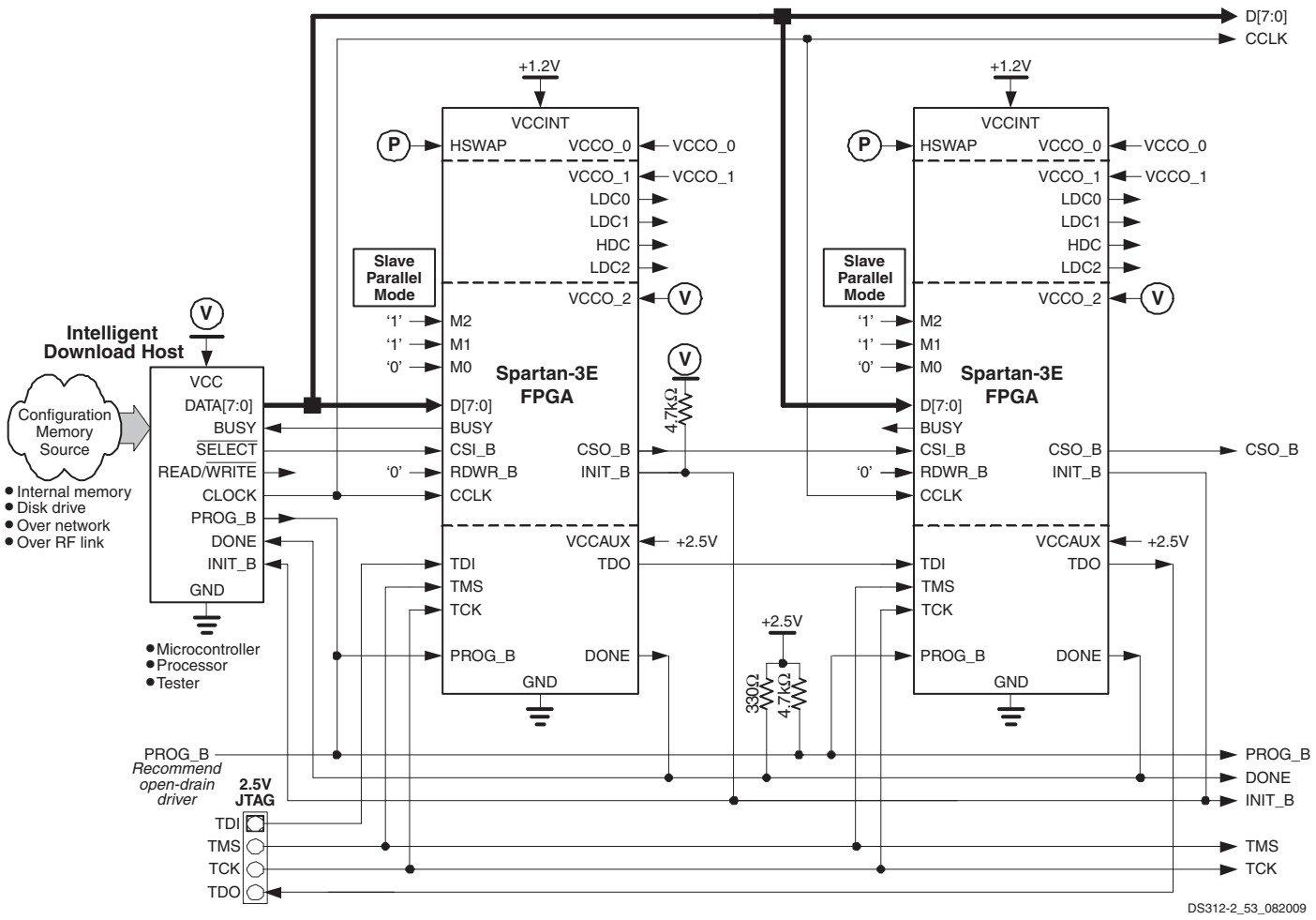

Figure 62: **Daisy-Chaining using Slave Parallel Mode**

Slave Serial Mode

For additional information, refer to the “Slave Serial Mode” chapter in UG332.

In Slave Serial mode (M[2:0] = <1:1:1>), an external host such as a microprocessor or microcontroller writes serial configuration data into the FPGA, using the synchronous serial interface shown in Figure 63. The serial configuration data is presented on the FPGA’s DIN input pin with sufficient setup time before each rising edge of the externally generated CCLK clock input.

The intelligent host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host then continues supplying data and clock signals until either the DONE pin goes High, indicating a successful configuration, or until the INIT_B pin goes Low, indicating a configuration error. The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA’s start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

Maximum Bitstream Size for Daisy-Chains

The maximum bitstream length supported by Spartan-3E FPGAs in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 720 XC3S1600E FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.

Configuration Sequence

For additional information including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in UG332.

The Spartan-3E configuration process is three-stage process that begins after the FPGA powers on (a POR event) or after the PROG_B input is asserted. Power-On Reset (POR) occurs after the V_{CCINT}, V_{CCAUX}, and the V_{CCO} Bank 2 supplies reach their respective input threshold levels. After either a POR or PROG_B event, the three-stage configuration process begins.

1. The FPGA clears (initializes) the internal configuration memory.
2. Configuration data is loaded into the internal memory.
3. The user-application is activated by a start-up process.

Figure 66 is a generalized block diagram of the Spartan-3E configuration logic, showing the interaction of different device inputs and Bitstream Generator (BitGen) options. A flow diagram for the configuration sequence of the Serial and Parallel modes appears in Figure 66. Figure 67 shows the Boundary-Scan or JTAG configuration sequence.

Initialization

Configuration automatically begins after power-on or after asserting the FPGA PROG_B pin, unless delayed using the FPGA's INIT_B pin. The FPGA holds the open-drain INIT_B signal Low while it clears its internal configuration memory. Externally holding the INIT_B pin Low forces the configuration sequencer to wait until INIT_B again goes High.

The FPGA signals when the memory-clearing phase is complete by releasing the open-drain INIT_B pin, allowing the pin to go High via the external pull-up resistor to VCCO_2.

Loading Configuration Data

After initialization, configuration data is written to the FPGA's internal memory. The FPGA holds the Global Set/Reset (GSR) signal active throughout configuration, holding all FPGA flip-flops in a reset state. The FPGA signals when the entire configuration process completes by releasing the DONE pin, allowing it to go High.

The FPGA configuration sequence can also be initiated by asserting PROG_B. Once released, the FPGA begins clearing its internal configuration memory, and progresses through the remainder of the configuration process.

Readback

FPGA configuration data can be read back using either the Slave Parallel or JTAG mode. This function is disabled if the Bitstream Generator ***Security*** option is set to either ***Level1*** or ***Level2***.

Along with the configuration data, it is possible to read back the contents of all registers and distributed RAM.

To synchronously control when register values are captured for readback, use the CAPTURE_SPARTAN3 library primitive, which applies for both Spartan-3 and Spartan-3E FPGA families.

The Readback feature is available in most Spartan-3E FPGA product options, as indicated in Table 68. The Readback feature is not available in the XC3S1200E and XC3S1600E FPGAs when using the -4 speed grade in the Commercial temperature grade. Similarly, block RAM Readback support is not available in the -4 speed grade, Commercial temperature devices. If Readback is required in an XC3S1200E or XC3S1600E FPGA, or if block RAM Readback is required on any Spartan-3E FPGA, upgrade to either the Industrial temperature grade version or the -5 speed grade.

The Xilinx iMPACT programming software uses the Readback feature for its optional Verify and Readback operations. The Xilinx ChipScope™ software presently does not use Readback but may in future updates.

Table 68: **Readback Support in Spartan-3E FPGAs**

Temperature Range	Commercial		Industrial
Speed Grade	**-4**	**-5**	**-4**
Block RAM Readback			
All Spartan-3E FPGAs	No	Yes	Yes
General Readback (registers, distributed RAM)			
XC3S100E	Yes	Yes	Yes
XC3S250E	Yes	Yes	Yes
XC3S500E	Yes	Yes	Yes
XC3S1200E	No	Yes	Yes
XC3S1600E	No	Yes	Yes

I/O Timing

Table 86: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max[2]	Max[2]	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used.	LVCMOS25[3], 12 mA output drive, Fast slew rate, with DCM[4]	XC3S100E	2.66	2.79	ns
			XC3S250E	3.00	3.45	ns
			XC3S500E	3.01	3.46	ns
			XC3S1200E	3.01	3.46	ns
			XC3S1600E	3.00	3.45	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not used.	LVCMOS25[3], 12 mA output drive, Fast slew rate, without DCM	XC3S100E	5.60	5.92	ns
			XC3S250E	4.91	5.43	ns
			XC3S500E	4.98	5.51	ns
			XC3S1200E	5.36	5.94	ns
			XC3S1600E	5.45	6.05	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 91. If the latter is true, *add* the appropriate Output adjustment from Table 94.
4. DCM output jitter is included in all measurements.

Table 105: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Phase Alignment(4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	-	±200	-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		-	±[1% of CLKIN period + 100]	-	±[1% of CLKIN period + 100]	ps
		All others		-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	600	-	600	µs
Delay Lines								
DCM_DELAY_STEP	Finest delay resolution		All	20	40	20	40	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 104.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI.
   Example: The data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps.

Digital Frequency Synthesizer (DFS)

Table 106: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} ≤ 150 MHz	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} > 150 MHz	-	±150	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	-	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 104.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

CP132 Footprint

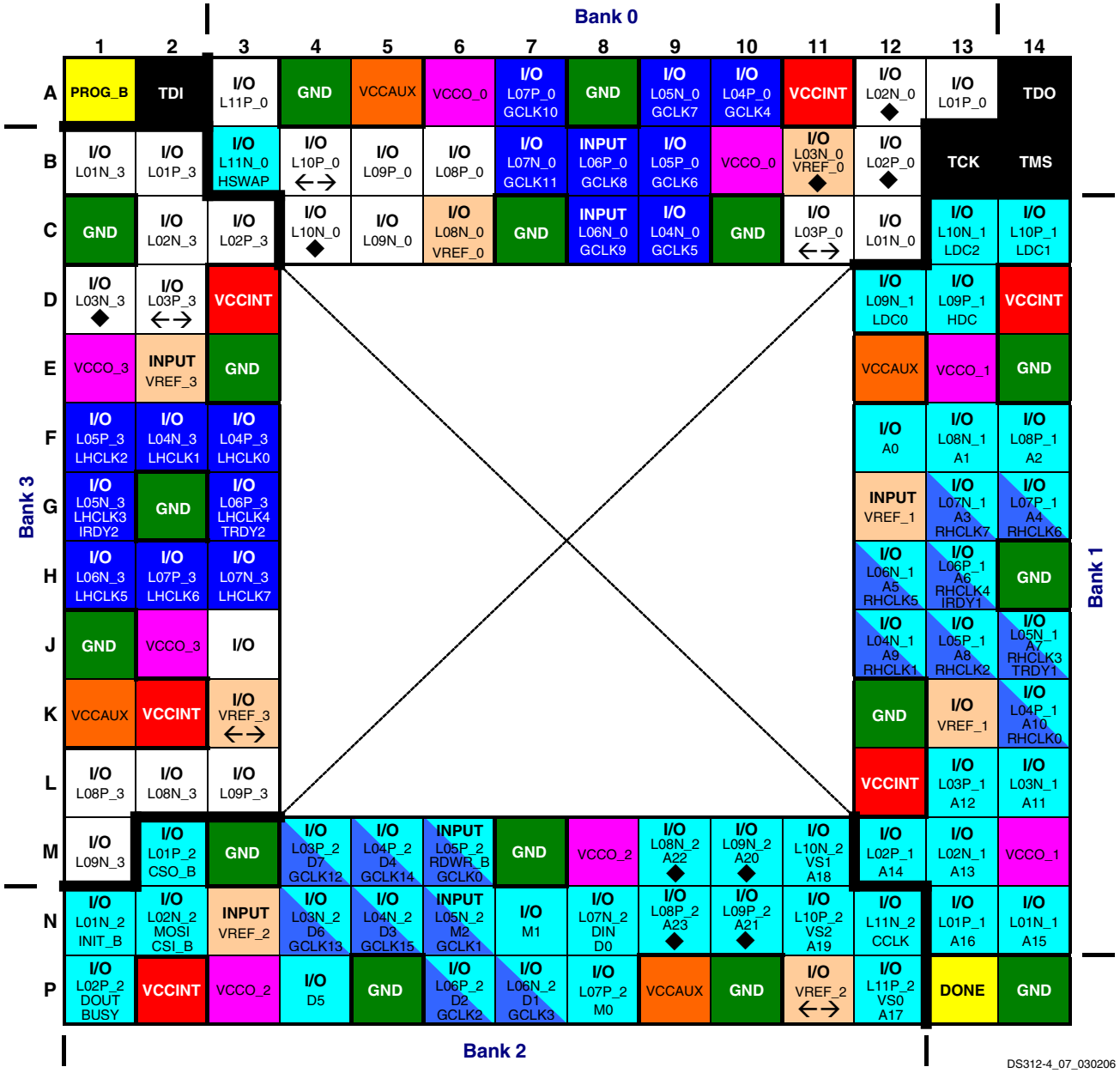

Figure 81: **CP132 Package Footprint (top view)**

16-22	**I/O:** Unrestricted, general-purpose user I/O	42-46	**DUAL:** Configuration pin, then possible user I/O	7-8	**VREF:** User I/O or input voltage reference for bank
0-2	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)
9	**N.C.:** Unconnected balls on the XC3S100E FPGA (◆)	16	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
2	N.C. (◆)	IO_L14N_2/VREF_2	IO_L14N_2/VREF_2	R10	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
2	N.C. (◆)	IO_L14P_2	IO_L14P_2	P10	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	IO_L15N_2	IO_L15N_2	IO_L15N_2	M10	I/O
2	IO_L15P_2	IO_L15P_2	IO_L15P_2	N10	I/O
2	IO_L16N_2/A22	IO_L16N_2/A22	IO_L16N_2/A22	P11	DUAL
2	IO_L16P_2/A23	IO_L16P_2/A23	IO_L16P_2/A23	R11	DUAL
2	IO_L18N_2/A20	IO_L18N_2/A20	IO_L18N_2/A20	N12	DUAL
2	IO_L18P_2/A21	IO_L18P_2/A21	IO_L18P_2/A21	P12	DUAL
2	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	R13	DUAL
2	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	T13	DUAL
2	IO_L20N_2/CCLK	IO_L20N_2/CCLK	IO_L20N_2/CCLK	R14	DUAL
2	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	P14	DUAL
2	IP	IP	IP	T2	INPUT
2	IP	IP	IP	T14	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	R3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	T3	INPUT
2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	T7	VREF
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	R7	INPUT
2	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	R9	DUAL/GCLK
2	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	T9	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	M11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	N11	INPUT
2	VCCO_2	VCCO_2	VCCO_2	L7	VCCO
2	VCCO_2	VCCO_2	VCCO_2	L10	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R5	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	B2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	B1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	C2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	C1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E4	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E3	I/O
3	N.C. (◆)	IO_L04N_3/VREF_3	IO_L04N_3/VREF_3	F4	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	F3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	E1	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	D1	I/O
3	IO_L06N_3	IO_L06N_3	IO_L06N_3	G4	I/O

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
VCCAUX	VCCAUX	VCCAUX	VCCAUX	A11	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	F1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	F16	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	L1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	L16	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	T6	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	T11	VCCAUX
VCCINT	VCCINT	VCCINT	VCCINT	D4	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	D13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E12	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	M5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	M12	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N4	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N13	VCCINT

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	N.C. (◆)	IO_L04N_3	IO_L04N_3	E3	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	E4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	F2	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	F1	I/O
3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	G4	VREF
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G3	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G5	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G6	I/O
3	IO_L08N_3	IO_L08N_3	IO_L08N_3	H5	I/O
3	IO_L08P_3	IO_L08P_3	IO_L08P_3	H6	I/O
3	IO_L09N_3	IO_L09N_3	IO_L09N_3	H3	I/O
3	IO_L09P_3	IO_L09P_3	IO_L09P_3	H4	I/O
3	IO_L10N_3	IO_L10N_3	IO_L10N_3	H1	I/O
3	IO_L10P_3	IO_L10P_3	IO_L10P_3	H2	I/O
3	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	J4	LHCLK
3	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	J5	LHCLK
3	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	J2	LHCLK
3	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	J1	LHCLK
3	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	K4	LHCLK
3	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	K3	LHCLK
3	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	K5	LHCLK
3	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	K6	LHCLK
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L2	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	L1	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	L4	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	L3	I/O
3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	L5	VREF
3	IO_L17P_3	IO_L17P_3	IO_L17P_3	L6	I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	M3	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	M4	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	M6	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	M5	I/O
3	IO_L20N_3	IO_L20N_3	IO_L20N_3	N5	I/O
3	IO_L20P_3	IO_L20P_3	IO_L20P_3	N4	I/O
3	IO_L21N_3	IO_L21N_3	IO_L21N_3	P1	I/O
3	IO_L21P_3	IO_L21P_3	IO_L21P_3	P2	I/O
3	N.C. (◆)	IO_L22N_3	IO_L22N_3	P4	**500E:** N.C. **1200E:** I/O **1600E:** I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IP_L14P_2	T9	INPUT
2	IP_L17N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L17P_2/RDWR_B/ GCLK0	P11	DUAL/ GCLK
2	IP_L20N_2	T12	INPUT
2	IP_L20P_2	R12	INPUT
2	IP_L23N_2/VREF_2	T13	VREF
2	IP_L23P_2	T14	INPUT
2	IP_L26N_2	V14	INPUT
2	IP_L26P_2	V15	INPUT
2	IP_L29N_2	W16	INPUT
2	IP_L29P_2	Y16	INPUT
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	D3	I/O
3	IO_L02N_3/VREF_3	E3	VREF
3	IO_L02P_3	E4	I/O
3	IO_L03N_3	C1	I/O
3	IO_L03P_3	B1	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F3	I/O
3	IO_L05P_3	F4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L07N_3	G4	I/O
3	IO_L07P_3	G3	I/O
3	IO_L08N_3	G5	I/O
3	IO_L08P_3	H5	I/O
3	IO_L09N_3/VREF_3	H3	VREF
3	IO_L09P_3	H2	I/O
3	IO_L10N_3	H7	I/O
3	IO_L10P_3	H6	I/O
3	IO_L11N_3	J4	I/O
3	IO_L11P_3	J3	I/O
3	IO_L12N_3	J1	I/O
3	IO_L12P_3	J2	I/O
3	IO_L13N_3	J6	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IO_L13P_3	K6	I/O
3	IO_L14N_3/LHCLK1	K2	LHCLK
3	IO_L14P_3/LHCLK0	K3	LHCLK
3	IO_L15N_3/LHCLK3/IRDY2	L7	LHCLK
3	IO_L15P_3/LHCLK2	K7	LHCLK
3	IO_L16N_3/LHCLK5	L1	LHCLK
3	IO_L16P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L17N_3/LHCLK7	L3	LHCLK
3	IO_L17P_3/LHCLK6	M3	LHCLK
3	IO_L18N_3	M7	I/O
3	IO_L18P_3	M8	I/O
3	IO_L19N_3	M4	I/O
3	IO_L19P_3	M5	I/O
3	IO_L20N_3/VREF_3	N6	VREF
3	IO_L20P_3	M6	I/O
3	IO_L21N_3	N2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	P7	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	N4	I/O
3	IO_L23P_3	N3	I/O
3	IO_L24N_3	R1	I/O
3	IO_L24P_3	P1	I/O
3	IO_L25N_3	R5	I/O
3	IO_L25P_3	P5	I/O
3	IO_L26N_3	T2	I/O
3	IO_L26P_3	R2	I/O
3	IO_L27N_3	R4	I/O
3	IO_L27P_3	R3	I/O
3	IO_L28N_3/VREF_3	T1	VREF
3	IO_L28P_3	U1	I/O
3	IO_L29N_3	T3	I/O
3	IO_L29P_3	U3	I/O
3	IO_L30N_3	V1	I/O
3	IO_L30P_3	V2	I/O
3	IP	F5	INPUT
3	IP	G1	INPUT
3	IP	G6	INPUT
3	IP	H1	INPUT
3	IP	J5	INPUT
3	IP	L5	INPUT
3	IP	L8	INPUT
3	IP	M2	INPUT

Table 155: **User I/Os Per Bank for the XC3S1600E in the FG484 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	94	56	22	1	7	8
Right	1	94	50	16	21	7	0[2]
Bottom	2	94	45	18	24	7	0[2]
Left	3	94	63	16	0	7	8
TOTAL		**376**	**214**	**72**	**46**	**28**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The XC3S1600E FPGA is the only Spartan-3E device offered in the FG484 package.