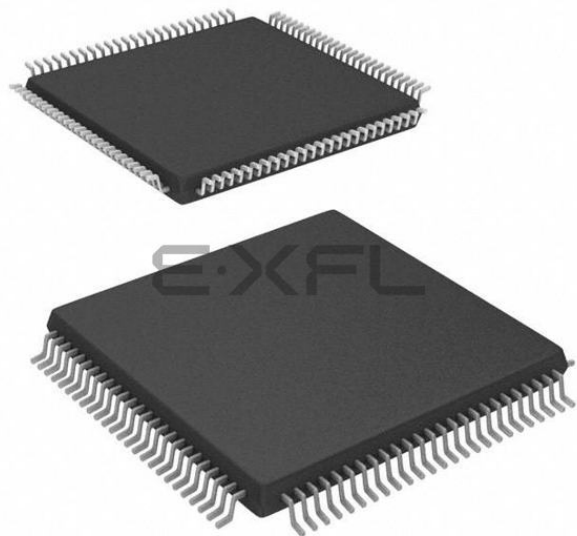




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1164
Number of Logic Elements/Cells	10476
Total RAM Bits	368640
Number of I/O	66
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s500e-4vqg100i

Configuration

Spartan-3E FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

Furthermore, Spartan-3E FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

I/O Capabilities

The Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. [Table 2](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz, and in some devices, [66 MHz](#)
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: Available User I/Os and Differential (Diff) I/O Pairs

Package	VQ100 VQG100		CP132 CPG132		TQ144 TQG144		PQ208 PQG208		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484	
Footprint Size (mm)	16 x 16		8 x 8		22 x 22		30.5 x 30.5		17 x 17		19 x 19		21 x 21		23 x 23	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S100E	66 ⁽²⁾ <i>9(7)</i>	30 <i>(2)</i>	83 <i>(11)</i>	35 <i>(2)</i>	108 <i>(28)</i>	40 <i>(4)</i>	-	-	-	-	-	-	-	-	-	-
XC3S250E	66 <i>(7)</i>	30 <i>(2)</i>	92 <i>(7)</i>	41 <i>(2)</i>	108 <i>(28)</i>	40 <i>(4)</i>	158 <i>(32)</i>	65 <i>(5)</i>	172 <i>(40)</i>	68 <i>(8)</i>	-	-	-	-	-	-
XC3S500E	66 ⁽³⁾ <i>(7)</i>	30 <i>(2)</i>	92 <i>(7)</i>	41 <i>(2)</i>	-	-	158 <i>(32)</i>	65 <i>(5)</i>	190 <i>(41)</i>	77 <i>(8)</i>	232 <i>(56)</i>	92 <i>(12)</i>	-	-	-	-
XC3S1200E	-	-	-	-	-	-	-	-	190 <i>(40)</i>	77 <i>(8)</i>	250 <i>(56)</i>	99 <i>(12)</i>	304 <i>(72)</i>	124 <i>(20)</i>	-	-
XC3S1600E	-	-	-	-	-	-	-	-	-	-	250 <i>(56)</i>	99 <i>(12)</i>	304 <i>(72)</i>	124 <i>(20)</i>	376 <i>(82)</i>	156 <i>(21)</i>

Notes:

1. All Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4, [Pinout Descriptions](#).
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in *italics* indicates the number of input-only pins.
3. The XC3S500E is available in the VQG100 Pb-free package and not the standard VQ100. The VQG100 and VQ100 pin-outs are identical and general references to the VQ100 will apply to the XC3S500E.



Spartan-3 FPGA Family: Functional Description

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Product Specification

Design Documentation Available

The functionality of the Spartan®-3E FPGA family is now described and updated in the following documents. The topics covered in each guide are listed below.

- [UG331: Spartan-3 Generation FPGA User Guide](#)
 - Clocking Resources
 - Digital Clock Managers (DCMs)
 - Block RAM
 - Configurable Logic Blocks (CLBs)
 - Distributed RAM
 - SRL16 Shift Registers
 - Carry and Arithmetic Logic
 - I/O Resources
 - Embedded Multiplier Blocks
 - Programmable Interconnect
 - ISE® Design Tools
 - IP Cores
 - Embedded Processing and Control Solutions
 - Pin Types and Package Overview
 - Package Drawings
 - Powering FPGAs
 - Power Management
- [UG332: Spartan-3 Generation Configuration User Guide](#)
 - Configuration Overview
 - Configuration Pins and Behavior
 - Bitstream Sizes
 - Detailed Descriptions by Mode
 - Master Serial Mode using Xilinx® Platform Flash PROM
 - Master SPI Mode using Commodity SPI Serial Flash PROM
 - Master BPI Mode using Commodity Parallel NOR Flash PROM
 - Slave Parallel (SelectMAP) using a Processor
 - Slave Serial using a Processor
 - JTAG Mode
 - ISE iMPACT Programming Examples
 - MultiBoot Reconfiguration

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Spartan-3E FPGA Starter Kit

For specific hardware examples, please see the Spartan-3E FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3E FPGA Starter Kit Board page
<http://www.xilinx.com/s3estarter>
- [UG230: Spartan-3E FPGA Starter Kit User Guide](#)

Spartan-3E FPGAs provide additional input flexibility by allowing I/O standards to be mixed in different banks. For a particular V_{CCO} voltage, Table 6 and Table 7 list all of the

IOSTANDARDS that can be combined and if the IOSTANDARD is supported as an input only or can be used for both inputs and outputs.

Table 6: Single-Ended IOSTANDARD Bank Compatibility

Single-Ended IOSTANDARD	V_{CCO} Supply/Compatibility					Input Requirements	
	1.2V	1.5V	1.8V	2.5V	3.3V	V_{REF}	Board Termination Voltage (V_{TT})
LVTTTL	-	-	-	-	Input/Output	N/R ⁽¹⁾	N/R
LVC MOS33	-	-	-	-	Input/Output	N/R	N/R
LVC MOS25	-	-	-	Input/Output	Input	N/R	N/R
LVC MOS18	-	-	Input/Output	Input	Input	N/R	N/R
LVC MOS15	-	Input/Output	Input	Input	Input	N/R	N/R
LVC MOS12	Input/Output	Input	Input	Input	Input	N/R	N/R
PCI33_3	-	-	-	-	Input/Output	N/R	N/R
PCI66_3	-	-	-	-	Input/Output	N/R	N/R
HSTL_I_18	-	-	Input/Output	Input	Input	0.9	0.9
HSTL_III_18	-	-	Input/Output	Input	Input	1.1	1.8
SSTL18_I	-	-	Input/Output	Input	Input	0.9	0.9
SSTL2_I	-	-	-	Input/Output	Input	1.25	1.25

Notes:

1. N/R - Not required for input operation.

Configurable Logic Block (CLB) and Slice Resources

For additional information, refer to the “Using Configurable Logic Blocks (CLBs)” chapter in [UG331](#).

CLB Overview

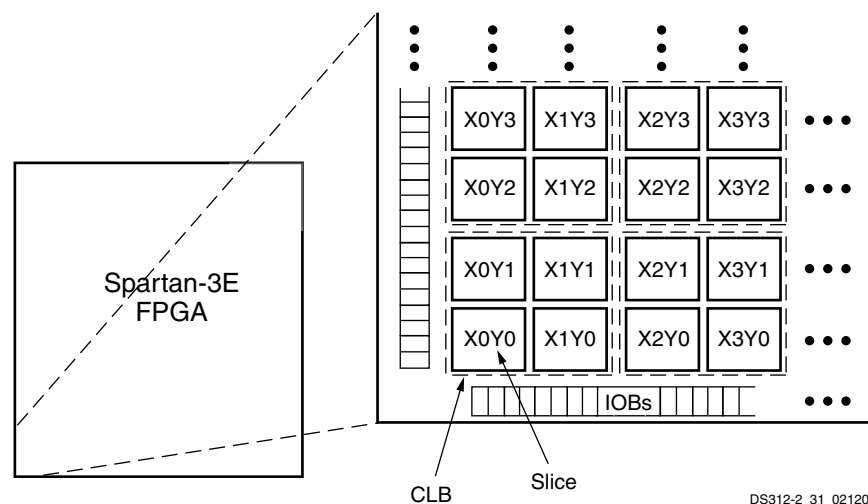
The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB contains four slices, and each slice contains two Look-Up Tables (LUTs) to implement logic and two dedicated storage elements that can be used as flip-flops or latches. The LUTs can be used as a 16x1 memory (RAM16) or as a 16-bit shift register

(SRL16), and additional multiplexers and carry logic simplify wide logic and arithmetic functions. Most general-purpose logic in a design is automatically mapped to the slice resources in the CLBs. Each CLB is identical, and the Spartan-3E family CLB structure is identical to that for the Spartan-3 family.

CLB Array

The CLBs are arranged in a regular array of rows and columns as shown in [Figure 14](#).

Each density varies by the number of rows and columns of CLBs (see [Table 9](#)).



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Figure 14: CLB Locations

Table 9: Spartan-3E CLB Resources

Device	CLB Rows	CLB Columns	CLB Total ⁽¹⁾	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S100E	22	16	240	960	1,920	2,160	960	15,360
XC3S250E	34	26	612	2,448	4,896	5,508	2,448	39,168
XC3S500E	46	34	1,164	4,656	9,312	10,476	4,656	74,496
XC3S1200E	60	46	2,168	8,672	17,344	19,512	8,672	138,752
XC3S1600E	76	58	3,688	14,752	29,504	33,192	14,752	236,032

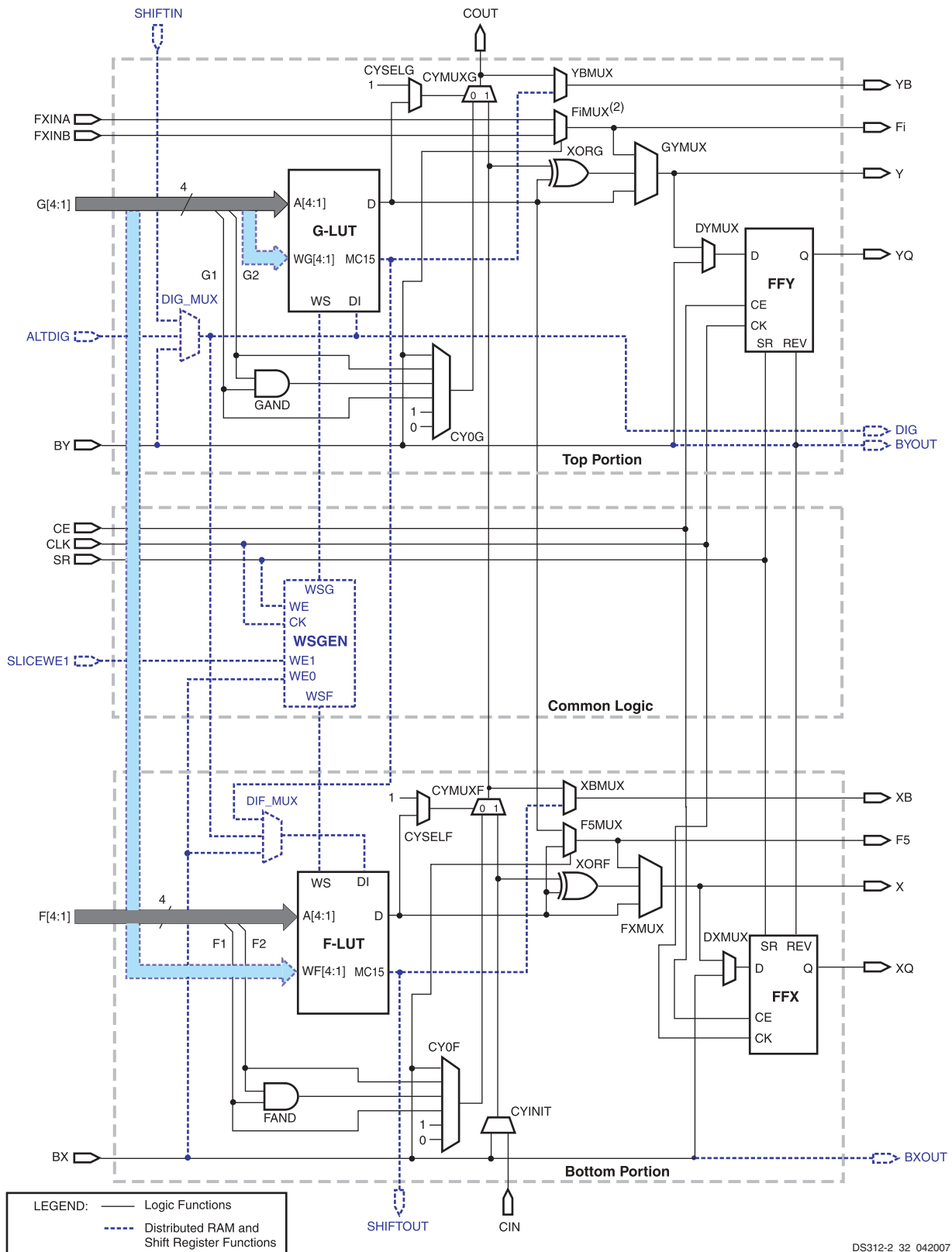
Notes:

- The number of CLBs is less than the multiple of the rows and columns because the block RAM/multiplier blocks and the DCMs are embedded in the array (see [Figure 1](#) in Module 1).

Slices

Each CLB comprises four interconnected slices, as shown in [Figure 16](#). These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain. The left pair supports both logic and memory functions and its slices are called SLICEM. The right pair supports logic only and its slices are called SLICEL. Therefore half the

LUTs support both logic and memory (including both RAM16 and SRL16 shift registers) while half support logic only, and the two types alternate throughout the array columns. The SLICEL reduces the size of the CLB and lowers the cost of the device, and can also provide a performance advantage over the SLICEM.



DS312-2_32_042007

Notes:

- Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
- The index i can be 6, 7, or 8, depending on the slice. The upper SLICEL has an F8MUX, and the upper SLICEM has an F7MUX. The lower SLICEL and SLICEM both have an F6MUX.

Figure 15: Simplified Diagram of the Left-Hand SLICEM

initialized distributed RAM contents are not disturbed during the configuration process.

The distributed RAM is useful for smaller amounts of memory. Larger memory requirements can use the dedicated 18Kbit RAM blocks (see [Block RAM](#)).

Shift Registers

For additional information, refer to the “Using Look-Up Tables as Shift Registers (SRL16)” chapter in [UG331](#).

It is possible to program each SLICEM LUT as a 16-bit shift register (see [Figure 28](#)). Used in this way, each LUT can delay serial data anywhere from 1 to 16 clock cycles without using any of the dedicated flip-flops. The resulting programmable delays can be used to balance the timing of data pipelines.

The SLICEM LUTs cascade from the G-LUT to the F-LUT through the DIFMUX (see [Figure 15](#)). SHIFTIN and SHIFTOUT lines cascade a SLICEM to the SLICEM below to form larger shift registers. The four SLICEM LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. It is also possible to combine shift registers across more than one CLB.

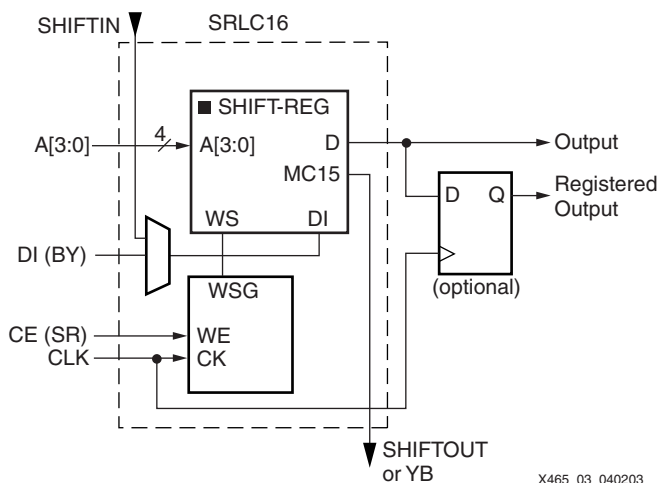
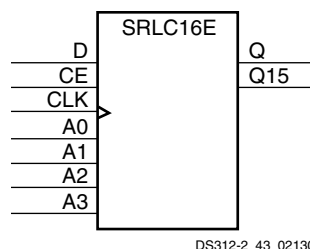


Figure 28: Logic Cell SRL16 Structure

Each shift register provides a shift output MC15 for the last bit in each LUT, in addition to providing addressable access to any bit in the shift register through the normal D output. The address inputs A[3:0] are the same as the distributed RAM address lines, which come from the LUT inputs F[4:1] or G[4:1]. At the end of the shift register, the CLB flip-flop can be used to provide one more shift delay for the addressable bit.

The shift register element is known as the SRL16 (Shift Register LUT 16-bit), with a ‘C’ added to signify a cascade ability (Q15 output) and ‘E’ to indicate a Clock Enable. See [Figure 29](#) for an example of the SRLC16E component.



DS312-2_43_021305

Figure 29: SRL16 Shift Register Component with Cascade and Clock Enable

The functionality of the shift register is shown in [Table 20](#). The SRL16 shifts on the rising edge of the clock input when the Clock Enable control is High. This shift register cannot be initialized either during configuration or during operation except by shifting data into it. The clock enable and clock inputs are shared between the two LUTs in a SLICEM. The clock enable input is automatically kept active if unused.

Table 20: SRL16 Shift Register Function

Inputs				Outputs	
Am	CLK	CE	D	Q	Q15
Am	X	0	X	Q[Am]	Q[15]
Am	↑	1	D	Q[Am-1]	Q[15]

Notes:

1. m = 0, 1, 2, 3.

Table 59: Byte-Wide Peripheral Interface (BPI) Connections (Cont'd)

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
DONE	Open-drain bidirectional I/O	FPGA Configuration Done. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA is successfully configured.
PROG_B	Input	Program FPGA. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 k Ω pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to Flash PROM pins.

Voltage Compatibility

Ⓥ The FPGA's parallel Flash interface signals are within I/O Banks 1 and 2. The majority of parallel Flash PROMs use a single 3.3V supply voltage. Consequently, in most cases, the FPGA's VCCO_1 and VCCO_2 supply voltages must also be 3.3V to match the parallel Flash PROM. There are some 1.8V parallel Flash PROMs available and the FPGA interfaces with these devices if the VCCO_1 and VCCO_2 supplies are also 1.8V.

Power-On Precautions if PROM Supply is Last in Sequence

Like SPI Flash PROMs, parallel Flash PROMs typically require some amount of internal initialization time when the supply voltage reaches its minimum value.

The PROM supply voltage also connects to the FPGA's VCCO_2 supply input. In many systems, the PROM supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the PROM supply is last in the sequence, a potential race occurs between the FPGA and the parallel Flash PROM. See

[Power-On Precautions if 3.3V Supply is Last in Sequence](#) for a similar description of the issue for SPI Flash PROMs.

Supported Parallel NOR Flash PROM Densities

[Table 60](#) indicates the smallest usable parallel Flash PROM to program a single Spartan-3E FPGA. Parallel Flash density is specified in bits but addressed as bytes. The FPGA presents up to 24 address lines during configuration but not all are required for single FPGA applications. [Table 60](#) shows the minimum required number of address lines between the FPGA and parallel Flash PROM. The actual number of address line required depends on the density of the attached parallel Flash PROM.

A multiple-FPGA daisy-chained application requires a parallel Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density parallel Flash PROM to hold additional data beyond just FPGA configuration data. For example, the parallel Flash PROM can also contain the application code for a MicroBlaze RISC processor core implemented within the Spartan-3E FPGA. After configuration, the MicroBlaze processor can execute directly from external Flash or can copy the code to other, faster system memory before executing the code.

Table 60: Number of Bits to Program a Spartan-3E FPGA and Smallest Parallel Flash PROM

Spartan-3E FPGA	Uncompressed File Sizes (bits)	Smallest Usable Parallel Flash PROM	Minimum Required Address Lines
XC3S100E	581,344	1 Mbit	A[16:0]
XC3S250E	1,353,728	2 Mbit	A[17:0]
XC3S500E	2,270,208	4 Mbit	A[18:0]
XC3S1200E	3,841,184	4 Mbit	A[18:0]
XC3S1600E	5,969,696	8 Mbit	A[19:0]

Table 65: Slave Parallel Mode Connections (Cont'd)

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	Initialization Indicator. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 k Ω pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	FPGA Configuration Done. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	Program FPGA. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 k Ω pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See [XAPP453: The 3.3V Configuration of Spartan-3 FPGAs](#) for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in [Figure 62](#) is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting its chip-select output, CSO_B.

Maximum Bitstream Size for Daisy-Chains

The maximum bitstream length supported by Spartan-3E FPGAs in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 720 XC3S1600E FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.

Configuration Sequence

For additional information including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in [UG332](#).

The Spartan-3E configuration process is three-stage process that begins after the FPGA powers on (a POR event) or after the PROG_B input is asserted. Power-On Reset (POR) occurs after the V_{CCINT}, V_{CCAUX}, and the V_{CCO} Bank 2 supplies reach their respective input threshold levels. After either a POR or PROG_B event, the three-stage configuration process begins.

1. The FPGA clears (initializes) the internal configuration memory.
2. Configuration data is loaded into the internal memory.
3. The user-application is activated by a start-up process.

[Figure 66](#) is a generalized block diagram of the Spartan-3E configuration logic, showing the interaction of different device inputs and Bitstream Generator (BitGen) options. A flow diagram for the configuration sequence of the Serial and Parallel modes appears in [Figure 66](#). [Figure 67](#) shows the Boundary-Scan or JTAG configuration sequence.

Initialization

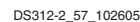
Configuration automatically begins after power-on or after asserting the FPGA PROG_B pin, unless delayed using the FPGA's INIT_B pin. The FPGA holds the open-drain INIT_B signal Low while it clears its internal configuration memory. Externally holding the INIT_B pin Low forces the configuration sequencer to wait until INIT_B again goes High.

The FPGA signals when the memory-clearing phase is complete by releasing the open-drain INIT_B pin, allowing the pin to go High via the external pull-up resistor to V_{CCO_2}.

Loading Configuration Data

After initialization, configuration data is written to the FPGA's internal memory. The FPGA holds the Global Set/Reset (GSR) signal active throughout configuration, holding all FPGA flip-flops in a reset state. The FPGA signals when the entire configuration process completes by releasing the DONE pin, allowing it to go High.

The FPGA configuration sequence can also be initiated by asserting PROG_B. Once released, the FPGA begins clearing its internal configuration memory, and progresses through the remainder of the configuration process.



DS312 (4.0) October 29, 2012
Product Specification

Table 93: Timing for the IOB Three-State Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T _{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.49	1.71	ns
T _{IOCKON} ⁽²⁾	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.70	3.10	ns
Asynchronous Output Enable/Disable Times						
T _{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3E primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	8.52	9.79	ns
Set/Reset Times						
T _{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	2.11	2.43	ns
T _{IOSRON} ⁽²⁾	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.32	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 95](#) and are based on the operating conditions set forth in [Table 77](#) and [Table 80](#).
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from [Table 94](#).
3. For minimum delays use the values reported by the Timing Analyzer.

Table 94: Output Timing Adjustments for IOB

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTTL	Slow	2 mA	5.20	5.41	ns
		4 mA	2.32	2.41	ns
		6 mA	1.83	1.90	ns
		8 mA	0.64	0.67	ns
		12 mA	0.68	0.70	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.80	5.00	ns
		4 mA	1.88	1.96	ns
		6 mA	1.39	1.45	ns
		8 mA	0.32	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVC MOS33	Slow	2 mA	5.08	5.29	ns
		4 mA	1.82	1.89	ns
		6 mA	1.00	1.04	ns
		8 mA	0.66	0.69	ns
		12 mA	0.40	0.42	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.68	4.87	ns
		4 mA	1.46	1.52	ns
		6 mA	0.38	0.39	ns
		8 mA	0.33	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVC MOS25	Slow	2 mA	4.04	4.21	ns
		4 mA	2.17	2.26	ns
		6 mA	1.46	1.52	ns
		8 mA	1.04	1.08	ns
		12 mA	0.65	0.68	ns
	Fast	2 mA	3.53	3.67	ns
		4 mA	1.65	1.72	ns
		6 mA	0.44	0.46	ns
		8 mA	0.20	0.21	ns
		12 mA	0	0	ns

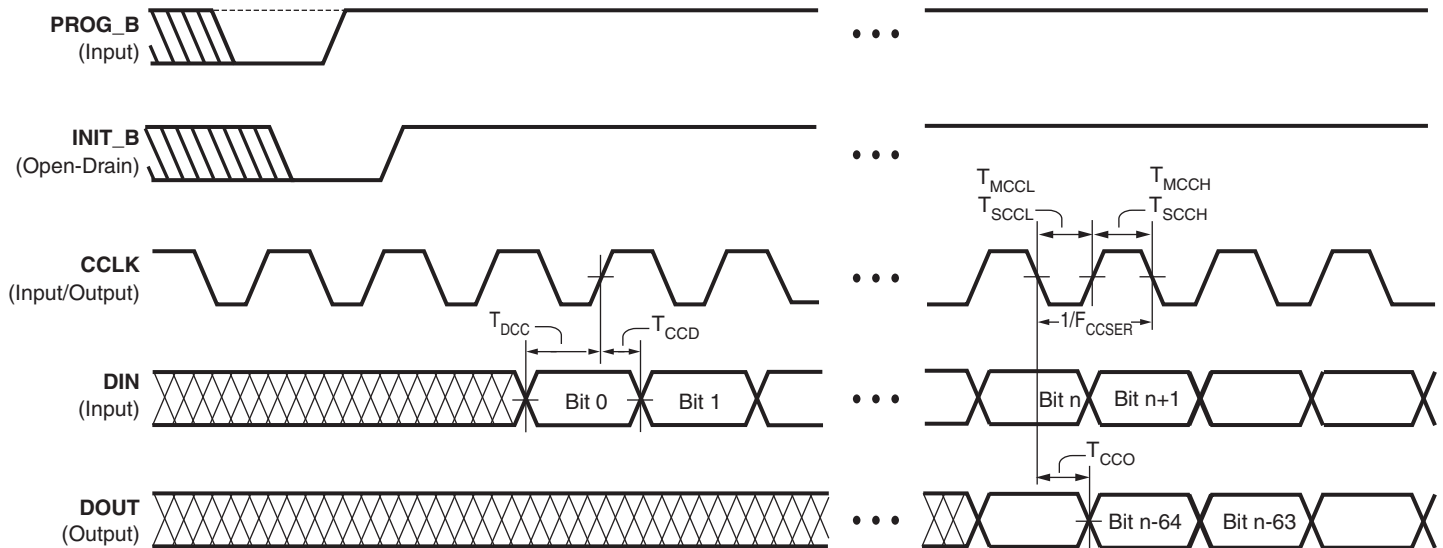
Table 94: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	5.03	5.24	ns
		4 mA	3.08	3.21	ns
		6 mA	2.39	2.49	ns
		8 mA	1.83	1.90	ns
	Fast	2 mA	3.98	4.15	ns
		4 mA	2.04	2.13	ns
		6 mA	1.09	1.14	ns
		8 mA	0.72	0.75	ns
LVCMOS15	Slow	2 mA	4.49	4.68	ns
		4 mA	3.81	3.97	ns
		6 mA	2.99	3.11	ns
	Fast	2 mA	3.25	3.38	ns
		4 mA	2.59	2.70	ns
		6 mA	1.47	1.53	ns
LVCMOS12	Slow	2 mA	6.36	6.63	ns
	Fast	2 mA	4.26	4.44	ns
HSTL_I_18			0.33	0.34	ns
HSTL_III_18			0.53	0.55	ns
PCI33_3			0.44	0.46	ns
PCI66_3			0.44	0.46	ns
SSTL18_I			0.24	0.25	ns
SSTL2_I			-0.20	-0.20	ns
Differential Standards					
LVDS_25			-0.55	-0.55	ns
BLVDS_25			0.04	0.04	ns
MINI_LVDS_25			-0.56	-0.56	ns
LVPECL_25			Input Only		ns
RSDS_25			-0.48	-0.48	ns
DIFF_HSTL_I_18			0.42	0.42	ns
DIFF_HSTL_III_18			0.53	0.55	ns
DIFF_SSTL18_I			0.40	0.40	ns
DIFF_SSTL2_I			0.44	0.44	ns

Notes:

- The numbers in this table are tested using the methodology presented in [Table 95](#) and are based on the operating conditions set forth in [Table 77](#), [Table 80](#), and [Table 82](#).
- These adjustments are used to convert output- and three-state-path times originally specified for the LVC MOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Master Serial and Slave Serial Mode Timing



DS312-3_05_103105

Figure 74: Waveforms for Master Serial and Slave Serial Configuration

Table 116: Timing for the Master Serial and Slave Serial Configuration Modes

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T _{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10.0	ns
Setup Times						
T _{DCC}	The time from the setup of data at the DIN pin to the active edge of the CCLK pin		Both	11.0	-	ns
Hold Times						
T _{CCD}	The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T _{CCH}	High pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
T _{CCL}	Low pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
F _{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	66 ⁽²⁾	MHz
		With bitstream compression		0	20	MHz

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 77.
- For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Table 133: CP132 Package Pinout (Cont'd)

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
GND	GND	GND	C10	GND
GND	GND	GND	E3	GND
GND	GND	GND	E14	GND
GND	GND	GND	G2	GND
GND	GND	GND	H14	GND
GND	GND	GND	J1	GND
GND	GND	GND	K12	GND
GND	GND	GND	M3	GND
GND	GND	GND	M7	GND
GND	GND	GND	P5	GND
GND	N.C. (GND)	GND	P10	GND
GND	GND	GND	P14	GND
VCCAUX	DONE	DONE	P13	CONFIG
VCCAUX	PROG_B	PROG_B	A1	CONFIG
VCCAUX	TCK	TCK	B13	JTAG
VCCAUX	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	A14	JTAG
VCCAUX	TMS	TMS	B14	JTAG
VCCAUX	VCCAUX	VCCAUX	A5	VCCAUX
VCCAUX	VCCAUX	VCCAUX	E12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P9	VCCAUX
VCCINT	VCCINT	VCCINT	A11	VCCINT
VCCINT	VCCINT	VCCINT	D3	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	D14	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	K2	VCCINT
VCCINT	VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	VCCINT	P2	VCCINT

TQ144: 144-lead Thin Quad Flat Package

The XC3S100E and the XC3S250E FPGAs are available in the 144-lead thin quad flat package, TQ144. Both devices share a common footprint for this package as shown in [Table 137](#) and [Figure 82](#).

[Table 137](#) lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The TQ144 package only supports 20 address output pins in the Byte-wide Peripheral Interface (BPI) configuration mode. In larger packages, there are 24 BPI address outputs.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 137: TQ144 Package Pinout

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
0	IO	IO	P132	I/O
0	IO/VREF_0	IO/VREF_0	P124	VREF
0	IO_L01N_0	IO_L01N_0	P113	I/O
0	IO_L01P_0	IO_L01P_0	P112	I/O
0	IO_L02N_0	IO_L02N_0	P117	I/O
0	IO_L02P_0	IO_L02P_0	P116	I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	P123	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	P122	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	P126	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	P125	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	P131	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	P130	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	P135	VREF
0	IO_L08P_0	IO_L08P_0	P134	I/O
0	IO_L09N_0	IO_L09N_0	P140	I/O
0	IO_L09P_0	IO_L09P_0	P139	I/O
0	IO_L10N_0/HSWAP	IO_L10N_0/HSWAP	P143	DUAL
0	IO_L10P_0	IO_L10P_0	P142	I/O
0	IP	IP	P111	INPUT
0	IP	IP	P114	INPUT
0	IP	IP	P136	INPUT
0	IP	IP	P141	INPUT
0	IP_L03N_0	IP_L03N_0	P120	INPUT
0	IP_L03P_0	IP_L03P_0	P119	INPUT
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	P129	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	P128	GCLK
0	VCCO_0	VCCO_0	P121	VCCO
0	VCCO_0	VCCO_0	P138	VCCO
1	IO/A0	IO/A0	P98	DUAL
1	IO/VREF_1	IO/VREF_1	P83	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	P75	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	P74	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	P77	DUAL

Table 141: PQ208 Package Pinout (Cont'd)

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
1	IO_L15N_1/LDC0	P151	DUAL
1	IO_L15P_1/HDC	P150	DUAL
1	IO_L16N_1/LDC2	P153	DUAL
1	IO_L16P_1/LDC1	P152	DUAL
1	IP	P110	INPUT
1	IP	P118	INPUT
1	IP	P124	INPUT
1	IP	P130	INPUT
1	IP	P142	INPUT
1	IP	P148	INPUT
1	IP	P154	INPUT
1	IP/VREF_1	P136	VREF
1	VCCO_1	P114	VCCO
1	VCCO_1	P125	VCCO
1	VCCO_1	P143	VCCO
2	IO/D5	P76	DUAL
2	IO/M1	P84	DUAL
2	IO/VREF_2	P98	VREF
2	IO_L01N_2/INIT_B	P56	DUAL
2	IO_L01P_2/CSO_B	P55	DUAL
2	IO_L03N_2/MOSI/CSI_B	P61	DUAL
2	IO_L03P_2/DOUT/BUSY	P60	DUAL
2	IO_L04N_2	P63	I/O
2	IO_L04P_2	P62	I/O
2	IO_L05N_2	P65	I/O
2	IO_L05P_2	P64	I/O
2	IO_L06N_2	P69	I/O
2	IO_L06P_2	P68	I/O
2	IO_L08N_2/D6/GCLK13	P75	DUAL/GCLK
2	IO_L08P_2/D7/GCLK12	P74	DUAL/GCLK
2	IO_L09N_2/D3/GCLK15	P78	DUAL/GCLK
2	IO_L09P_2/D4/GCLK14	P77	DUAL/GCLK
2	IO_L11N_2/D1/GCLK3	P83	DUAL/GCLK
2	IO_L11P_2/D2/GCLK2	P82	DUAL/GCLK
2	IO_L12N_2/DIN/D0	P87	DUAL
2	IO_L12P_2/M0	P86	DUAL
2	IO_L13N_2	P90	I/O
2	IO_L13P_2	P89	I/O
2	IO_L14N_2/A22	P94	DUAL
2	IO_L14P_2/A23	P93	DUAL
2	IO_L15N_2/A20	P97	DUAL
2	IO_L15P_2/A21	P96	DUAL
2	IO_L16N_2/VS1/A18	P100	DUAL

Table 141: PQ208 Package Pinout (Cont'd)

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
2	IO_L16P_2/VS2/A19	P99	DUAL
2	IO_L17N_2/CCLK	P103	DUAL
2	IO_L17P_2/VS0/A17	P102	DUAL
2	IP	P54	INPUT
2	IP	P91	INPUT
2	IP	P101	INPUT
2	IP_L02N_2	P58	INPUT
2	IP_L02P_2	P57	INPUT
2	IP_L07N_2/VREF_2	P72	VREF
2	IP_L07P_2	P71	INPUT
2	IP_L10N_2/M2/GCLK1	P81	DUAL/GCLK
2	IP_L10P_2/RDWR_B/ GCLK0	P80	DUAL/GCLK
2	VCCO_2	P59	VCCO
2	VCCO_2	P73	VCCO
2	VCCO_2	P88	VCCO
3	IO/VREF_3	P45	VREF
3	IO_L01N_3	P3	I/O
3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	P4	I/O
3	IO_L03N_3	P9	I/O
3	IO_L03P_3	P8	I/O
3	IO_L04N_3	P12	I/O
3	IO_L04P_3	P11	I/O
3	IO_L05N_3	P16	I/O
3	IO_L05P_3	P15	I/O
3	IO_L06N_3	P19	I/O
3	IO_L06P_3	P18	I/O
3	IO_L07N_3/LHCLK1	P23	LHCLK
3	IO_L07P_3/LHCLK0	P22	LHCLK
3	IO_L08N_3/LHCLK3	P25	LHCLK
3	IO_L08P_3/LHCLK2	P24	LHCLK
3	IO_L09N_3/LHCLK5	P29	LHCLK
3	IO_L09P_3/LHCLK4	P28	LHCLK
3	IO_L10N_3/LHCLK7	P31	LHCLK
3	IO_L10P_3/LHCLK6	P30	LHCLK
3	IO_L11N_3	P34	I/O
3	IO_L11P_3	P33	I/O
3	IO_L12N_3	P36	I/O
3	IO_L12P_3	P35	I/O
3	IO_L13N_3	P40	I/O
3	IO_L13P_3	P39	I/O
3	IO_L14N_3	P42	I/O

Table 148: FG320 Package Pinout (Cont'd)

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	T12	I/O
2	N.C. (◆)	IO_L21N_2	IO_L21N_2	P12	500E: N.C. 1200E: I/O 1600E: I/O
2	N.C. (◆)	IO_L21P_2	IO_L21P_2	N12	500E: N.C. 1200E: I/O 1600E: I/O
2	IO_L22N_2/A22	IO_L22N_2/A22	IO_L22N_2/A22	R13	DUAL
2	IO_L22P_2/A23	IO_L22P_2/A23	IO_L22P_2/A23	P13	DUAL
2	IO_L24N_2/A20	IO_L24N_2/A20	IO_L24N_2/A20	R14	DUAL
2	IO_L24P_2/A21	IO_L24P_2/A21	IO_L24P_2/A21	T14	DUAL
2	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	U15	DUAL
2	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	V15	DUAL
2	IO_L26N_2/CCLK	IO_L26N_2/CCLK	IO_L26N_2/CCLK	U16	DUAL
2	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	T16	DUAL
2	IP	IP	IP	V2	INPUT
2	IP	IP	IP	V16	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	V3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	V4	INPUT
2	IP_L08N_2	IP_L08N_2	IP_L08N_2	R7	INPUT
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	T7	INPUT
2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	V8	VREF
2	IP_L11P_2	IP_L11P_2	IP_L11P_2	U8	INPUT
2	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	T10	DUAL/GCLK
2	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	U10	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	U11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	T11	INPUT
2	IP_L23N_2	IP_L23N_2	IP_L23N_2	U14	INPUT
2	IP_L23P_2	IP_L23P_2	IP_L23P_2	V14	INPUT
2	VCCO_2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	VCCO_2	M11	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T6	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T13	VCCO
2	VCCO_2	VCCO_2	VCCO_2	V10	VCCO
3	N.C. (◆)	IO	IO	D4	500E: N.C. 1200E: I/O 1600E: I/O
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	C2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	C1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	D1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E2	I/O

User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 149: User I/Os Per Bank for XC3S500E in the FG320 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF ⁽¹⁾	CLK ⁽²⁾
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0 ⁽²⁾
Bottom	2	58	17	13	24	4	0 ⁽²⁾
Left	3	58	34	11	0	5	8
TOTAL		232	102	48	46	20	16

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 150: User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF ⁽¹⁾	CLK ⁽²⁾
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0 ⁽²⁾
Bottom	2	63	23	11	24	5	0 ⁽²⁾
Left	3	63	38	12	0	5	8
TOTAL		250	120	47	46	21	16

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 155: User I/Os Per Bank for the XC3S1600E in the FG484 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF ⁽¹⁾	CLK ⁽²⁾
Top	0	94	56	22	1	7	8
Right	1	94	50	16	21	7	0 ⁽²⁾
Bottom	2	94	45	18	24	7	0 ⁽²⁾
Left	3	94	63	16	0	7	8
TOTAL		376	214	72	46	28	16

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The XC3S1600E FPGA is the only Spartan-3E device offered in the FG484 package.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in the CP132 package to Table 129 . Corrected number of differential I/O pairs on CP132. Added pinout and footprint information for the CP132, FG400, and FG484 packages. Removed IRDY and TRDY pins from the VQ100, TQ144, and PQ208 packages.
11/23/05	2.0	Corrected title of Table 153 . Updated differential pair numbering for some pins in Bank 0 of the FG400 package, affecting Table 152 and Figure 87 . Pin functionality and ball assignment were not affected. Added Package Thermal Characteristics section. Added package mass values to Table 125 .
03/22/06	3.0	Included I/O pins, not just input-only pins under the VREF description in Table 124 . Clarified that some global clock inputs are Input-only pins in Table 124 . Added information on the XC3S100E in the CP132 package, affecting Table 129 , Table 130 , Table 133 , Table 134 , Table 136 , and Figure 81 . Ball A12 on the XC3S1600E in the FG320 package a full I/O pin, not an Input-only pin. Corrected the I/O counts for the XC3S1600E in the FG320 package, affecting Table 129 , Table 150 , Table 151 , and Figure 86 . Corrected pin type for XC3S1600E balls N14 and N15 in Table 148 .
05/19/06	3.1	Minor text edits.
11/09/06	3.4	Added package thermal data for the XC3S100E in the CP132 package to Table 130 . Corrected pin migration arrows for balls E17 and F4 between the XC3S500E and XC3S1600E in Table 151 . Promoted Module 4 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Minor formatting changes.
05/29/07	3.6	Corrected 'Lxx' to 'Lxy' in Table 124 . Noted that some GCLK and VREF pins are on INPUT pins in Table 124 and Table 129 . Added link before Table 127 to Material Declaration Data Sheets.
04/18/08	3.7	Added XC3S500E VQG100 package. Added Material Declaration Data Sheet links in Table 127 . Updated Thermal Characteristics in Table 130 . Updated links.
08/26/09	3.8	Minor typographical updates.
10/29/12	4.0	Added Notice of Disclaimer . This product is not recommended for new designs. Updated the XC3S250E-FT256 in Table 129 .

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