AMD Xilinx - XC3S500E-5PQ208C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1164
Number of Logic Elements/Cells	10476
Total RAM Bits	368640
Number of I/O	158
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s500e-5pq208c

Carry and Arithmetic Logic

For additional information, refer to the “Using Carry and Arithmetic Logic” chapter in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry logic is automatically used for most arithmetic functions in a design. The gates and multiplexers of the carry and arithmetic logic can also be used for general-purpose logic, including simple wide Boolean functions.

The carry chain enters the slice as CIN and exits as COUT, controlled by several multiplexers. The carry chain connects directly from one CLB to the CLB above. The carry chain can be initialized at any point from the BX (or BY) inputs.

The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). These gates work in conjunction with the LUTs to implement efficient arithmetic functions, including counters and multipliers, typically at two bits per slice. See Figure 22 and Table 14.

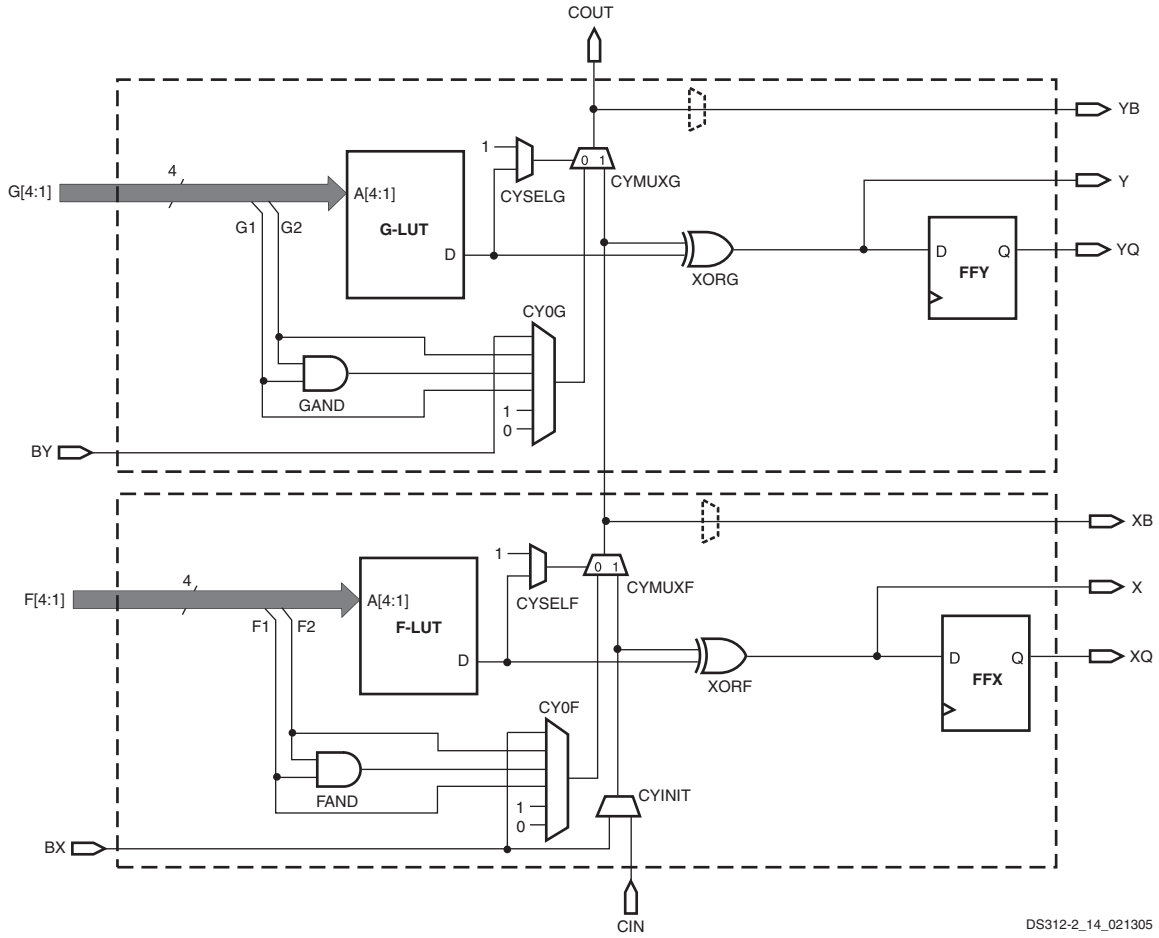


Figure 22: **Carry Logic**

Table 14: **Carry Logic Functions**

Function	Description
CYINIT	Initializes carry chain for a slice. Fixed selection of: · CIN carry input from the slice below · BX input
CY0F	Carry generation for bottom half of slice. Fixed selection of: · F1 or F2 inputs to the LUT (both equal 1 when a carry is to be generated) · FAND gate for multiplication · BX input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function

Initialization

The CLB storage elements are initialized at power-up, during configuration, by the global GSR signal, and by the individual SR or REV inputs to the CLB. The storage elements can also be re-initialized using the GSR input on the STARTUP_SPARTAN3E primitive. See Global Controls (STARTUP_SPARTAN3E).

Table 17: **Slice Storage Element Initialization**

Signal	Description
SR	Set/Reset input. Forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. For each slice, set and reset can be set to be synchronous or asynchronous.
REV	Reverse of Set/Reset input. A second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition if both are active. Same synchronous/asynchronous setting as for SR.
GSR	Global Set/Reset. GSR defaults to active High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN3E element. The initial state after configuration or GSR is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

Distributed RAM

For additional information, refer to the “Using Look-Up Tables as Distributed RAM” chapter in UG331.

The LUTs in the SLICEM can be programmed as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One SLICEM LUT stores 16 bits (RAM16). The four LUT inputs F[4:1] or G[4:1] become the address lines labeled A[4:1] in the device model and A[3:0] in the design components, providing a 16x1 configuration in one LUT. Multiple SLICEM LUTs can be combined in various ways to store larger amounts of data, including 16x4, 32x2, or 64x1 configurations in one CLB. The fifth and sixth address lines required for the 32-deep and 64-deep configurations, respectively, are implemented using the BX and BY inputs, which connect to the write enable logic for writing and the F5MUX and F6MUX for reading.

Writing to distributed RAM is always synchronous to the SLICEM clock (WCLK for distributed RAM) and enabled by the SLICEM SR input which functions as the active-High Write Enable (WE). The read operation is asynchronous, and, therefore, during a write, the output initially reflects the old data at the address being written.

The distributed RAM outputs can be captured using the flip-flops within the SLICEM element. The WE write-enable control for the RAM and the CE clock-enable control for the flip-flop are independent, but the WCLK and CLK clock inputs are shared. Because the RAM read operation is asynchronous, the output data always reflects the currently addressed RAM location.

A dual-port option combines two LUTs so that memory access is possible from two independent data lines. The same data is written to both 16x1 memories but they have independent read address lines and outputs. The dual-port function is implemented by cascading the G-LUT address lines, which are used for both read and write, to the F-LUT write address lines (WF[4:1] in Figure 15), and by cascading the G-LUT data input D1 through the DIF_MUX in Figure 15 and to the D1 input on the F-LUT. One CLB provides a 16x1 dual-port memory as shown in Figure 26.

Any write operation on the D input and any read operation on the SPO output can occur simultaneously with and independently from a read operation on the second read-only port, DPO.

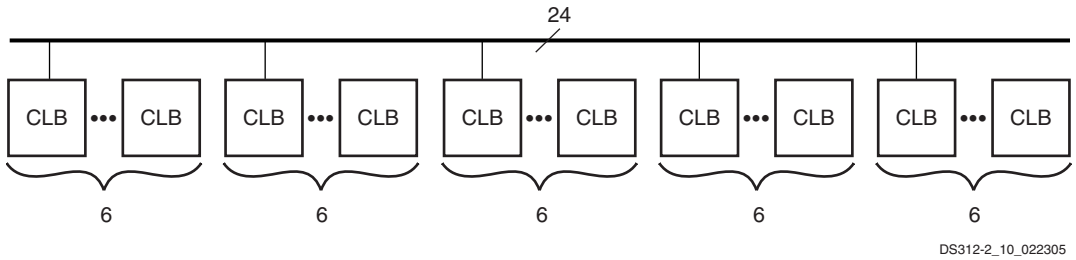
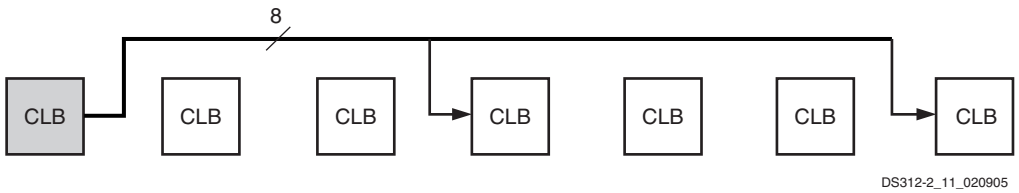
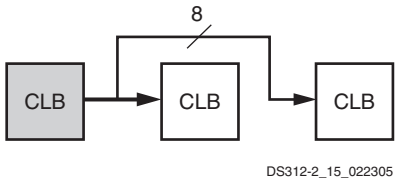
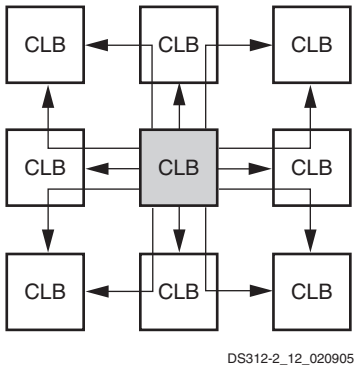
Horizontal and Vertical Long Lines (horizontal channel shown as an example)	
Horizontal and Vertical Hex Lines (horizontal channel shown as an example)	
Horizontal and Vertical Double Lines (horizontal channel shown as an example)	
Direct Connections	

Figure 50: **Interconnect Types between Two Adjacent Interconnect Tiles**

The four types of general-purpose interconnect available in each channel, shown in Figure 50, are described below.

Long Lines

Each set of 24 long line signals spans the die both horizontally and vertically and connects to one out of every six interconnect tiles. At any tile, four of the long lines drive or receive signals from a switch matrix. Because of their low capacitance, these lines are well-suited for carrying high-frequency signals with minimal loading effects (e.g. skew). If all global clock lines are already committed and additional clock signals remain to be assigned, long lines serve as a good alternative.

Hex Lines

Each set of eight hex lines are connected to one out of every three tiles, both horizontally and vertically. Thirty-two hex lines are available between any given interconnect tile. Hex lines are only driven from one end of the route.

Double Lines

Each set of eight double lines are connected to every other tile, both horizontally and vertically. in all four directions. Thirty-two double lines available between any given interconnect tile. Double lines are more connections and more flexibility, compared to long line and hex lines.

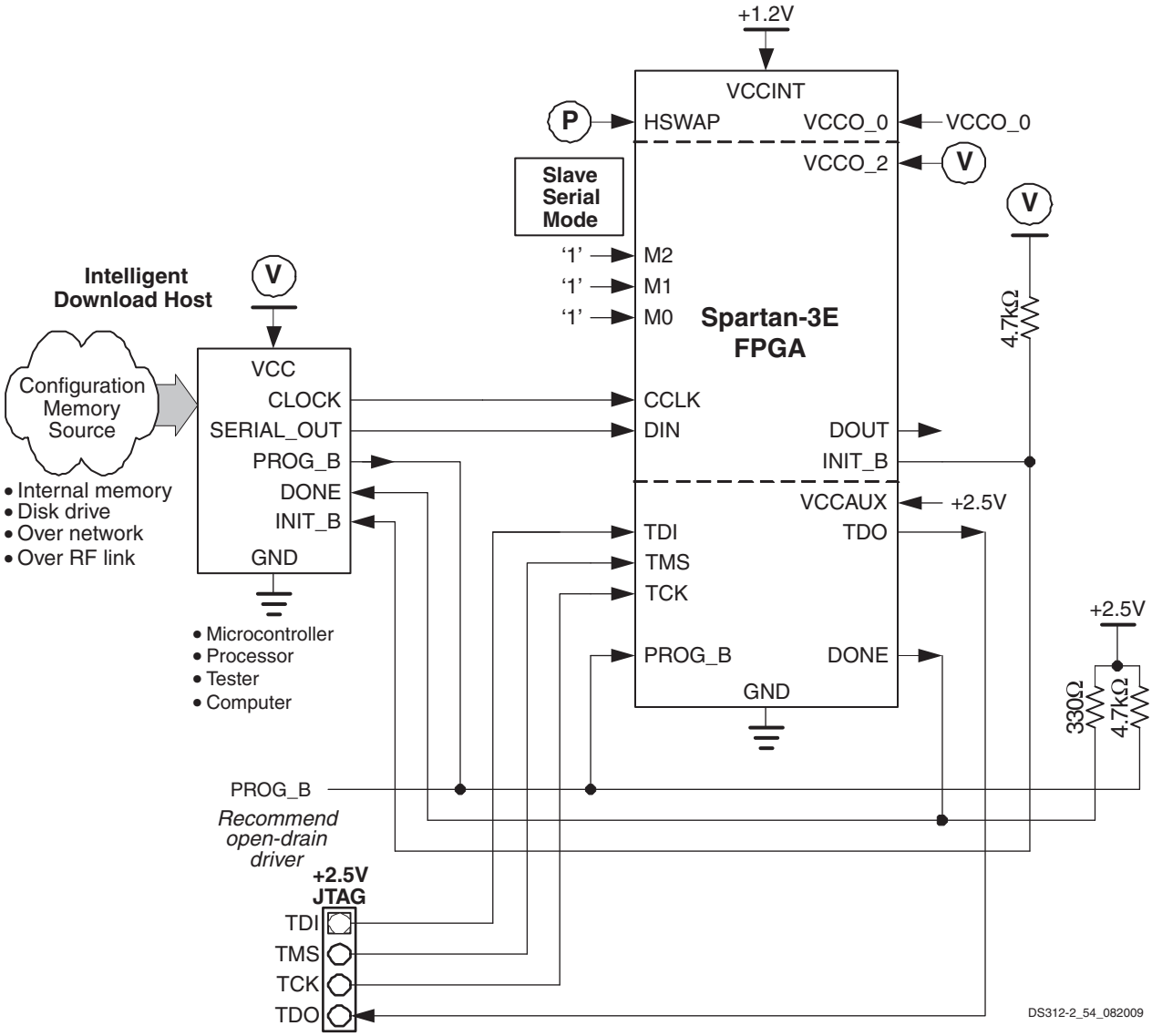


Figure 63: **Slave Serial Configuration**

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

Voltage Compatibility

(V) Most Slave Serial interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 3.3V, 2.5V, or 1.8V to match the requirements of the external host, ideally 2.5V. Using 3.3V or 1.8V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 64. Use Slave Serial mode (M[2:0] = <1:1:1>) for all FPGAs in the daisy-chain. After the lead FPGA is filled with its configuration data, the lead

FPGA passes configuration data via its DOUT output pin to the next FPGA on the falling CCLK edge.

Table 66: **Slave Serial Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-up during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 1, M1 = 1, M0 = 1 Sampled when INIT_B goes High.	User I/O
DIN	Input	**Data Input**.	Serial data provided by host. FPGA captures data on rising CCLK edge.	User I/O
CCLK	Input	**Configuration Clock**. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	External clock.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs including some with integrated three-rail regulators specifically designed for Spartan-3 and Spartan-3E FPGAs. The Xilinx Power Corner website provides links to vendor solution guides and Xilinx power estimation and analysis tools.

Power Distribution System (PDS) Design and Decoupling/Bypass Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, but especially so for high performance applications, greater than 100 MHz. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, please review XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

Power-On Behavior

For additional power-on behavior information, including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in UG332.

Spartan-3E FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supplies reach their respective input threshold levels (see Table 74 in Module 3). After all three supplies reach their respective thresholds, the POR reset is released and the FPGA begins its configuration process.

Supply Sequencing

Because the three FPGA supply inputs must be valid to release the POR reset and can be supplied in any order, there are no FPGA-specific voltage sequencing requirements. Applying the FPGA's V_{CCAUX} supply before the V_{CCINT} supply uses the least I_{CCINT} current.

Although the FPGA has no specific voltage sequence requirements, be sure to consider any potential sequencing requirement of the configuration device attached to the FPGA, such as an SPI serial Flash PROM, a parallel NOR Flash PROM, or a microcontroller. For example, Flash PROMs have a minimum time requirement before the PROM can be selected and this must be considered if the 3.3V supply is the last in the sequence. See Power-On Precautions if 3.3V Supply is Last in Sequence for more details.

When all three supplies are valid, the minimum current required to power-on the FPGA equals the worst-case quiescent current, specified in Table 79. Spartan-3E FPGAs do not require Power-On Surge (POS) current to successfully configure.

Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}

If the V_{CCINT} supply is applied before the V_{CCAUX} supply, the FPGA might draw a surplus I_{CCINT} current in addition to the I_{CCINT} quiescent current levels specified in Table 79, page 118. The momentary additional I_{CCINT} surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the V_{CCAUX} supply is applied, and, in response, the FPGA's I_{CCINT} quiescent current demand drops to the levels specified in Table 79. The FPGA does not use or require the surplus current to successfully power-on and configure. If applying V_{CCINT} before V_{CCAUX}, ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents, as specified in Table 76.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, the current device configuration must be cleared using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold (Table 74).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_2 supply after configuration. Consequently, dropping the VCCO_2 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3E FPGA circuitry is fully static and does not employ internal charge pumps.

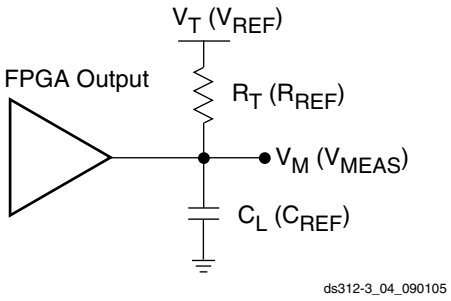
The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 95 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 72. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 72: **Output Test Setup**

Table 95: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
Differential							
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
Single-Ended Standards							
LVTTL	Slow	2	34	20	19	52	60
		4	17	10	10	26	41
		6	17	10	7	26	29
		8	8	6	6	13	22
		12	8	6	5	13	13
		16	5	5	5	6	11
	Fast	2	17	17	17	26	34
		4	9	9	9	13	20
		6	7	7	7	13	15
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	5	5	5	5	9
LVCMOS33	Slow	2	34	20	20	52	76
		4	17	10	10	26	46
		6	17	10	7	26	27
		8	8	6	6	13	20
		12	8	6	5	13	13
		16	5	5	5	6	10
	Fast	2	17	17	17	26	44
		4	8	8	8	13	26
		6	8	6	6	13	16
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	8	8	5	5	8
LVCMOS25	Slow	2	28	16	16	42	76
		4	13	10	10	19	46
		6	13	7	7	19	33
		8	6	6	6	9	24
		12	6	6	6	9	18
	Fast	2	17	16	16	26	42
		4	9	9	9	13	20
		6	9	7	7	13	15
		8	6	6	6	6	13
		12	5	5	5	6	11
LVCMOS18	Slow	2	19	11	8	29	64
		4	13	7	6	19	34
		6	6	5	5	9	22
		8	6	4	4	9	18
	Fast	2	13	8	8	19	36
		4	8	5	5	13	21
		6	4	4	4	6	13
		8	4	4	4	6	10

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
LVCMOS15	Slow	2	16	10	10	19	55
		4	8	7	7	9	31
		6	6	5	5	9	18
	Fast	2	9	9	9	13	25
		4	7	7	7	7	16
		6	5	5	5	5	13
LVCMOS12	Slow	2	17	11	11	16	55
	Fast	2	10	10	10	10	31
PCI33_3			8	8	8	16	16
PCI66_3			8	8	8	13	13
PCIX			7	7	7	11	11
HSTL_I_18			10	10	10	16	17
HSTL_III_18			10	10	10	16	16
SSTL18_I			9	9	9	15	15
SSTL2_I			12	12	12	18	18
Differential Standards (Number of I/O Pairs or Channels)							
LVDS_25			6	6	6	12	20
BLVDS_25			4	4	4	4	4
MINI_LVDS_25			6	6	6	12	20
LVPECL_25			Input Only				
RSDS_25			6	6	6	12	20
DIFF_HSTL_I_18			5	5	5	8	8
DIFF_HSTL_IIII_18			5	5	5	8	8
DIFF_SSTL18_I			4	4	4	7	7
DIFF_SSTL2_I			6	6	6	9	8

Notes:

1. The numbers in this table are recommendations that assume sound board layout practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per VCCO and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the VIL/VIH voltage limits for the respective I/O standard.
2. The PQ208 results are based on physical measurements of a PQ208 package soldered to a typical printed circuit board. All other results are based on worst-case simulation and an interpolation of the PQ208 physical results.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: Managing Ground Bounce in Large FPGAs for information on how to perform weighted average SSO calculations.

Block RAM Timing

Table 103: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.45	-	2.82	ns
Setup Times						
T_{BACK}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.33	-	0.38	-	ns
T_{BDCK}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	0.23	-	ns
T_{BECK}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.67	-	0.77	-	ns
T_{BWCK}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.09	-	1.26	-	ns
Hold Times						
T_{BCKA}	Hold time on the ADDR inputs after the active transition at the CLK input	0.12	-	0.14	-	ns
T_{BCKD}	Hold time on the DIN inputs after the active transition at the CLK input	0.12	-	0.13	-	ns
T_{BCKE}	Hold time on the EN input after the active transition at the CLK input	0	-	0	-	ns
T_{BCKW}	Hold time on the WE input after the active transition at the CLK input	0	-	0	-	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.39	-	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.39	-	1.59	-	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift-registers and circular buffers. Write-only or read-only performance is faster.	0	270	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Table 121: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5\,T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded int o the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

Table 122: **MultiBoot Trigger (MBT) Timing**

Symbol	Description	Minimum	Maximum	Units
T_{MBT}	MultiBoot Trigger (MBT) Low pulse width required to initiate MultiBoot reconfiguration	300	∞	ns

Notes:

1. MultiBoot re-configuration starts on the rising edge after MBT is Low for at least the prescribed minimum period.

IEEE 1149.1/1532 JTAG Test Access Port Timing

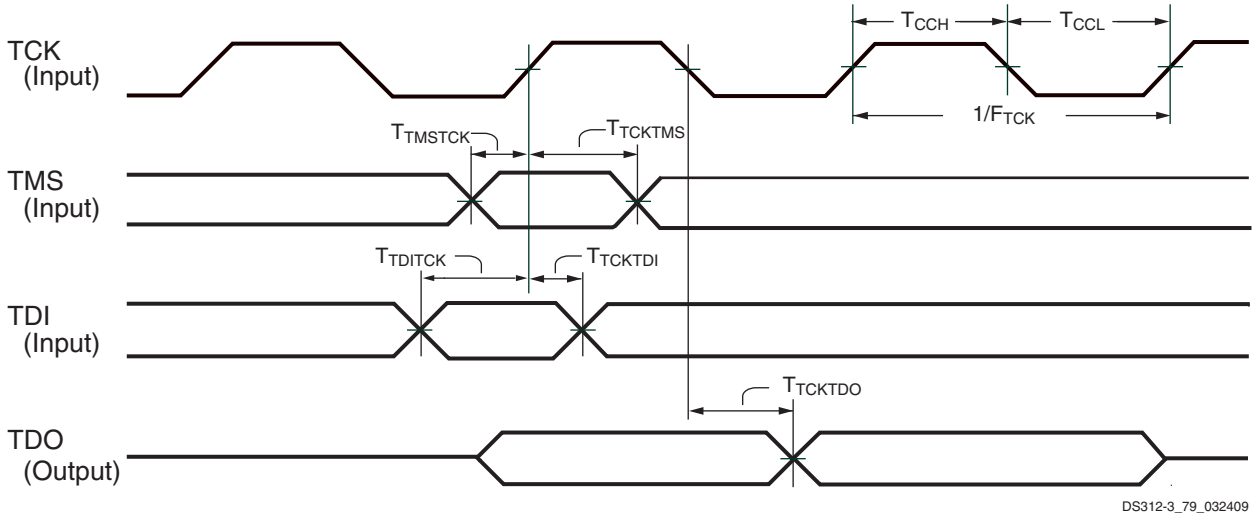


Figure 78: **JTAG Waveforms**

Table 123: **Timing for the JTAG Test Access Port**

Symbol	Description	All Speed Grades		Units
		Min	Max	
Clock-to-Output Times				
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns
Setup Times				
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	7.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	-	ns
Hold Times				
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T_{CCH}	The High pulse width at the TCK pin	5	-	ns
T_{CCL}	The Low pulse width at the TCK pin	5	-	ns
F_{TCK}	Frequency of the TCK signal	-	30	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

VQ100: 100-lead Very-thin Quad Flat Package

The XC3S100E, XC3S250E, and the XC3S500E devices are available in the 100-lead very-thin quad flat package, VQ100. All devices share a common footprint for this package as shown in Table 131 and Figure 80.

Table 131 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 package does not support the Byte-wide Peripheral Interface (BPI) configuration mode. Consequently, the VQ100 footprint has fewer DUAL-type pins than other packages.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 131 shows the pinout for production Spartan-3E FPGAs in the VQ100 package.

Table 131: **VQ100 Package Pinout**

Bank	XC3S100E XC3S250E XC3S500E Pin Name	VQ100 Pin Number	Type
0	IO	P92	I/O
0	IO_L01N_0	P79	I/O
0	IO_L01P_0	P78	I/O
0	IO_L02N_0/GCLK5	P84	GCLK
0	IO_L02P_0/GCLK4	P83	GCLK
0	IO_L03N_0/GCLK7	P86	GCLK
0	IO_L03P_0/GCLK6	P85	GCLK
0	IO_L05N_0/GCLK11	P91	GCLK
0	IO_L05P_0/GCLK10	P90	GCLK
0	IO_L06N_0/VREF_0	P95	VREF
0	IO_L06P_0	P94	I/O
0	IO_L07N_0/HSWAP	P99	DUAL
0	IO_L07P_0	P98	I/O
0	IP_L04N_0/GCLK9	P89	GCLK
0	IP_L04P_0/GCLK8	P88	GCLK
0	VCCO_0	P82	VCCO
0	VCCO_0	P97	VCCO
1	IO_L01N_1	P54	I/O
1	IO_L01P_1	P53	I/O
1	IO_L02N_1	P58	I/O
1	IO_L02P_1	P57	I/O
1	IO_L03N_1/RHCLK1	P61	RHCLK
1	IO_L03P_1/RHCLK0	P60	RHCLK
1	IO_L04N_1/RHCLK3	P63	RHCLK
1	IO_L04P_1/RHCLK2	P62	RHCLK
1	IO_L05N_1/RHCLK5	P66	RHCLK
1	IO_L05P_1/RHCLK4	P65	RHCLK
1	IO_L06N_1/RHCLK7	P68	RHCLK
1	IO_L06P_1/RHCLK6	P67	RHCLK
1	IO_L07N_1	P71	I/O
1	IO_L07P_1	P70	I/O
1	IP/VREF_1	P69	VREF
1	VCCO_1	P55	VCCO
1	VCCO_1	P73	VCCO
2	IO/D5	P34	DUAL
2	IO/M1	P42	DUAL
2	IO_L01N_2/INIT_B	P25	DUAL
2	IO_L01P_2/CSO_B	P24	DUAL
2	IO_L02N_2/MOSI/CSI_B	P27	DUAL
2	IO_L02P_2/DOUT/BUSY	P26	DUAL
2	IO_L03N_2/D6/GCLK13	P33	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	P32	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	P36	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	P35	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	P41	DUAL/GCLK
2	IO_L06P_2/D2/GCLK2	P40	DUAL/GCLK
2	IO_L07N_2/DIN/D0	P44	DUAL
2	IO_L07P_2/M0	P43	DUAL
2	IO_L08N_2/VS1	P48	DUAL
2	IO_L08P_2/VS2	P47	DUAL
2	IO_L09N_2/CCLK	P50	DUAL
2	IO_L09P_2/VS0	P49	DUAL
2	IP/VREF_2	P30	VREF
2	IP_L05N_2/M2/GCLK1	P39	DUAL/GCLK
2	IP_L05P_2/RDWR_B/ GCLK0	P38	DUAL/GCLK
2	VCCO_2	P31	VCCO
2	VCCO_2	P45	VCCO
3	IO_L01N_3	P3	I/O
3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	P5	VREF

TQ144: 144-lead Thin Quad Flat Package

The XC3S100E and the XC3S250E FPGAs are available in the 144-lead thin quad flat package, TQ144. Both devices share a common footprint for this package as shown in Table 137 and Figure 82.

Table 137 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The TQ144 package only supports 20 address output pins in the Byte-wide Peripheral Interface (BPI) configuration mode. In larger packages, there are 24 BPI address outputs.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 137: **TQ144 Package Pinout**

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
0	IO	IO	P132	I/O
0	IO/VREF_0	IO/VREF_0	P124	VREF
0	IO_L01N_0	IO_L01N_0	P113	I/O
0	IO_L01P_0	IO_L01P_0	P112	I/O
0	IO_L02N_0	IO_L02N_0	P117	I/O
0	IO_L02P_0	IO_L02P_0	P116	I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	P123	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	P122	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	P126	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	P125	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	P131	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	P130	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	P135	VREF
0	IO_L08P_0	IO_L08P_0	P134	I/O
0	IO_L09N_0	IO_L09N_0	P140	I/O
0	IO_L09P_0	IO_L09P_0	P139	I/O
0	IO_L10N_0/HSWAP	IO_L10N_0/HSWAP	P143	DUAL
0	IO_L10P_0	IO_L10P_0	P142	I/O
0	IP	IP	P111	INPUT
0	IP	IP	P114	INPUT
0	IP	IP	P136	INPUT
0	IP	IP	P141	INPUT
0	IP_L03N_0	IP_L03N_0	P120	INPUT
0	IP_L03P_0	IP_L03P_0	P119	INPUT
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	P129	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	P128	GCLK
0	VCCO_0	VCCO_0	P121	VCCO
0	VCCO_0	VCCO_0	P138	VCCO
1	IO/A0	IO/A0	P98	DUAL
1	IO/VREF_1	IO/VREF_1	P83	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	P75	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	P74	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	P77	DUAL

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
2	IP	IP	P38	INPUT
2	IP	IP	P41	INPUT
2	IP	IP	P69	INPUT
2	IP_L03N_2/VREF_2	IP_L03N_2/VREF_2	P48	VREF
2	IP_L03P_2	IP_L03P_2	P47	INPUT
2	IP_L06N_2/M2/GCLK1	IP_L06N_2/M2/GCLK1	P57	DUAL/GCLK
2	IP_L06P_2/RDWR_B/GCLK0	IP_L06P_2/RDWR_B/GCLK0	P56	DUAL/GCLK
2	VCCO_2	VCCO_2	P42	VCCO
2	VCCO_2	VCCO_2	P49	VCCO
2	VCCO_2	VCCO_2	P64	VCCO
3	IP/VREF_3	IO/VREF_3	P31	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	P3	I/O
3	IO_L01P_3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	IO_L02P_3	P4	I/O
3	IO_L03N_3	IO_L03N_3	P8	I/O
3	IO_L03P_3	IO_L03P_3	P7	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	P15	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	P14	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3	P17	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	P16	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	P21	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4	P20	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	P23	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	P22	LHCLK
3	IO_L08N_3	IO_L08N_3	P26	I/O
3	IO_L08P_3	IO_L08P_3	P25	I/O
3	IO_L09N_3	IO_L09N_3	P33	I/O
3	IO_L09P_3	IO_L09P_3	P32	I/O
3	IO_L10N_3	IO_L10N_3	P35	I/O
3	IO_L10P_3	IO_L10P_3	P34	I/O
3	IP	IP	P6	INPUT
3	IO	IP	P10	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P18	INPUT
3	IP	IP	P24	INPUT
3	IO	IP	P29	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P36	INPUT
3	IP/VREF_3	IP/VREF_3	P12	VREF
3	VCCO_3	VCCO_3	P13	VCCO
3	VCCO_3	VCCO_3	P28	VCCO
GND	GND	GND	P11	GND
GND	GND	GND	P19	GND

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
3	IO_L14P_3	P41	I/O
3	IO_L15N_3	P48	I/O
3	IO_L15P_3	P47	I/O
3	IO_L16N_3	P50	I/O
3	IO_L16P_3	P49	I/O
3	IP	P6	INPUT
3	IP	P14	INPUT
3	IP	P26	INPUT
3	IP	P32	INPUT
3	IP	P43	INPUT
3	IP	P51	INPUT
3	IP/VREF_3	P20	VREF
3	VCCO_3	P21	VCCO
3	VCCO_3	P38	VCCO
3	VCCO_3	P46	VCCO
GND	GND	P10	GND
GND	GND	P17	GND
GND	GND	P27	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P53	GND
GND	GND	P70	GND
GND	GND	P79	GND
GND	GND	P85	GND
GND	GND	P95	GND
GND	GND	P105	GND
GND	GND	P121	GND
GND	GND	P131	GND
GND	GND	P141	GND
GND	GND	P156	GND
GND	GND	P173	GND
GND	GND	P182	GND
GND	GND	P188	GND
GND	GND	P198	GND
GND	GND	P208	GND
VCCAUX	DONE	P104	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P158	JTAG
VCCAUX	TDI	P207	JTAG
VCCAUX	TDO	P157	JTAG
VCCAUX	TMS	P155	JTAG
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	P44	VCCAUX

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX
VCCAUX	VCCAUX	P111	VCCAUX
VCCAUX	VCCAUX	P149	VCCAUX
VCCAUX	VCCAUX	P166	VCCAUX
VCCAUX	VCCAUX	P195	VCCAUX
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P67	VCCINT
VCCINT	VCCINT	P117	VCCINT
VCCINT	VCCINT	P170	VCCINT

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 143 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 143 and with the black diamond character (◆) in Table 143 and Figure 83.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 143: **FT256 Package Pinout**

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO	IO	IO	A7	I/O
0	IO	IO	IO	A12	I/O
0	IO	IO	IO	B4	I/O
0	IP	IP	IO	B6	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IP	IP	IO	B10	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	D9	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A14	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B14	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	A13	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	B13	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	E11	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	D11	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B11	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	C11	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E10	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	D10	I/O
0	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	F9	GCLK
0	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	E9	GCLK
0	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	A9	GCLK
0	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	A10	GCLK
0	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	D8	GCLK
0	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	C8	GCLK
0	IO_L12N_0	IO_L12N_0	IO_L12N_0	F8	I/O

User I/Os by Bank

Table 144, Table 145, and Table 146 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package.

The XC3S250E FPGA in the FT256 package has 18 unconnected balls, labeled with an "N.C." type. These pins are also indicated with the black diamond (◆) symbol in Figure 85.

Table 144: **User I/Os Per Bank on XC3S250E in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	44	20	10	1	5	8
Right	1	42	10	7	21	4	0(2)
Bottom	2	44	8	9	24	3	0(2)
Left	3	42	24	7	0	3	8
TOTAL		**172**	**62**	**33**	**46**	**15**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 145: **User I/Os Per Bank on XC3S500E in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	46	22	10	1	5	8
Right	1	48	15	7	21	5	0(2)
Bottom	2	48	11	9	24	4	0(2)
Left	3	48	28	7	0	5	8
TOTAL		**190**	**76**	**33**	**46**	**19**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 146: **User I/Os Per Bank on XC3S1200E in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	46	24	8	1	5	8
Right	1	48	14	8	21	5	0(2)
Bottom	2	48	13	7	24	4	0(2)
Left	3	48	27	8	0	5	8
TOTAL		**190**	**78**	**31**	**46**	**19**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IP_L17P_0/GCLK8	H10	GCLK
0	IP_L20N_0	G9	INPUT
0	IP_L20P_0	G8	INPUT
0	IP_L23N_0	C8	INPUT
0	IP_L23P_0	D8	INPUT
0	IP_L26N_0	E6	INPUT
0	IP_L26P_0	E7	INPUT
0	IP_L29N_0	A4	INPUT
0	IP_L29P_0	A5	INPUT
0	VCCO_0	B4	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	D7	VCCO
0	VCCO_0	D13	VCCO
0	VCCO_0	F10	VCCO
1	IO_L01N_1/A15	U18	DUAL
1	IO_L01P_1/A16	U17	DUAL
1	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	T17	DUAL
1	IO_L03N_1/VREF_1	V19	VREF
1	IO_L03P_1	U19	I/O
1	IO_L04N_1	W20	I/O
1	IO_L04P_1	V20	I/O
1	IO_L05N_1	R18	I/O
1	IO_L05P_1	R17	I/O
1	IO_L06N_1	T20	I/O
1	IO_L06P_1	U20	I/O
1	IO_L07N_1	P18	I/O
1	IO_L07P_1	P17	I/O
1	IO_L08N_1/VREF_1	P20	VREF
1	IO_L08P_1	R20	I/O
1	IO_L09N_1	P16	I/O
1	IO_L09P_1	N16	I/O
1	IO_L10N_1	N19	I/O
1	IO_L10P_1	N18	I/O
1	IO_L11N_1	N15	I/O
1	IO_L11P_1	M15	I/O
1	IO_L12N_1/A11	M18	DUAL
1	IO_L12P_1/A12	M17	DUAL
1	IO_L13N_1/VREF_1	L19	VREF
1	IO_L13P_1	M19	I/O
1	IO_L14N_1/A9/RHCLK1	L16	RHCLK/ DUAL

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
1	IO_L14P_1/A10/RHCLK0	M16	RHCLK/ DUAL
1	IO_L15N_1/A7/RHCLK3/ TRDY1	L14	RHCLK/ DUAL
1	IO_L15P_1/A8/RHCLK2	L15	RHCLK/ DUAL
1	IO_L16N_1/A5/RHCLK5	K14	RHCLK/ DUAL
1	IO_L16P_1/A6/RHCLK4/ IRDY1	K13	RHCLK/ DUAL
1	IO_L17N_1/A3/RHCLK7	J20	RHCLK/ DUAL
1	IO_L17P_1/A4/RHCLK6	K20	RHCLK/ DUAL
1	IO_L18N_1/A1	K16	DUAL
1	IO_L18P_1/A2	J16	DUAL
1	IO_L19N_1/A0	J13	DUAL
1	IO_L19P_1	J14	I/O
1	IO_L20N_1	J17	I/O
1	IO_L20P_1	J18	I/O
1	IO_L21N_1	H19	I/O
1	IO_L21P_1	J19	I/O
1	IO_L22N_1	H15	I/O
1	IO_L22P_1	H16	I/O
1	IO_L23N_1	H18	I/O
1	IO_L23P_1	H17	I/O
1	IO_L24N_1/VREF_1	H20	VREF
1	IO_L24P_1	G20	I/O
1	IO_L25N_1	G16	I/O
1	IO_L25P_1	F16	I/O
1	IO_L26N_1	F19	I/O
1	IO_L26P_1	F20	I/O
1	IO_L27N_1	F18	I/O
1	IO_L27P_1	F17	I/O
1	IO_L28N_1	D20	I/O
1	IO_L28P_1	E20	I/O
1	IO_L29N_1/LDC0	D18	DUAL
1	IO_L29P_1/HDC	E18	DUAL
1	IO_L30N_1/LDC2	C19	DUAL
1	IO_L30P_1/LDC1	C20	DUAL
1	IP	B20	INPUT
1	IP	G15	INPUT
1	IP	G18	INPUT
1	IP	H14	INPUT
1	IP	J15	INPUT

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IP_L14P_2	T9	INPUT
2	IP_L17N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L17P_2/RDWR_B/ GCLK0	P11	DUAL/ GCLK
2	IP_L20N_2	T12	INPUT
2	IP_L20P_2	R12	INPUT
2	IP_L23N_2/VREF_2	T13	VREF
2	IP_L23P_2	T14	INPUT
2	IP_L26N_2	V14	INPUT
2	IP_L26P_2	V15	INPUT
2	IP_L29N_2	W16	INPUT
2	IP_L29P_2	Y16	INPUT
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	D3	I/O
3	IO_L02N_3/VREF_3	E3	VREF
3	IO_L02P_3	E4	I/O
3	IO_L03N_3	C1	I/O
3	IO_L03P_3	B1	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F3	I/O
3	IO_L05P_3	F4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L07N_3	G4	I/O
3	IO_L07P_3	G3	I/O
3	IO_L08N_3	G5	I/O
3	IO_L08P_3	H5	I/O
3	IO_L09N_3/VREF_3	H3	VREF
3	IO_L09P_3	H2	I/O
3	IO_L10N_3	H7	I/O
3	IO_L10P_3	H6	I/O
3	IO_L11N_3	J4	I/O
3	IO_L11P_3	J3	I/O
3	IO_L12N_3	J1	I/O
3	IO_L12P_3	J2	I/O
3	IO_L13N_3	J6	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IO_L13P_3	K6	I/O
3	IO_L14N_3/LHCLK1	K2	LHCLK
3	IO_L14P_3/LHCLK0	K3	LHCLK
3	IO_L15N_3/LHCLK3/IRDY2	L7	LHCLK
3	IO_L15P_3/LHCLK2	K7	LHCLK
3	IO_L16N_3/LHCLK5	L1	LHCLK
3	IO_L16P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L17N_3/LHCLK7	L3	LHCLK
3	IO_L17P_3/LHCLK6	M3	LHCLK
3	IO_L18N_3	M7	I/O
3	IO_L18P_3	M8	I/O
3	IO_L19N_3	M4	I/O
3	IO_L19P_3	M5	I/O
3	IO_L20N_3/VREF_3	N6	VREF
3	IO_L20P_3	M6	I/O
3	IO_L21N_3	N2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	P7	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	N4	I/O
3	IO_L23P_3	N3	I/O
3	IO_L24N_3	R1	I/O
3	IO_L24P_3	P1	I/O
3	IO_L25N_3	R5	I/O
3	IO_L25P_3	P5	I/O
3	IO_L26N_3	T2	I/O
3	IO_L26P_3	R2	I/O
3	IO_L27N_3	R4	I/O
3	IO_L27P_3	R3	I/O
3	IO_L28N_3/VREF_3	T1	VREF
3	IO_L28P_3	U1	I/O
3	IO_L29N_3	T3	I/O
3	IO_L29P_3	U3	I/O
3	IO_L30N_3	V1	I/O
3	IO_L30P_3	V2	I/O
3	IP	F5	INPUT
3	IP	G1	INPUT
3	IP	G6	INPUT
3	IP	H1	INPUT
3	IP	J5	INPUT
3	IP	L5	INPUT
3	IP	L8	INPUT
3	IP	M2	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IP	E6	INPUT
0	IP_L02N_0	D17	INPUT
0	IP_L02P_0	D18	INPUT
0	IP_L05N_0	C17	INPUT
0	IP_L05P_0	B17	INPUT
0	IP_L08N_0	E15	INPUT
0	IP_L08P_0	D15	INPUT
0	IP_L14N_0	D13	INPUT
0	IP_L14P_0	C13	INPUT
0	IP_L17N_0	A12	INPUT
0	IP_L17P_0	A13	INPUT
0	IP_L20N_0/GCLK9	H11	GCLK
0	IP_L20P_0/GCLK8	H12	GCLK
0	IP_L23N_0	F10	INPUT
0	IP_L23P_0	F11	INPUT
0	IP_L26N_0	G9	INPUT
0	IP_L26P_0	G10	INPUT
0	IP_L31N_0	C8	INPUT
0	IP_L31P_0	D8	INPUT
0	IP_L34N_0	C7	INPUT
0	IP_L34P_0	C6	INPUT
0	IP_L37N_0	A3	INPUT
0	IP_L37P_0	A2	INPUT
0	VCCO_0	B5	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	F14	VCCO
0	VCCO_0	G11	VCCO
1	IO_L01N_1/A15	Y22	DUAL
1	IO_L01P_1/A16	AA22	DUAL
1	IO_L02N_1/A13	W21	DUAL
1	IO_L02P_1/A14	Y21	DUAL
1	IO_L03N_1/VREF_1	W20	VREF
1	IO_L03P_1	V20	I/O
1	IO_L04N_1	U19	I/O
1	IO_L04P_1	V19	I/O
1	IO_L05N_1	V22	I/O
1	IO_L05P_1	W22	I/O
1	IO_L06N_1	T19	I/O
1	IO_L06P_1	T18	I/O
1	IO_L07N_1/VREF_1	U20	VREF
1	IO_L07P_1	U21	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IO_L08N_1	T22	I/O
1	IO_L08P_1	U22	I/O
1	IO_L09N_1	R19	I/O
1	IO_L09P_1	R18	I/O
1	IO_L10N_1	R16	I/O
1	IO_L10P_1	T16	I/O
1	IO_L11N_1	R21	I/O
1	IO_L11P_1	R20	I/O
1	IO_L12N_1/VREF_1	P18	VREF
1	IO_L12P_1	P17	I/O
1	IO_L13N_1	P22	I/O
1	IO_L13P_1	R22	I/O
1	IO_L14N_1	P15	I/O
1	IO_L14P_1	P16	I/O
1	IO_L15N_1	N18	I/O
1	IO_L15P_1	N19	I/O
1	IO_L16N_1/A11	N16	DUAL
1	IO_L16P_1/A12	N17	DUAL
1	IO_L17N_1/VREF_1	M20	VREF
1	IO_L17P_1	N20	I/O
1	IO_L18N_1/A9/RHCLK1	M22	RHCLK/ DUAL
1	IO_L18P_1/A10/RHCLK0	N22	RHCLK/ DUAL
1	IO_L19N_1/A7/RHCLK3/ TRDY1	M16	RHCLK/ DUAL
1	IO_L19P_1/A8/RHCLK2	M15	RHCLK/ DUAL
1	IO_L20N_1/A5/RHCLK5	L21	RHCLK/ DUAL
1	IO_L20P_1/A6/RHCLK4/ IRDY1	L20	RHCLK/ DUAL
1	IO_L21N_1/A3/RHCLK7	L19	RHCLK/ DUAL
1	IO_L21P_1/A4/RHCLK6	L18	RHCLK/ DUAL
1	IO_L22N_1/A1	K22	DUAL
1	IO_L22P_1/A2	L22	DUAL
1	IO_L23N_1/A0	K17	DUAL
1	IO_L23P_1	K16	I/O
1	IO_L24N_1	K19	I/O
1	IO_L24P_1	K18	I/O
1	IO_L25N_1	K15	I/O
1	IO_L25P_1	J15	I/O
1	IO_L26N_1	J20	I/O
1	IO_L26P_1	J21	I/O