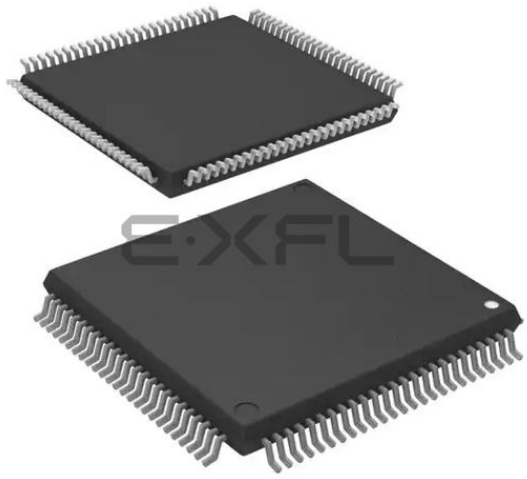

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38799fp10v

1.3 Pin Assignment

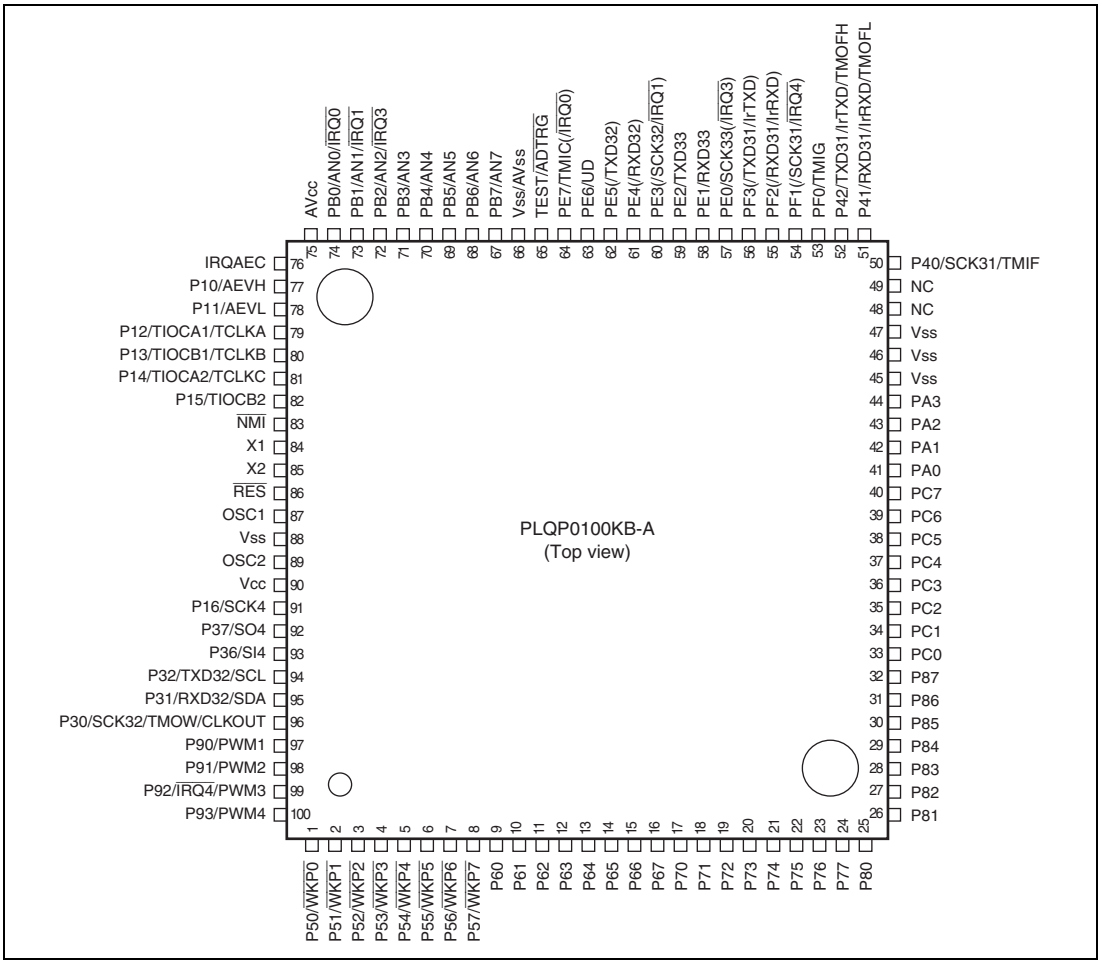

Figure 1.2 Pin Assignment of H8/38799 Group (PLQP0100KB-A)

- Description on operation

1. When the BCLR instruction is executed, first the CPU reads PCR5. Since PCR5 is a write-only register, the CPU reads a value of H'FF, even though the PCR5 value is actually H'3F.
2. Next, the CPU clears bit 0 in the read data to 0, changing the data to H'FE.
3. Finally, H'FE is written to PCR5 and BCLR instruction execution ends.

   As a result of this operation, bit 0 in PCR5 becomes 0, making P50 an input port. However, bits 7 and 6 in PCR5 change to 1, so that P57 and P56 change from input pins to output pins. To prevent this problem, store a copy of the PDR5 data in a work area in memory and manipulate data of the bit in the work area, then write this data to PDR5.

- Prior to executing BCLR instruction

```
MOV.B   #H'3F, R0L
MOV.B   R0L,  @RAM0
MOV.B   R0L,  @PCR5
```

The PCR5 value (H'3F) is written to a work area in memory (RAM0) as well as to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	1

- BCLR instruction executed

```
BCLR   #0,    @RAM0:8
```

The BCLR instructions executed for the PCR5 work area (RAM0).

- After executing BCLR instruction

```
MOV.B   @RAM0, R0L
MOV.B   R0L,   @PCR5
```

The work area (RAM0) value is written to PCR5.

4.3.1 Interrupt Edge Select Register (IEGR)

IEGR selects the sense of an edge that generates interrupt requests of the $\overline{\text{NMI}}$, TMIF, $\overline{\text{ADTRG}}$, $\overline{\text{IRQ4}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ0}}$ pins.

Bit	Bit Name	Initial Value	R/W	Descriptions
7	NMIEG	0	R/W	NMI Edge Select 0: Detects a falling edge of the $\overline{\text{NMI}}$ pin input 1: Detects a rising edge of the $\overline{\text{NMI}}$ pin input
6	TMIFEG	0	R/W	TMIF Edge Select 0: Detects a falling edge of the TMIF pin input 1: Detects a rising edge of the TMIF pin input
5	ADTRGNEG	0	R/W	$\overline{\text{ADTRG}}$ Edge Select 0: Detects a falling edge of the $\overline{\text{ADTRG}}$ pin input 1: Detects a rising edge of the $\overline{\text{ADTRG}}$ pin input
4	IEG4	0	R/W	IRQ4 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ4}}$ pin input 1: Detects a rising edge of the $\overline{\text{IRQ4}}$ pin input
3	IEG3	0	R/W	IRQ3 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ3}}$ pin input 1: Detects a rising edge of the $\overline{\text{IRQ3}}$ pin input
2	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
1	IEG1	0	R/W	IRQ1 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ1}}$ pin input 1: Detects a rising edge of the $\overline{\text{IRQ1}}$ pin input
0	IEG0	0	R/W	IRQ0 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ0}}$ pin input 1: Detects a rising edge of the $\overline{\text{IRQ0}}$ pin input

3. If a conflict occurs between interrupt requests that are not held pending due to the settings of the IMTM1, IMTN0 bits in INTM or the I bit in CCR, the interrupt request with the highest mask level according to table 4.2 is selected regardless of the IPR setting.
4. When the CPU accepts an interrupt request, it starts interrupt exception handling after execution of the current instruction has been completed.
5. PC and CCR are saved to the stack area by interrupt exception handling.
6. Next, the I bit in CCR is set to 1. This masks all interrupts except NMI and address break.
7. The CPU generates a vector address for the accepted interrupt and starts interrupt handling by reading the interrupt routine start address in the vector table.

9.10 Port B

Port B is an input-only port: its pins can also be configured to function as an interrupt input pin and analog input pin. Figure 9.10 shows the pin configuration.

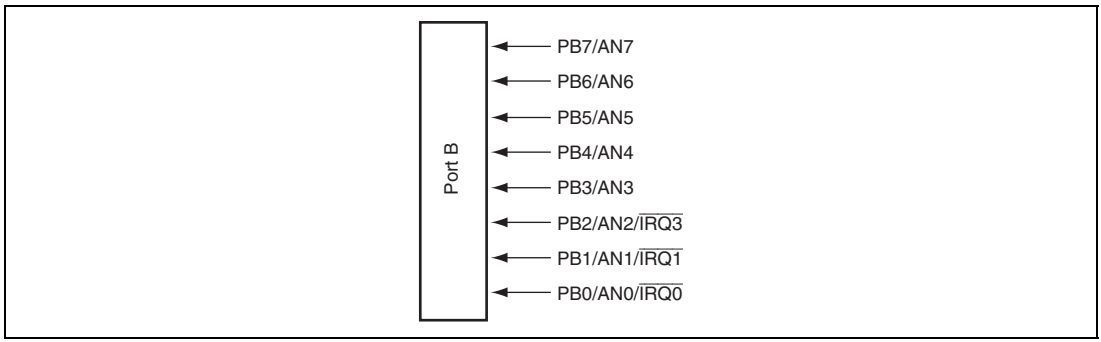

Figure 9.10 Port B Pin Configuration

Port B has the following registers.

- Port data register B (PDRB)
- Port mode register B (PMRB)

9.10.1 Port Data Register B (PDRB)

PDRB is a register that stores data of port B.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7	Undefined	R	Reading PDRB always gives the pin states. However, if a port B pin is selected as an analog input channel by the CH3 to CH0 bits in AMR of the A/D converter, that pin is read as 0 regardless of the input voltage.
6	PB6	Undefined	R	
5	PB5	Undefined	R	
4	PB4	Undefined	R	
3	PB3	Undefined	R	
2	PB2	Undefined	R	
1	PB1	Undefined	R	
0	PB0	Undefined	R	

12.5 Timer F Operating States

The timer F operating states are shown in table 12.2.

Table 12.2 Timer F Operating States

Operating Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCF	Reset	Functioning*1	Functioning*1	Functioning/ Halted*2	Functioning/ Halted*3	Functioning/ Halted*3	Halted	Halted
OCRF	Reset	Functioning	Retained	Retained	Functioning	Retained	Retained	Retained
TCRF	Reset	Functioning	Retained	Retained	Functioning	Retained	Retained	Retained
TCSRF	Reset	Functioning	Retained	Retained	Functioning	Retained	Retained	Retained

Note: 1. When $\phi_W/4$ is selected as the TCF input clock in active mode or sleep mode, since the system clock and internal clock are mutually asynchronous, synchronization is maintained by a synchronization circuit. This results in a maximum count cycle error of $1/\phi$ (s).

2. When the counter is operated in watch mode, $\phi_W/4$ must be selected as the internal clock. The counter will not operate if any other internal clock is selected.

3. When the counter is operated in subactive mode or subsleep mode, either an external clock or internal clock ϕ_W /4 must be selected as the input clock. The counter will not operate if any other internal clock is selected.

Section 14 16-Bit Timer Pulse Unit (TPU)

Microcontrollers of the H8/38799 Group have an on-chip 16-bit timer pulse unit (TPU) that comprises two 16-bit timer channels. The function list of the TPU is shown in table 14.1. A block diagram of the TPU is shown in figure 14.1.

14.1 Features

- Maximum 4-pulse input/output
- Selection of 7 or 8 counter input clocks for each channel
- The following operations can be set for each channel:
  Waveform output at compare match
  Input capture function
  Counter clear operation
  Multiple timer counters (TCNT) can be written to simultaneously
  Simultaneous clearing by compare match and input capture is possible
  Register synchronous input/output is possible by synchronous counter operation
  PWM output with any duty level is possible
  A maximum 3-phase PWM output is possible in combination with synchronous operation
- Operation with cascaded connection
- Fast access via internal 16-bit bus
- 6 types of interrupt sources
- Module standby mode enables this module to be placed in standby mode independently when it is not in use (for details, refer to section 6.4, Module Standby Function).

Table 14.8 TIOR_2 (Channel 2)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_2 Function**	**TIOCB2 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Capture input source is TIOCB2 pin Input capture at rising edge
			1		Capture input source is TIOCB2 pin Input capture at falling edge
		1	x		Capture input source is TIOCB2 pin Input capture at both edges

[Legend]

x: Don't care

16.3 Operation

16.3.1 Watchdog Timer Mode

The watchdog timer is provided with an 8-bit up-counter. To use it as the watchdog timer, clear the WT/$\overline{IT}$ bit in TCSRWD2 to 0. (To write the WT/$\overline{IT}$ bit, two write accesses are required.) If 1 is written to the WDON bit and 0 to the B2WI bit simultaneously when the TCSRWE bit in TCSRWD1 is set to 1, TCWD begins counting up. (To operate the watchdog timer, two write accesses to TCSRWD1 are required.) When a clock pulse is input after the TCWD count value has reached H'FF, the watchdog timer overflows and an internal reset signal is generated. The internal reset signal is output for a period of 512 clock cycles of the on-chip watchdog timer oscillator. TCWD is a writable counter, and when a value is set in TCWD, the count-up starts from that value. An overflow period in the range of 1 to 256 input clock cycles can therefore be set, according to the TCWD set value.

Figure 16.2 shows an example of watchdog timer operation.

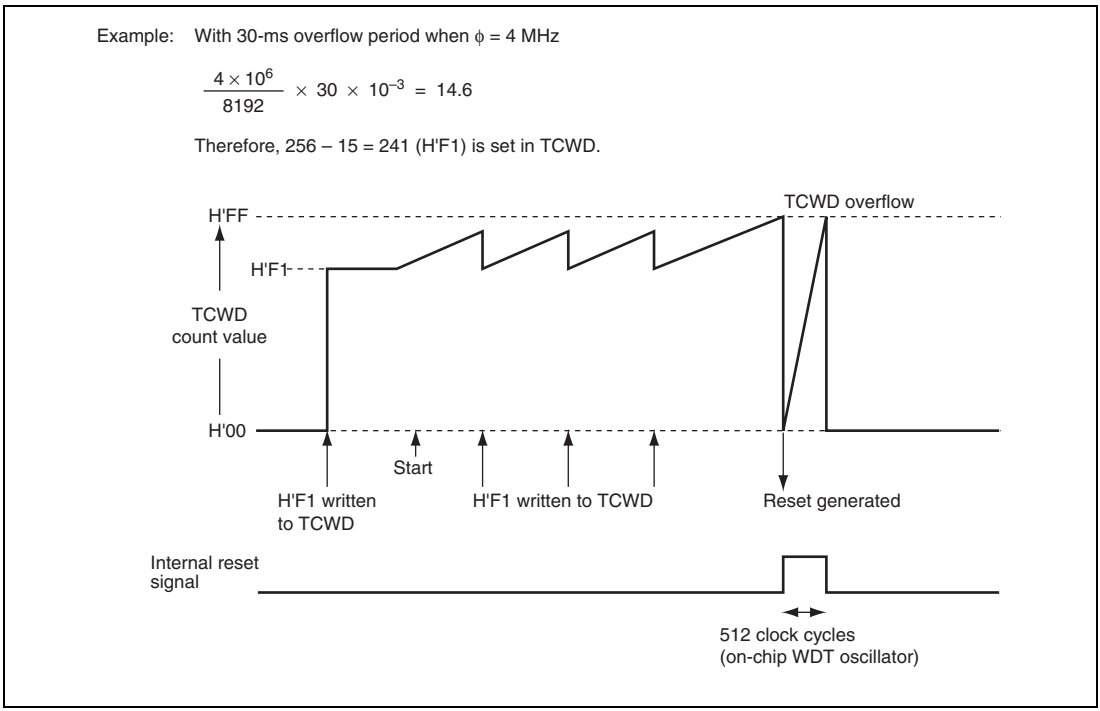

Figure 16.2 Example of Watchdog Timer Operation

Table 17.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode, ABCS = 0) (4)

Bit Rate	6.144 MHz			7.3728 MHz			8 MHz			9.8304 MHz			10 MHz		
(bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	108	0.08	2	130	–0.07	2	141	0.03	2	174	–0.26	2	177	–0.25
150	2	79	0.00	2	95	0.00	2	103	0.16	2	127	0.00	2	129	0.16
200	2	59	0.00	2	71	0.00	2	77	0.16	2	95	0.00	2	97	–0.35
250	2	47	0.00	2	57	–0.69	2	62	–0.79	2	76	–0.26	2	77	0.16
300	2	39	0.00	2	47	0.00	2	51	0.16	2	63	0.00	2	64	0.16
600	2	19	0.00	2	23	0.00	2	25	0.16	2	31	0.00	2	32	–1.36
1200	0	159	0.00	0	191	0.00	0	207	0.16	0	255	0.00	2	15	1.73
2400	0	79	0.00	0	95	0.00	0	103	0.16	0	127	0.00	0	129	0.16
4800	0	39	0.00	0	47	0.00	0	51	0.16	0	63	0.00	0	64	0.16
9600	0	19	0.00	0	23	0.00	0	25	0.16	0	31	0.00	0	32	–1.36
19200	0	9	0.00	0	11	0.00	0	12	0.16	0	15	0.00	0	15	1.73
31250	0	5	2.40	—	—	—	0	7	0.00	0	9	–1.70	0	9	0.00
38400	0	4	0.00	0	5	0.00	—	—	—	0	7	0.00	0	7	1.73

17.6.1 Multiprocessor Serial Data Transmission

Figure 17.16 shows a sample flowchart for multiprocessor serial data transmission. For an ID transmission cycle, set the MPBT bit in SSR to 1 before transmission. For a data transmission cycle, clear the MPBT bit in SSR to 0 before transmission. All other SCI3 operations are the same as those in asynchronous mode.

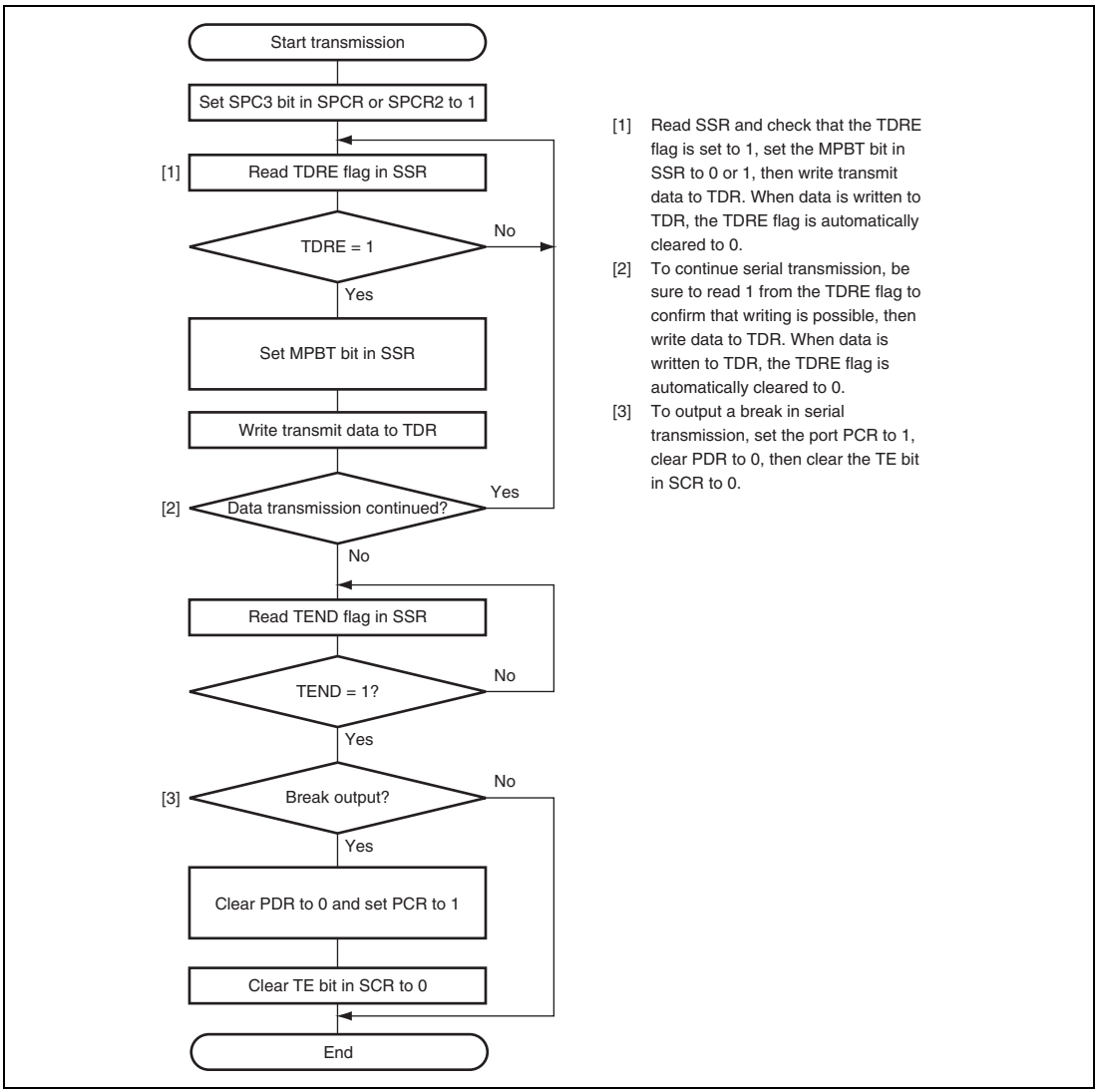

Figure 17.16 Sample Multiprocessor Serial Transmission Flowchart

17.8 Interrupt Requests

The SCI3 creates the following six interrupt requests: transmit end, transmit data empty, receive data full, and receive errors (overrun error, framing error, and parity error). Table 17.14 shows the interrupt sources.

Table 17.14 SCI3 Interrupt Requests

Interrupt Requests	Abbreviation	Interrupt Sources
Receive data full	RXI3	Setting RDRF in SSR
Transmit data empty	TXI3	Setting TDRE in SSR
Transmission end	TEI3	Setting TEND in SSR
Receive error	ERI3	Setting OER, FER, and PER in SSR

Each interrupt request can be enabled or disabled by means of bits TIE and RIE in SCR.

When the TDRE bit in SSR is set to 1, a TXI3 interrupt is requested. When the TEND bit in SSR is set to 1, a TEI3 interrupt is requested. These two interrupts are generated during transmission.

The initial value of the TDRE flag in SSR is 1. Thus, when the TIE bit in SCR is set to 1 before transferring the transmit data to TDR, a TXI3 interrupt request is generated even if the transmit data is not ready. The initial value of the TEND flag in SSR is 1. Thus, when the TEIE bit in SCR is set to 1 before transferring the transmit data to TDR, a TEI3 interrupt request is generated even if the transmit data has not been sent. It is possible to make use of the most of these interrupt requests efficiently by transferring the transmit data to TDR in the interrupt routine. To prevent the generation of these interrupt requests (TXI3 and TEI3), set the enable bits (TIE and TEIE) that correspond to these interrupt requests to 1, after transferring the transmit data to TDR.

When the RDRF bit in SSR is set to 1, an RXI3 interrupt is requested, and if any of bits OER, PER, and FER is set to 1, an ERI3 interrupt is requested. These two interrupt requests are generated during reception.

The SCI3 can carry out continuous reception using an RXI3 and continuous transmission using a TXI3.

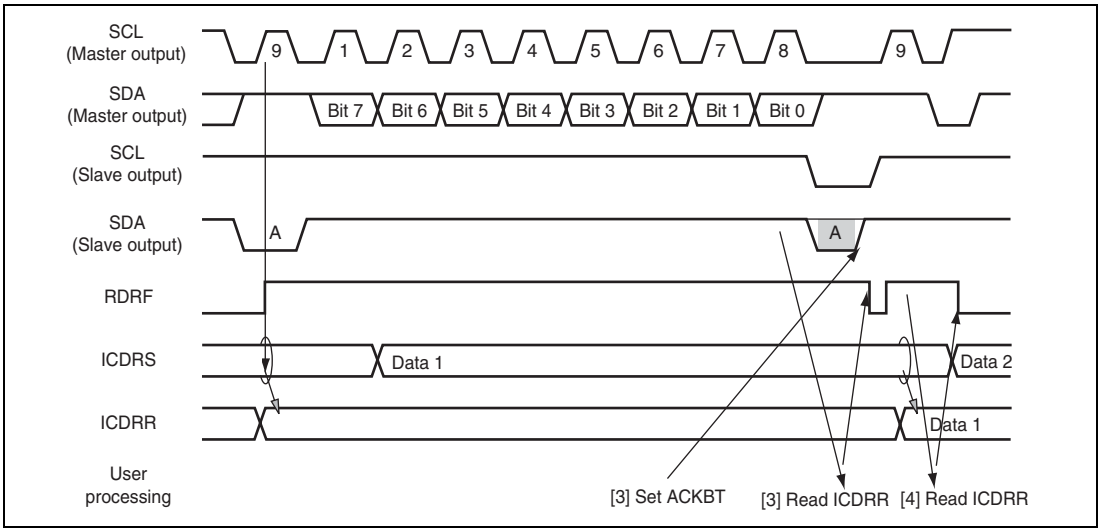

Figure 21.12 Slave Receive Mode Operation Timing (2)

21.4.6 Clock Synchronous Serial Format

This module can be operated with the clock synchronous serial format, by setting the FS bit in SAR to 1. When the MST bit in ICCR1 is 1, the transfer clock output from SCL is selected. When MST is 0, the external clock input is selected.

(1) Data Transfer Format

Figure 21.13 shows the clock synchronous serial transfer format.

The transfer data is output from the rise to the fall of the SCL clock, and the data at the rising edge of the SCL clock is guaranteed. The MLS bit in ICMR sets the order of data transfer, in either the MSB first or LSB first. The output level of SDA can be changed during the transfer wait, by the SDAO bit in ICCR2.

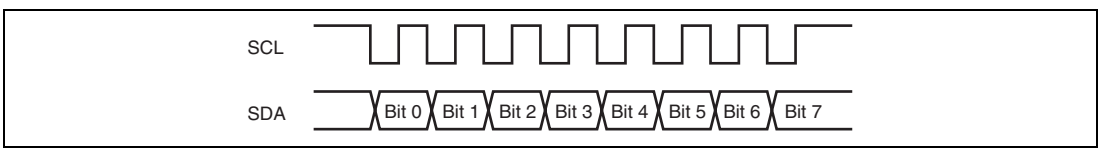

Figure 21.13 Clock Synchronous Serial Transfer Format

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Note
Active mode supply current	I_{OPE1}	V_{CC}	Active (high-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	1.1	—	mA	Max. guideline = 1.1 × typ *1 *2 *4
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = Rosc	—	3.7	—		Max. guideline = 1.1 × typ *1 *2
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	3.4	—		Max. guideline = 1.1 × typ *1 *2
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	7.4	11.0		*1 *2
	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	0.4	—	mA	Max. guideline = 1.1 × typ *1 *2 *5
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz, ϕ_{osc}/64	—	0.7	—		Max. guideline = 1.1 × typ *1 *2
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	1.1	1.5		*1 *2
Sleep mode supply current	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	1.0	—	mA	Max. guideline = 1.1 × typ *1 *2 *4
			V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	2.5	—		Max. guideline = 1.1 × typ *1 *2
			V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	5.2	7.5		*1 *2
Subactive mode supply current	I_{SUB}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_w/8)	—	9.0	—	µA	*1 *2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_w/2)	—	27.0	50.0		*1 *2

25.2.3 AC Characteristics

Table 25.3 lists the control signal timing, table 25.4 lists the serial interface timing, and table 25.5 lists the I^2C bus interface timing.

Table 25.3 Control Signal Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V (10-MHz version)	2.0	—	10.0	MHz	
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	2.0	—	4.2		
System clock on-chip oscillation frequency	f_{Rosc}		On-chip oscillator for system clock selected V_{CC} = 1.8 to 3.6 V	0.5	—	10.0		*3
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V (10-MHz version)	100	—	500	ns	Figure 25.14
			V_{CC} = 1.8 to 3.6 V (4-MHz version)	238	—	500		
System clock on-chip oscillation clock (ϕ_{ROSC}) cycle time	t_{ROSC}		On-chip oscillator for system clock selected V_{CC} = 1.8 to 3.6 V	100	—	2000		*3
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	
				—	—	32	µs	

25.5 Operation Timing

Figures 25.14 to 25.21 show operation timings.

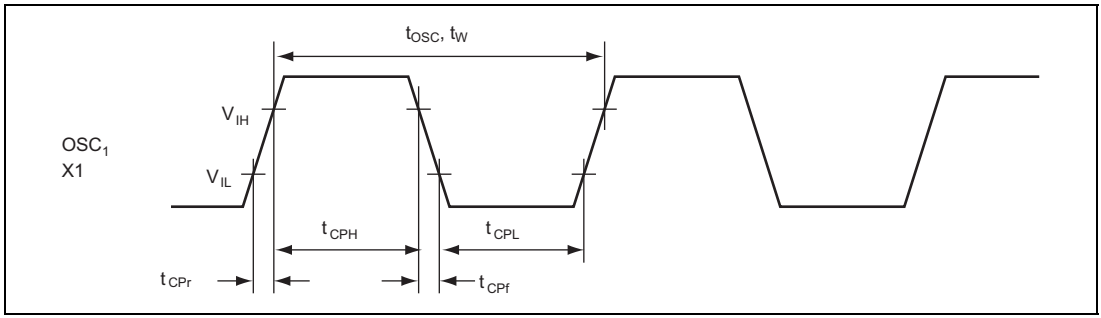

Figure 25.14 Clock Input Timing

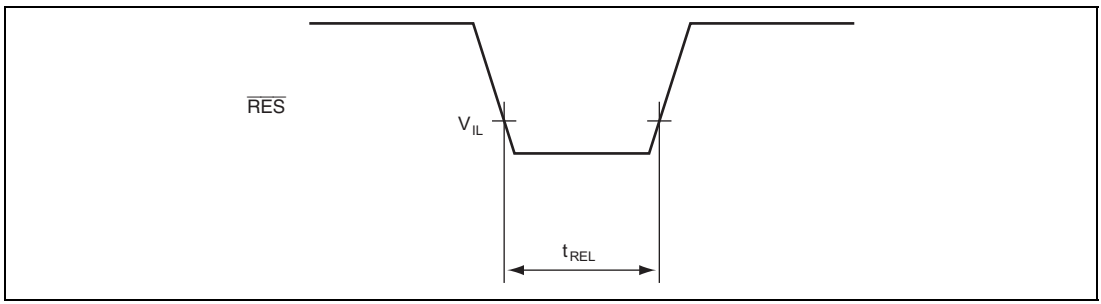

Figure 25.15 $\overline{RES}$ Low Width Timing

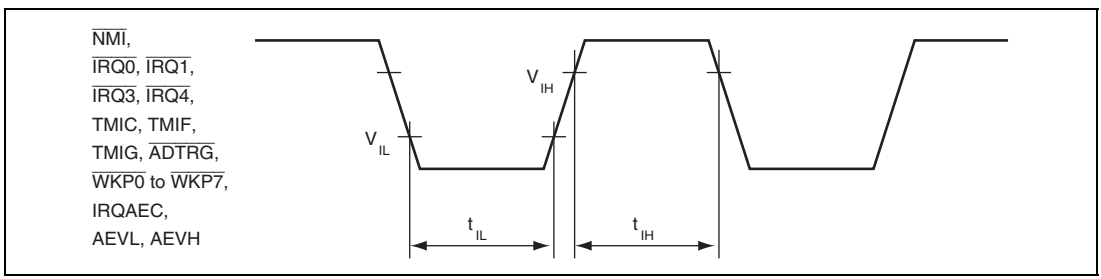

Figure 25.16 Input Timing

25.6 Output Load Circuit

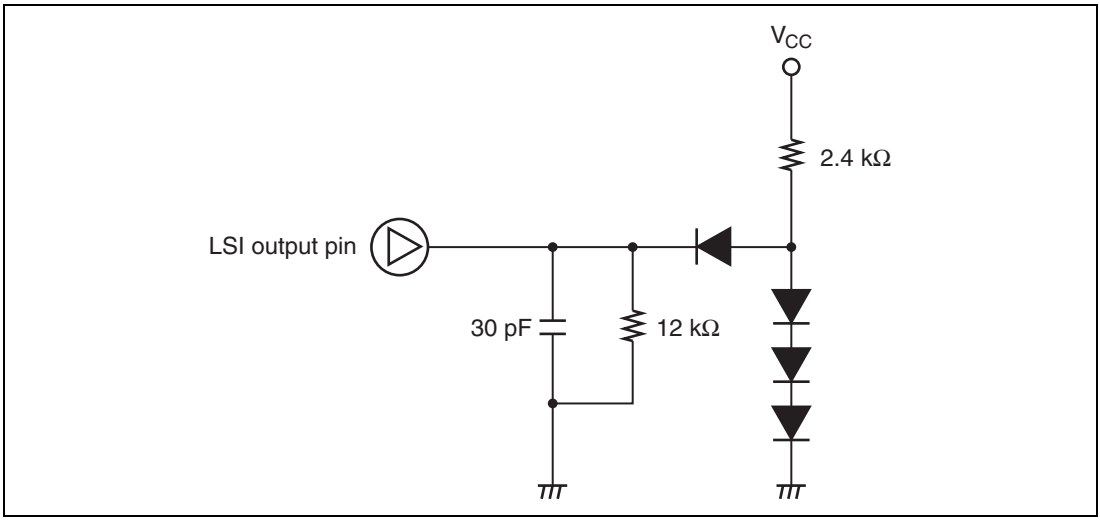

Figure 25.22 Output Load Condition

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ROTXR	ROTXR.B Rd	1					
	ROTXR.W Rd	1					
	ROTXR.L ERd	1					
RTE	RTE	2		2			2
RTS	RTS	2		1			2
SHAL	SHAL.B Rd	1					
	SHAL.W Rd	1					
	SHAL.L ERd	1					
SHAR	SHAR.B Rd	1					
	SHAR.W Rd	1					
	SHAR.L ERd	1					
SHLL	SHLL.B Rd	1					
	SHLL.W Rd	1					
	SHLL.L ERd	1					
SHLR	SHLR.B Rd	1					
	SHLR.W Rd	1					
	SHLR.L ERd	1					
SLEEP	SLEEP	1					
STC	STC CCR, Rd	1					
	STC CCR, @ERd	2				1	
	STC CCR, @(d:16,ERd)	3				1	
	STC CCR, @(d:24,ERd)	5				1	
	STC CCR,@-ERd	2				1	2
	STC CCR, @aa:16	3				1	
	STC CCR, @aa:24	4				1	
SUB	SUB.B Rs, Rd	1					
	SUB.W #xx:16, Rd	2					
	SUB.W Rs, Rd	1					
	SUB.L #xx:32, ERd	3					
	SUB.L ERs, ERd	1					
SUBS	SUBS #1/2/4, ERd	1					

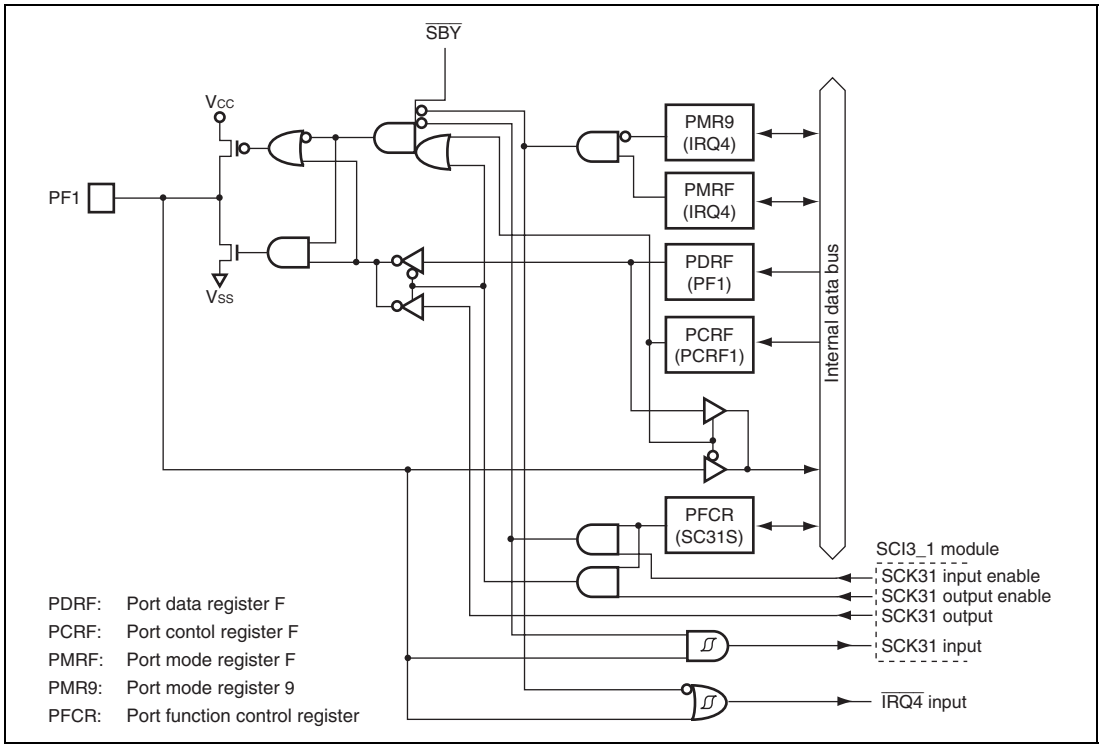

Figure B.13 (c) Port F Block Diagram (PF1)