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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 23x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf324lpmc1-g-jne2

1. Product Lineup

Memory Size

Product name		MB9BF321K/L/M	MB9BF322K/L/M	MB9BF324K/L/M
On-chip Flash memory	Main area	64 Kbytes	128 Kbytes	256 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	8 Kbytes	8 Kbytes	16 Kbytes
	SRAM1	8 Kbytes	8 Kbytes	16 Kbytes
	Total	16 Kbytes	16 Kbytes	32 Kbytes

Function

Product name			MB9BF321K MB9BF322K MB9BF324K	MB9BF321L MB9BF322L MB9BF324L	MB9BF321M MB9BF322M MB9BF324M
Pin count			48	64	80/96
CPU			Cortex-M3		
	Freq.		72 MHz		
Power supply voltage range			2.7 V to 5.5 V		
USB2.0 (Function/Host)			1ch. (Max)		
DMAC			8ch.		
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			4ch. (Max) ch.0/1/3: FIFO ch.5: No FIFO (In ch.1/5, only UART and LIN are available.)	8ch. (Max) ch.0/1/3/4 FIFO ch.2/5/6/7: No FIFO (In ch.1, only UART and LIN are available.)	
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF-Timer	A/D activation compare	2ch.	1 unit		
	Input capture	4ch.*			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
QPRC			1ch.	2ch. (Max)	
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			14 pins (Max) + NMI × 1	19 pins (Max) + NMI × 1	23 pins (Max) + NMI × 1
I/O ports			35 pins (Max)	50 pins (Max)	65 pins (Max)
12-bit A/D converter			14ch. (2 units)	23ch. (2 units)	26ch. (2 units)
10-bit D/A converter			2ch. (Max)		
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SWJ-DP		
Unique ID			Yes		

*: The external input channel which can be used is shown as follows.

- ch.0 to ch.3 : MB9BF321M/F322M/F324M
- ch.0, ch.2, ch.3 : MB9BF321K/F322K/F324K, MB9BF321L/F322L/F324L

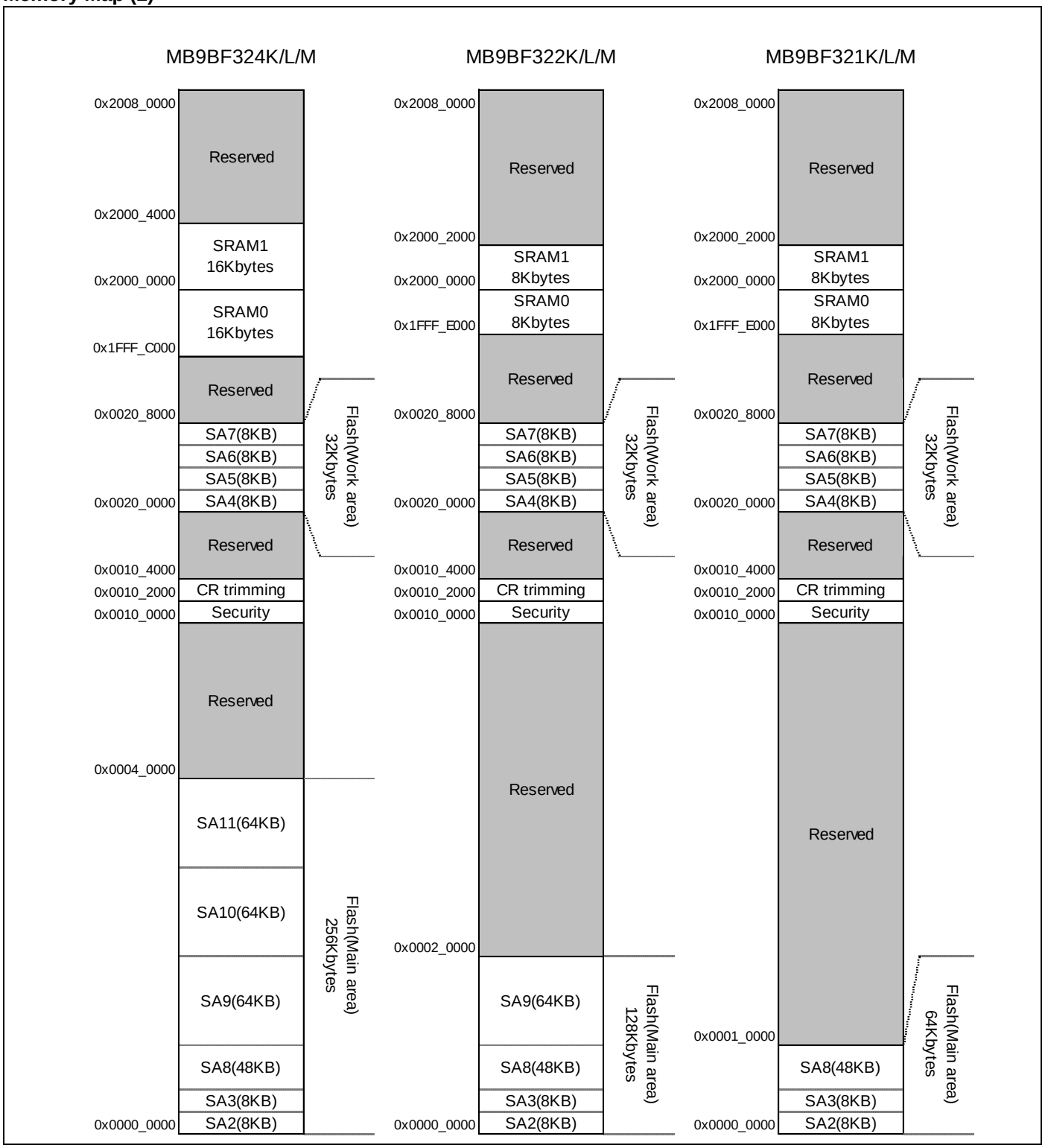
Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
See “12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics” for accuracy of built-in CR.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
45	H10	37	28	AVSS	-	
46	H9	38	29	P14	F	N
				AN04		
				INT03_1		
				IC02_2		
				SIN0_1		
47	G10	39	30	P15	F	N
				AN05		
				IC03_2		
				SOT0_1 (SDA0_1)		
				INT14_0		
48	G9	-	-	P16	F	N
				AN06		
				SCK0_1 (SCL0_1)		
				INT15_0		
49	F10	40	-	P17	F	N
				AN07		
				SIN2_2		
				INT04_1		
50	H11	41	31	AVCC	-	
51	F11	42	32	AVRH	-	
52	G11	43	33	AVRL	-	
53	F9	44	-	P18	F	M
				AN08		
				SOT2_2 (SDA2_2)		
54	E11	45	-	P19	F	M
				AN09		
				SCK2_2 (SCL2_2)		
55	E10	-	-	P1A	F	N
				AN10		
				SIN4_1		
				INT05_1		
				IC00_1		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
76	C4	60	44	P60 SIN5_0 TIOA2_2 INT15_1 WKUP3 IGTRG_1 AN21	J*	N
77	A4	61	45	USBVCC	-	
78	A3	62	46	P80 UDM0 INT16_1	H	H
79	A2	63	47	P81 UDP0 INT17_1	H	H
80	A1	64	48	VSS	-	
-	A5, A7, A11, B2, B10, C3, C9, F1, F2, F3, J3, J9, K2, K10, L6	-	-	VSS	-	

*: 5 V tolerant I/O

Memory Map (2)



Refer to the programming manual for the detail of Flash main area.

■MB9AB40N/A40N/340N/140N/150R,MB9B520M/320M/120M Series Flash Programming Manual

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled		Hi-Z at trans-mission/ Input enabled/ Internal input fixed at "0" at reception	Hi-Z at trans-mission/ Input enabled/ Internal input fixed at "0" at reception	Hi-Z / Input enabled	Hi-Z / Input enabled	Hi-Z / Input enabled
I	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input disabled	Hi-Z / Internal input fixed at "0" / Analog input disabled	Hi-Z / Internal input fixed at "0" / Analog input disabled
	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									Maintain previous state
J	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB)*1, *3	$USBV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	Except for USB pin
		V_{SS} - 0.5	$USBV_{CC}$ + 0.5 (≤ 6.5 V)	V	USB pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*8
Clamp total maximum current	$\Sigma[I_{CLAMP}]$		+20	mA	*8
L level maximum output current*5	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
			39	mA	The pin doubled as USB I/O
L level average output current*6	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
			16.5	mA	The pin doubled as USB I/O
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*5	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
			- 39	mA	The pin doubled as USB I/O
H level average output current*6	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
			- 18	mA	The pin doubled as USB I/O
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: $USBV_{CC}$ must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8mA					
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OH} = - 18.0 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	
			$USBV_{CC}$ < 4.5 V, I_{OH} = - 12.0 mA					
L level output voltage	V_{OL}	4 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 4mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 2mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 12mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 8mA					
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OL} = 16.5mA	V_{SS}	-	0.4	V	
			$USBV_{CC}$ < 4.5 V, I_{OL} = 10.5mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	V_{CC} ≥ 4.5 V	33	50	90	kΩ	
			V_{CC} < 4.5 V	-	-	180		
Input capacitance	C_{IN}	Other than VCC, USBVCC, VSS, AVCC, AVSS, AVRH, AVRL	-	-	5	15	pF	

12.4.4 Operating Conditions of Main and USB PLL (In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	5	-	37	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	
USB clock frequency*3	$f_{CLKSPLL}$	-	-	48	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter: Clock” in “FM3 Family Peripheral Manual”.

*3: For more information about USB clock, see “Chapter 2-2: USB Clock Generation” in “FM3 Family Peripheral Manual Communication Macro Part”.

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	19	-	35	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	

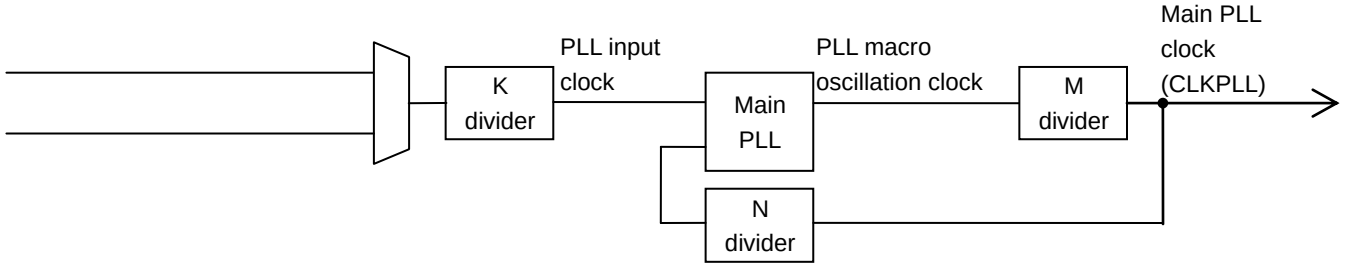
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter 2-1: Clock” in “FM3 Family Peripheral Manual”.

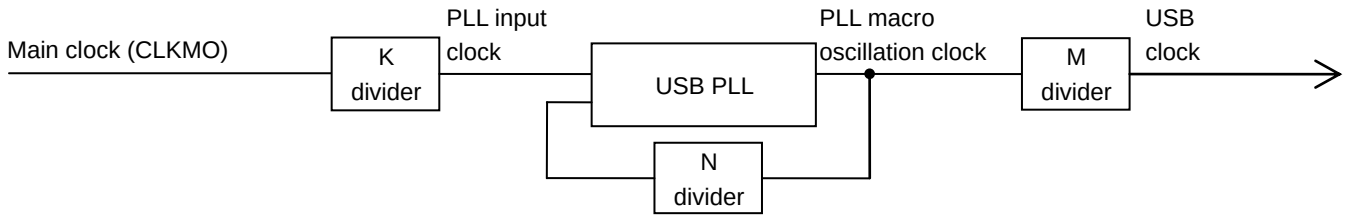
Note: Make sure to input to the Main PLL source clock, the high-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.

When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection



USB PLL connection



12.4.6 Reset Input Characteristics

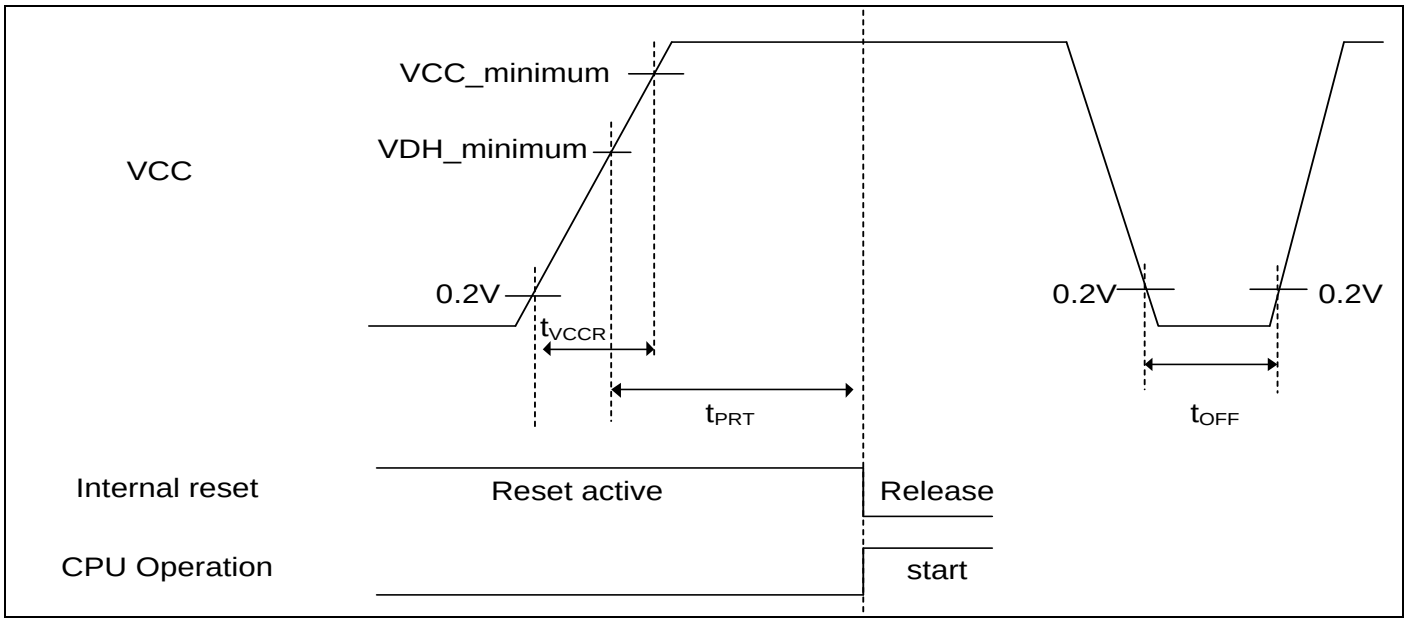
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{VCCR}	VCC	0	-	ms	
Power supply shut down time	t_{OFF}		1	-	ms	
Time until releasing Power-on reset	t_{PRT}		1.34	18.6	ms	



Glossary

VCC_minimum : Minimum V_{CC} of recommended operating conditions

VDH_minimum : Minimum detection voltage (when SVHR=00000) of Low-Voltage detection reset

See “12.8. Low-Voltage Detection Characteristics”

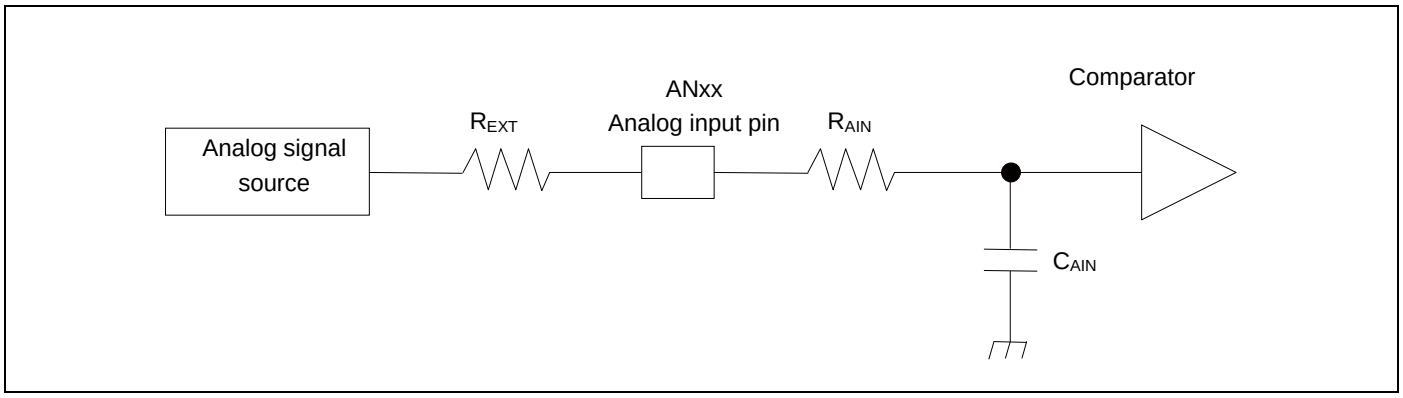
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see “Block Diagram” in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: input resistor of A/D = 1.5 kΩ at 4.5 V $\leq AV_{CC} \leq$ 5.5 V ch.0 to ch.7
input resistor of A/D = 1.6 kΩ at 4.5 V $\leq AV_{CC} \leq$ 5.5 V ch.8 to ch.15
input resistor of A/D = 1.7 kΩ at 4.5 V $\leq AV_{CC} \leq$ 5.5 V ch.16 to ch.26
input resistor of A/D = 2.2 kΩ at 2.7 V $\leq AV_{CC} <$ 4.5 V ch.0 to ch.7
input resistor of A/D = 2.3 kΩ at 2.7 V $\leq AV_{CC} <$ 4.5 V ch.8 to ch.15
input resistor of A/D = 2.4 kΩ at 2.7 V $\leq AV_{CC} <$ 4.5 V ch.16 to ch.26

C_{AIN}: input capacity of A/D = 9.7 pF at 2.7 V $\leq AV_{CC} \leq$ 5.5 V

R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

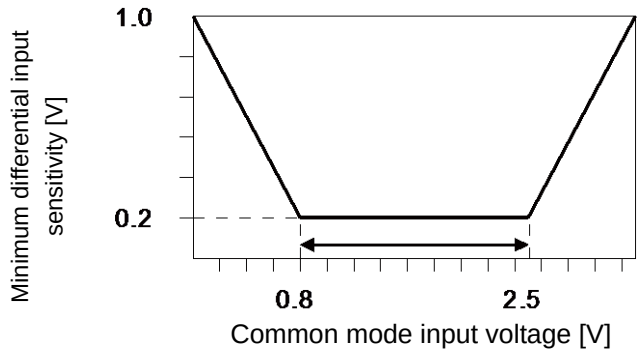
12.7 USB Characteristics

(V_{CC} = 2.7V to 5.5V, $USBV_{CC}$ = 3.0V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	$USBV_{CC}$ + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-down resistor = 15kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistor = 1.5kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-Speed	4	20	ns	*5
	Falling time	t_{FF}		Full-Speed	4	20	ns	*5
	Rising/ falling time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-Speed	75	300	ns	*7
	Falling time	t_{LF}		Low-Speed	75	300	ns	*7
	Rising/ falling time matching	t_{LRFM}		Low-Speed	80	125	%	*7

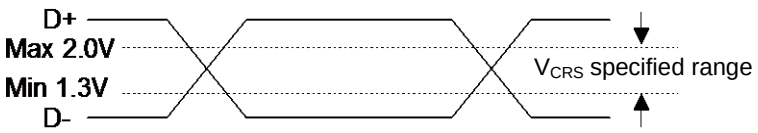
*1: The switching threshold voltage of the Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2: Use the differential-Receiver to receive the USB differential data signal.
The Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
The voltage range above is said to be the common mode input voltage range.

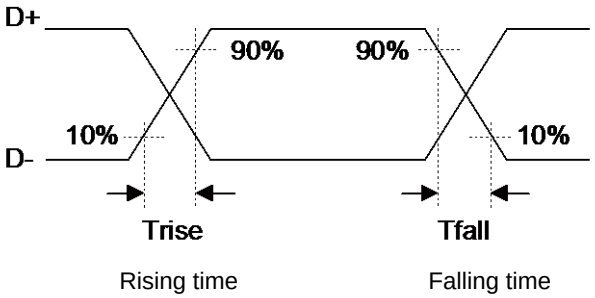


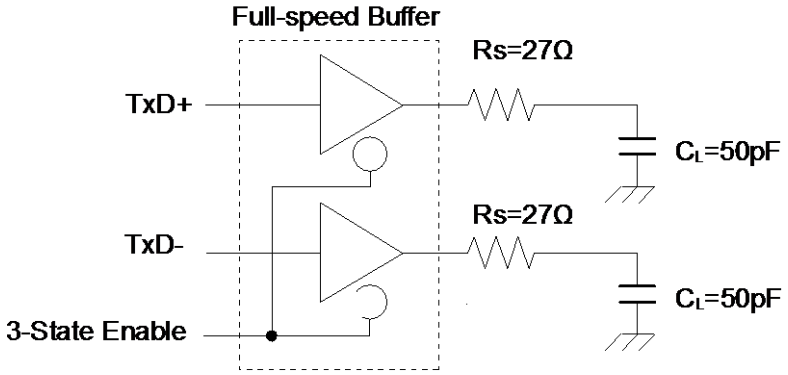
*3: The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to ground and 15 kΩ load) at High-State (V_{OH}).

*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.



*5: They indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.





12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR*1= 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*2	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*1: The SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is initialized to "00000" by Low-Voltage Detection Reset.

*2: t_{CYCP} indicates the APB2 bus clock cycle time.

12.8.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.9 Flash Memory Write/Erase Characteristics

12.9.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

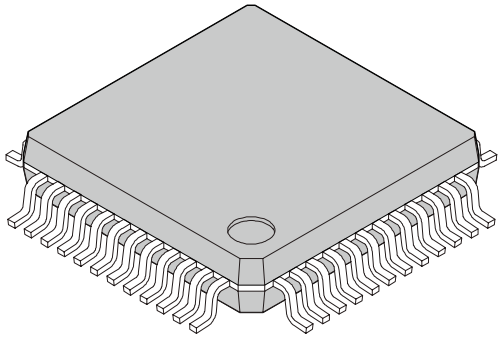
Parameter		Value		Unit	Remarks
		Typ	Max		
Sector erase time	Large Sector	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector	0.3	0.9		
Half word (16-bit) write time		16	310	µs	Not including system-level overhead time
Chip erase time		6.8	18	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximam value is guarantee value under 10,000 cycle of erase/write.

12.9.2 Write cycles and data hold time

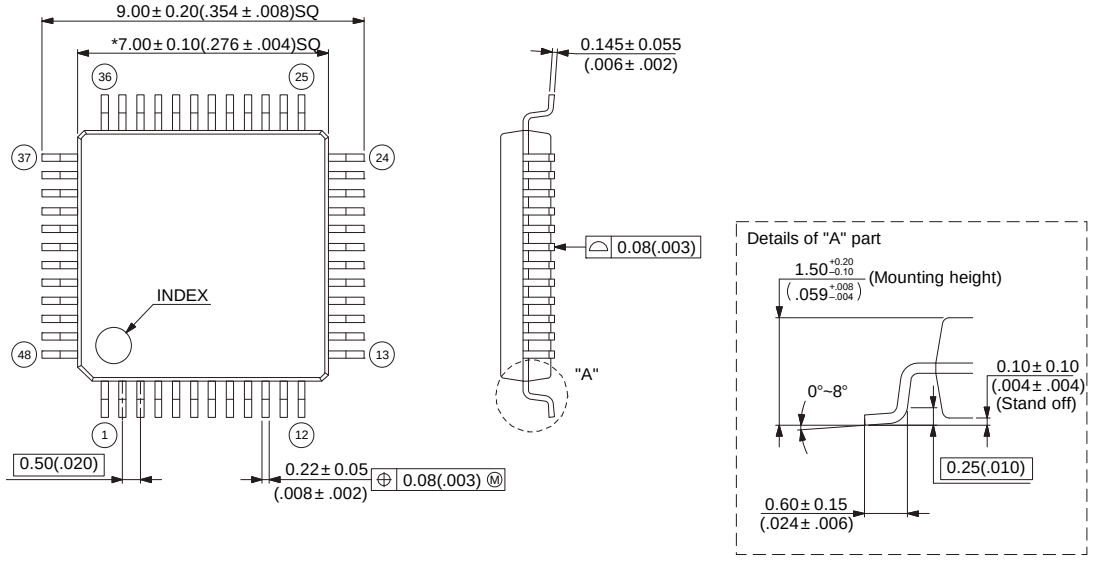
Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

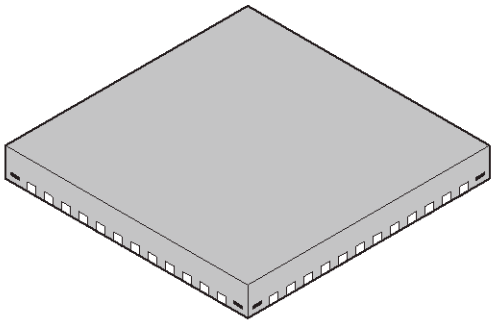
48-pin plastic LQFP		
 (FPT-48P-M49)	Lead pitch	0.50 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

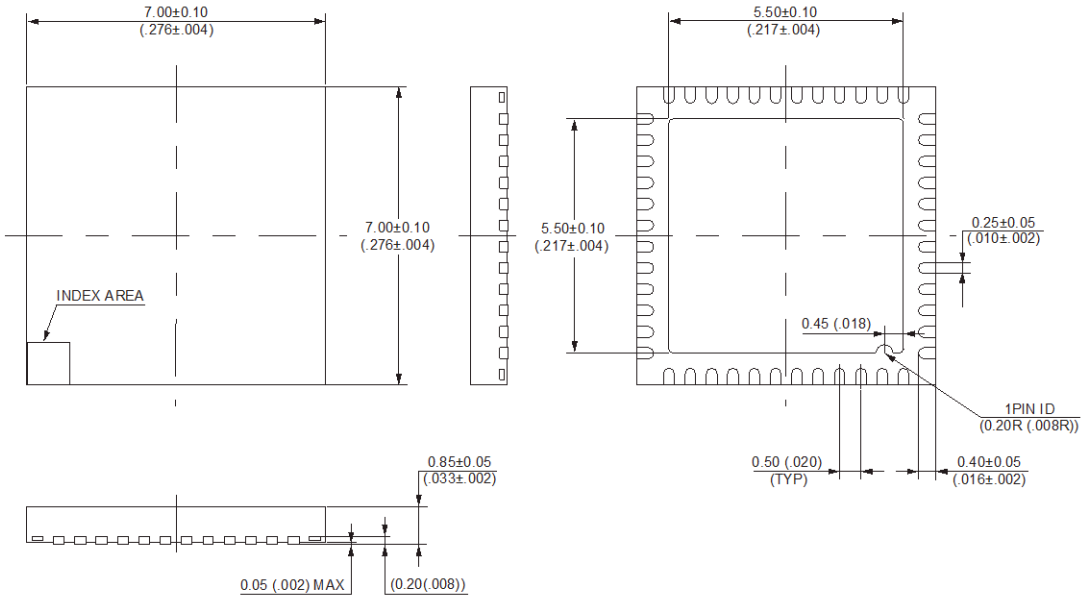
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

48-pin plastic QFN		
	Lead pitch	0.5 mm
	Package width × package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	–
(LCC-48P-M73)		

48-pin plastic QFN
(LCC-48P-M73)



Dimensions in mm (inches).
Note: The values in parentheses are reference **values**.

15. Major Changes

Spansion Publication Number: MB9B320M_DS706-00049

Page	Section	Change Results
Revision 1.0		
-	-	Preliminary → Data Sheet
3	Features A/D Converter (Max 26channels)	Revised the conversion time: 1.0µs → 0.8µs
6	Uniqueid	Added the "Unique ID".
7	Product Lineup Function	Added the "Unique ID".
16 to 18	List Of Pin Functions List Of Pin Numbers	Corrected the I/O circuit type. Corrected the Pin state type.
33	List Of Pin Functions	Corrected the Pin function.
39	I/O Circuit Type	Added the "Type: L".
46	Block Diagram	Corrected the figure. - TIOA: input → input/output - TIOB: output → input
55	Electrical Characteristics 1. Absolute Maximum Ratings	Revised the value of "TBD".
57	2. Recommended Operating Conditions	Revised the Condition of "Operating temperature".
58, 59	3. Dc Characteristics (1) Current Rating	Revised the value of "TBD". Added "Flash memory write/erase current".
62	4. Ac Characteristics (3) Built-In Cr Oscillation Characteristics	Revised the Condition. Revised the footnote.
63	(4-2) Operating Conditions Of Main PLL (In The Case Of Using Built-In High-Speed CR For Input Clock Of Main PLL)	Revised the value of "TBD".
79	5. 12-Bit A/D Converter Electrical Characteristics For The A/D Converter	Deleted "(Preliminary value)". Revised the conversion time. Min: 1.0µs → 0.8µs Revised the value of "Compare clock cycle ($AV_{CC} \geq 4.5V$)". Min: 50ns → 40ns Revised the footnote.
82	6. 10-Bit D/A Converter	Deleted "(Preliminary value)".
87	8. Low-Voltage Detection Characteristics	Revised the value of "TBD".
88	9. Mainflash Memory Write/Erase Characteristics	Revised the value of "TBD". Revised the value of "Sector erase time". - Large Sector Typ: 1.065s → 1.1s - Small Sector Typ: 0.606s → 0.3s Revised the value of "Chip erase time". Typ: 9.11s → 6.8s Deleted "(targeted value)".
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
2	Features On-Chip Memories [Flash Memory]	Revised the features of Dual operation Flash memory
	USB Interface [USB Function]	Added the size of each endpoint.
3	Multi-Function Serial Interface [I^2C]	Corrected the mode. High speed mode → Fast mode
4	General-Purpose I/O Port	Revised the features of 5V tolerant I/O.
	Multi-Function Timer	Corrected the number of A/D activating compare channels. 3ch. → 2ch.

Document History

Document Title: MB9B320M Series 32-Bit ARM® Cortex®-M3, FM3 Microcontroller
Document Number: 002-05652

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	TOYO	09/13/2012	Migrated to Cypress and assigned document number 002-05652. No change to document contents or format.
*A	5166569	TOYO	03/08/2016	Updated to Cypress format.