Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	126 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08ka4ctg

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9RS08KA8 MCU.

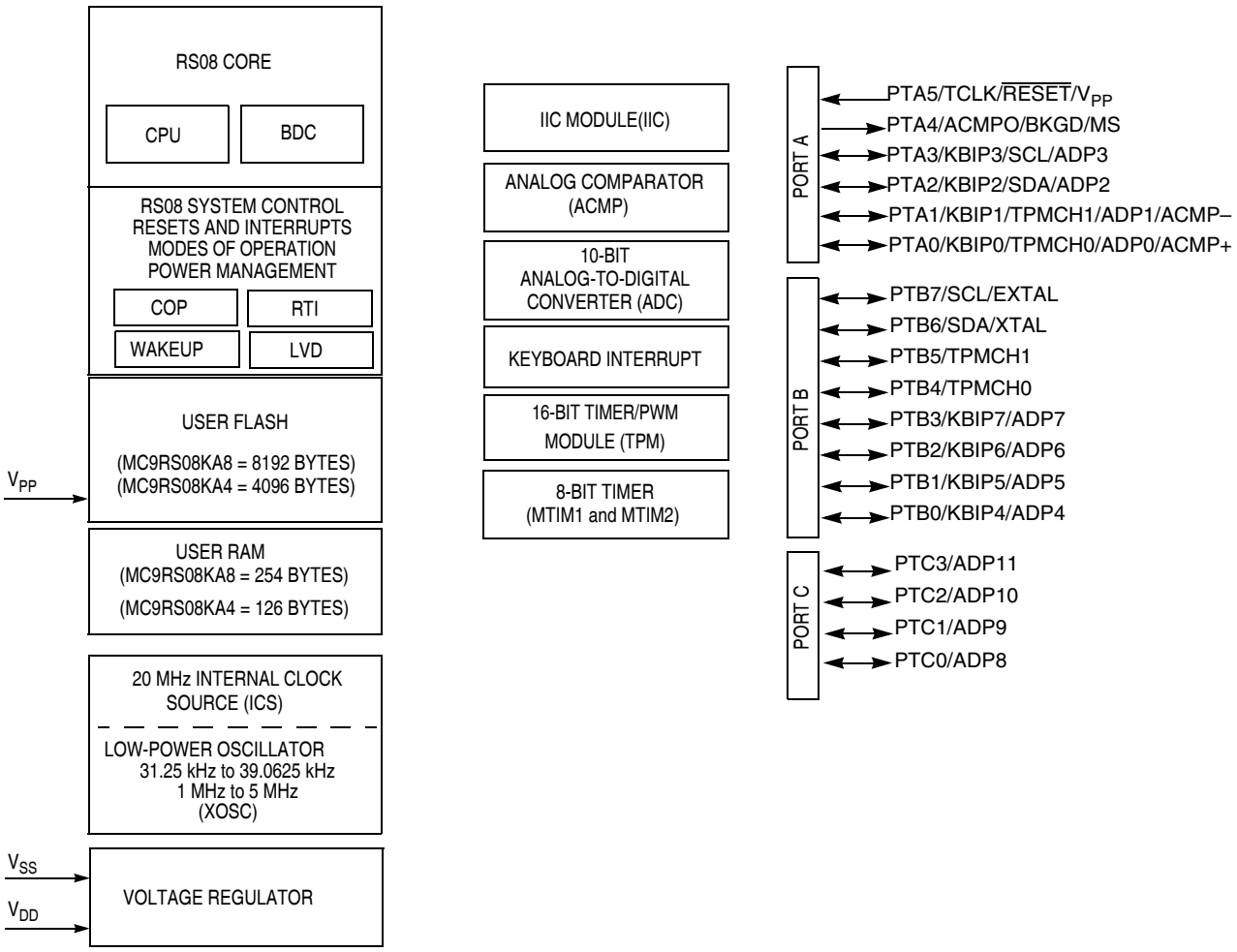


Figure 1. MC9RS08KA8 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KA8 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number		<-- Lowest **Priority** --> Highest				
20	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	PTA5		TCLK	$\overline{\text{RESET}}$	V_{PP}
2	2	PTA4	ACMPO	BKGD	MS	
3	3					V_{DD}
4	4					V_{SS}
5	5	PTB7	SCL[1]			EXTAL
6	6	PTB6	SDA[1]			XTAL
7	7	PTB5	TPMCH1[2]			
8	8	PTB4	TPMCH0[2]			
9	—	PTC3			ADP11	
10	—	PTC2			ADP10	
11	—	PTC1			ADP9	
12	—	PTC0			ADP8	
13	9	PTB3	KBIP7		ADP7	
14	10	PTB2	KBIP6		ADP6	
15	11	PTB1	KBIP5		ADP5	
16	12	PTB0	KBIP4		ADP4	
17	13	PTA3	KBIP3	SCL[1]	ADP3	
18	14	PTA2	KBIP2	SDA[1]	ADP2	
19	15	PTA1	KBIP1	TPMCH1[2]	ADP1	ACMP–
20	16	PTA0	KBIP0	TPMCH0[2]	ADP0	ACMP+

1 IIC pins can be remapped to PTA3 and PTA2

2 TPM pins can be remapped to PTA0 and PTA1

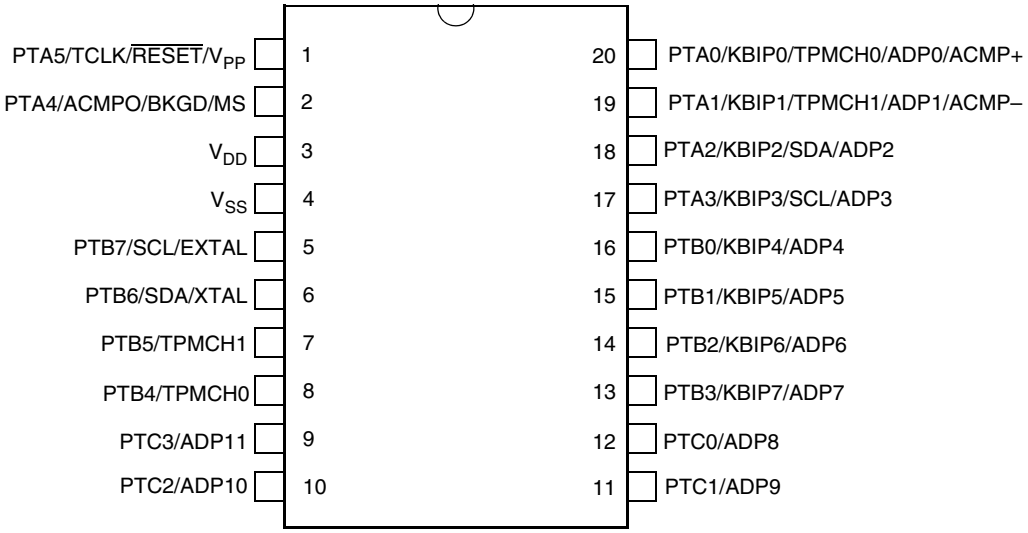


Figure 2. MC9RS08KA8 Series in 20-Pin PDIP/SOIC Package

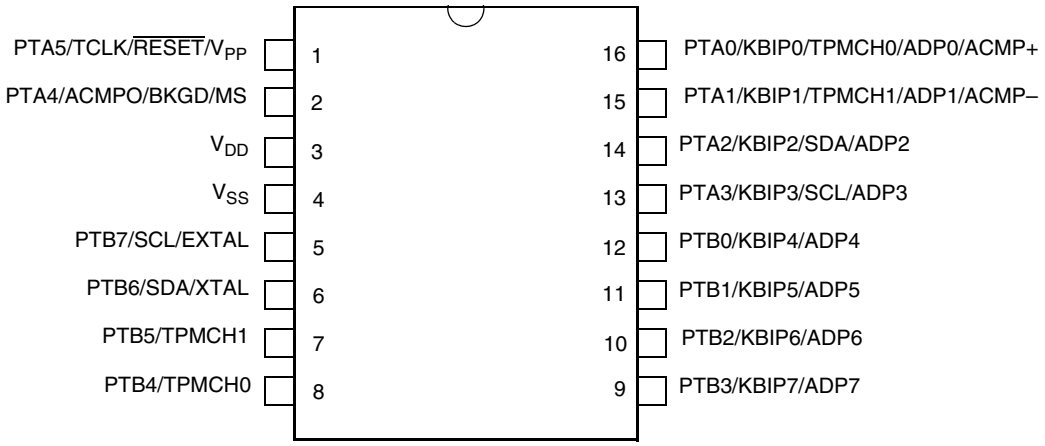


Figure 3. MC9RS08KA8 Series in 16-Pin PDIP/SOIC/TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KA8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C (applies to all pins except pin 9 PTC3/ADP11)	I_{LAT}	±100[2]	—	mA
	Latch-up current at T_A = 85°C (applies to pin 9 PTC3/ADP11)	I_{LAT}	±75[3]	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2 These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ±100mA.

3 This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ±75mA. This pin is only present on 20 pin package types.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage (run, wait and stop modes.) 0 < f_{Bus} <10MHz V_{DD} rising V_{DD} falling	V_{DD}	2.0 1.8	—	5.5	V
Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
Low-voltage Detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.03	V
Power on RESET (POR) voltage	V_{POR}[1]	0.9	—	1.7	V

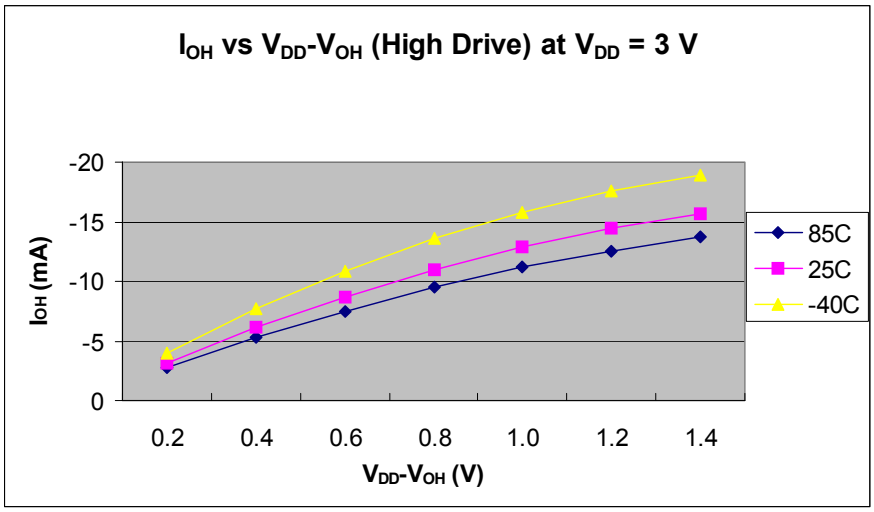


Figure 6. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 3 V (High Drive)

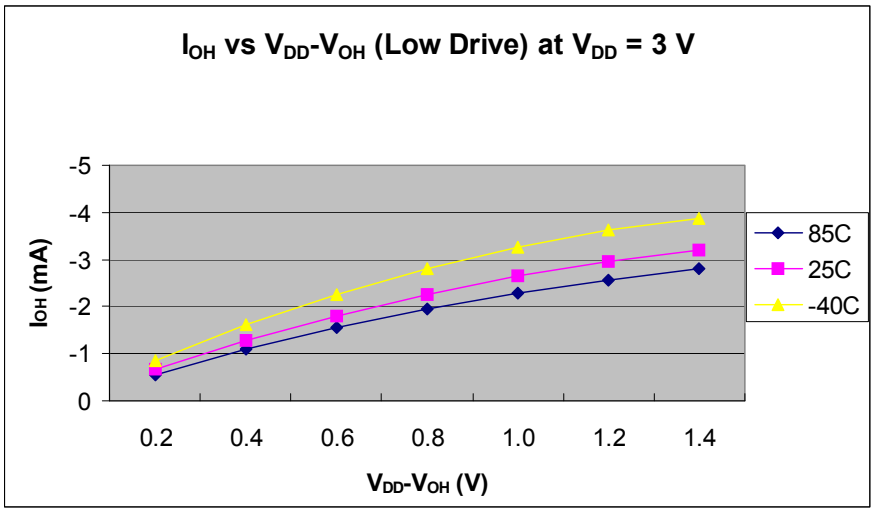


Figure 7. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 3 V (Low Drive)

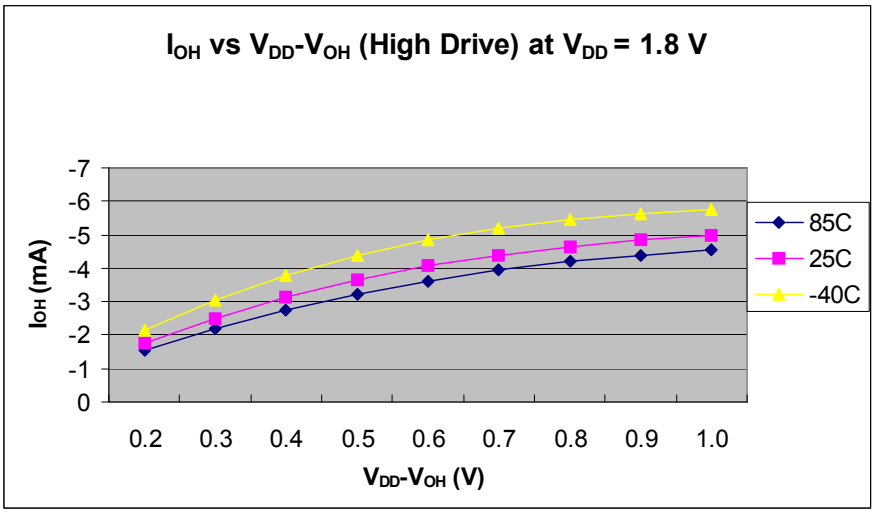


Figure 8. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 1.8 V (High Drive)

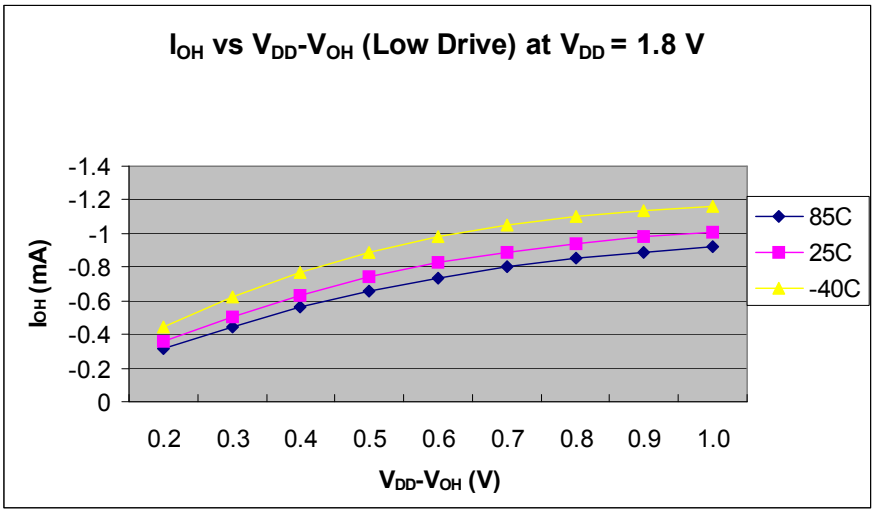


Figure 9. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 1.8 V (Low Drive)

Table 8. Supply Current Characteristics (continued)

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
Run supply current[3] measured at (f_{Bus} = 1.25 MHz)	RI_{DD1}	5	0.42 mA	2 mA	25 85
		3	0.42 mA	—	25 85
		1.80	0.3 mA	—	25 85
Stop mode supply current	SI_{DD}	5	2.4 µA	5 µA 8 µA	25 85
		3	2 µA	—	25 85
		1.80	1.5 µA	—	25 85
ADC adder from stop[4]	—	5	128 µA	150 µA 165 µA	25 85
		3	121 µA	—	25 85
		1.80	79 µA	—	25 85
ACMP adder from stop (ACME = 1)	—	5	21 µA	22 µA	25 85
		3	18.5 µA	—	25 85
		1.80	17.5 µA	—	25 85
RTI adder from stop with 1 kHz clock source enabled[5]	—	5	2.4 µA	2 µA	25 85
		3	1.9 µA	—	25 85
		1.80	1.5 µA	—	25 85
RTI adder from stop with 1 MHz external clock source reference enabled	—	5	2.1 µA	2 µA	25 85
		3	1.6 µA	—	25 85
		1.80	1.2 µA	—	25 85
LVI adder from stop (LVDE=1 and LVDSE=1)	—	5	70 µA	80 µA	25 85
		3	65 µA	—	25 85
		1.80	60 µA	—	25 85

1 Typicals are measured at 25°C.

2 Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

3 Not include any DC loads on port pins.

4 Required asynchronous ADC clock and LVD to be enabled.

5 Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 1.3 mA at 3 V and 1 mA at 2 V with f_{Bus} = 1 MHz.

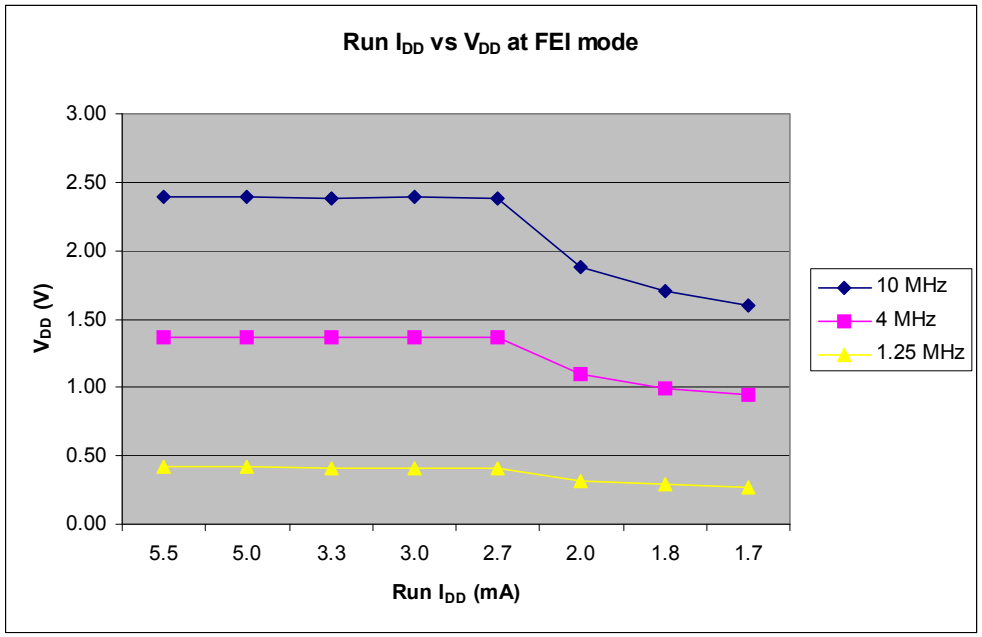


Figure 16. Typical Run I_{DD} vs. V_{DD} for FEI Mode

3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = –40 to 125°C Ambient)

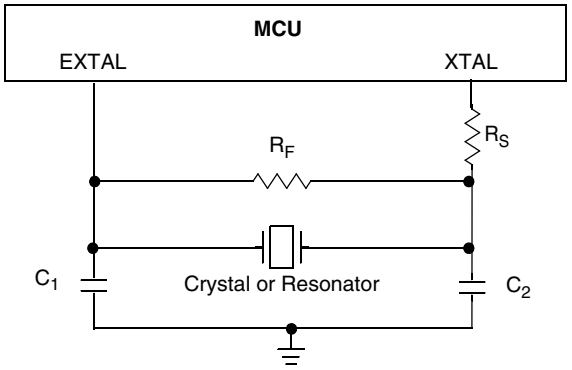
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	D	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	 MΩ
4	D	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	 kΩ
5	C	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 20	 — — — —	 ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] FBELP mode	f_{extal}	0.03125 0	—	5 40	MHz

1 Typical data was characterized at 5.0 V, 25 °C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal.



3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.1 Control Timing

Table 10. Control Timing

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	0	—	10	MHz
2	D	Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	µs
3	D	External $\overline{\text{RESET}}$ pulse width[1]	t_{extrst}	150	—	—	ns
4	D	KBI pulse width[2]	t_{KBIPW}	1.5 t_{cyc}	—	—	ns
5	D	KBI pulse width in stop[1]	t_{KBIPWS}	100	—	—	ns
6	D	Port rise and fall time (load = 50 pF)[3] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	— —	ns

1 This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

2 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

3 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

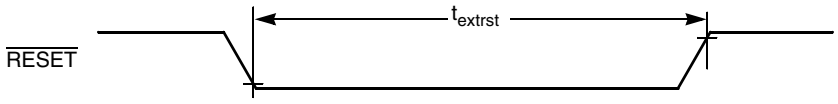


Figure 17. Reset Timing

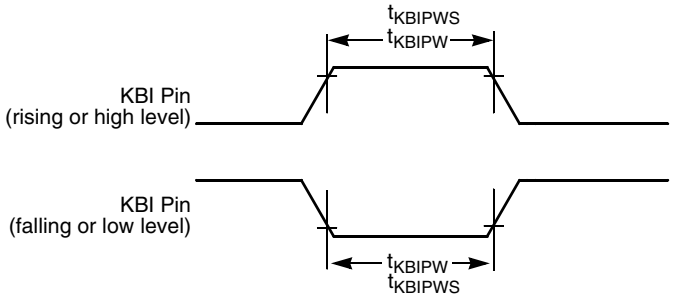
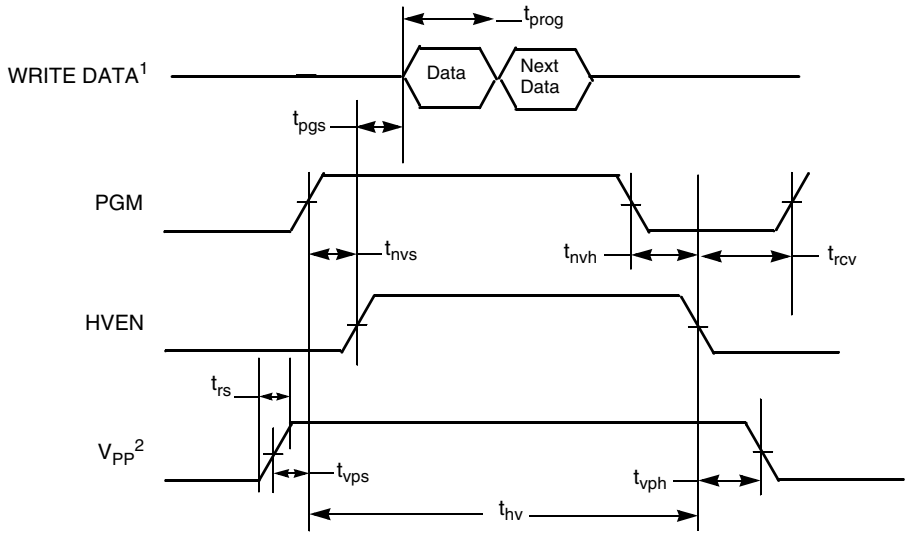
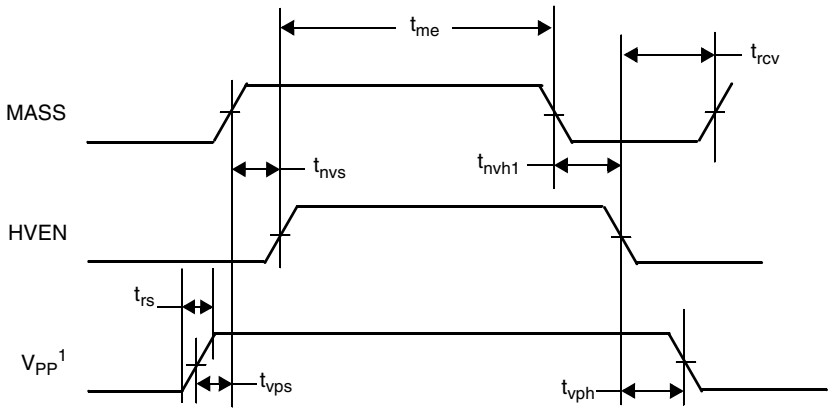


Figure 18. KBI Pulse Width



[1] Next Data applies if programming multiple bytes in a single row, refer to MC9RS08KA8 Series *Reference Manual*.
[2] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 23. Flash Program Timing



[1] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

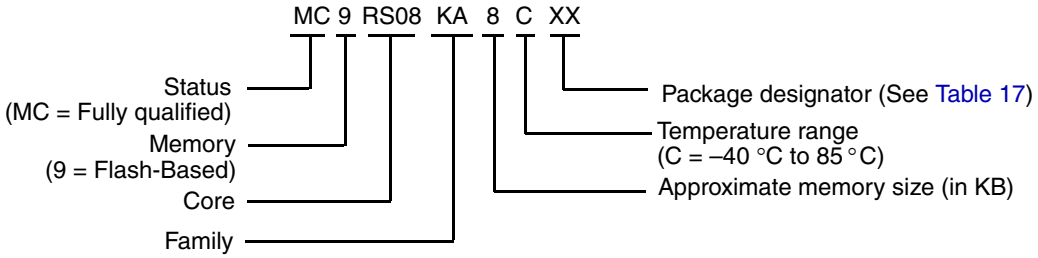
Figure 24. Flash Mass Erase Timing

4 Ordering Information

This section contains ordering numbers for MC9RS08KA8 series devices. See below for an example of the device numbering system.

Table 17. Device Numbering System

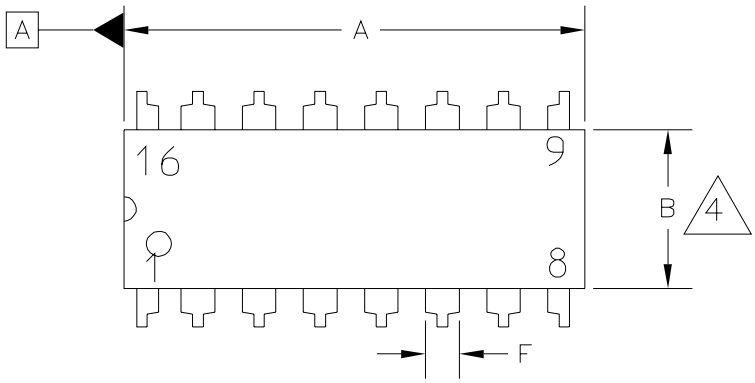
Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KA8 **MC9RS08KA4**	8K bytes 4K bytes	254 bytes 126 bytes	16 PDIP	PG	98ASB42431B
			16 W-SOIC	WG	98ASB42567B
			16 TSSOP	TG	98ASH70247A
			20 PDIP	PJ	98ASB42899B
			20 W-SOIC	WJ	98ASB42343B

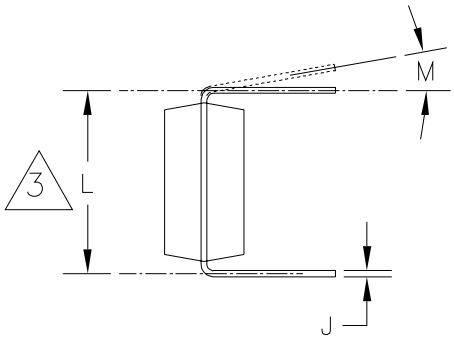


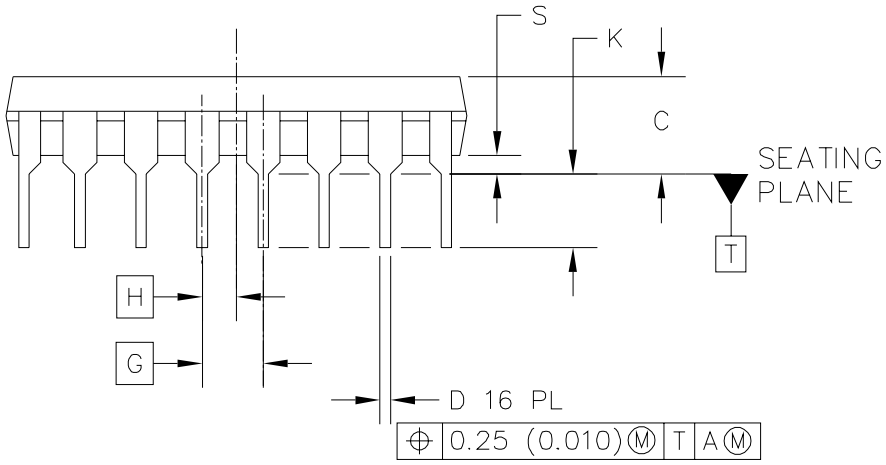
5 Mechanical Drawings

This following pages contain mechanical specifications for MC9RS08KA8 series package options.

- 16-pin PDIP (plastic dual in-line pin)
- 16-pin W-SOIC (wide body small outline integrated circuit)
- 16-pin TSSOP (thin shrink sSmall outline package)
- 20-pin PDIP (plastic dual in-line pin)
- 20-pin W-SOIC (wide body small outline integrated circuit)







MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42431B	REV: T
16 LD PDIP	CASE NUMBER: 648-08	19 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.55	0.740	0.770					
B	6.35	6.85	0.250	0.270					
C	3.69	4.44	0.145	0.175					
D	0.39	0.53	0.015	0.021					
F	1.02	1.77	0.040	0.070					
G	2.54 BSC		0.100 BSC						
H	1.27 BSC		0.050 BSC						
J	0.21	0.38	0.008	0.015					
K	2.80	3.30	0.110	0.130					
L	7.50	7.74	0.295	0.305					
M	0°	10°	0°	10°					
S	0.51	1.01	0.020	0.040					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

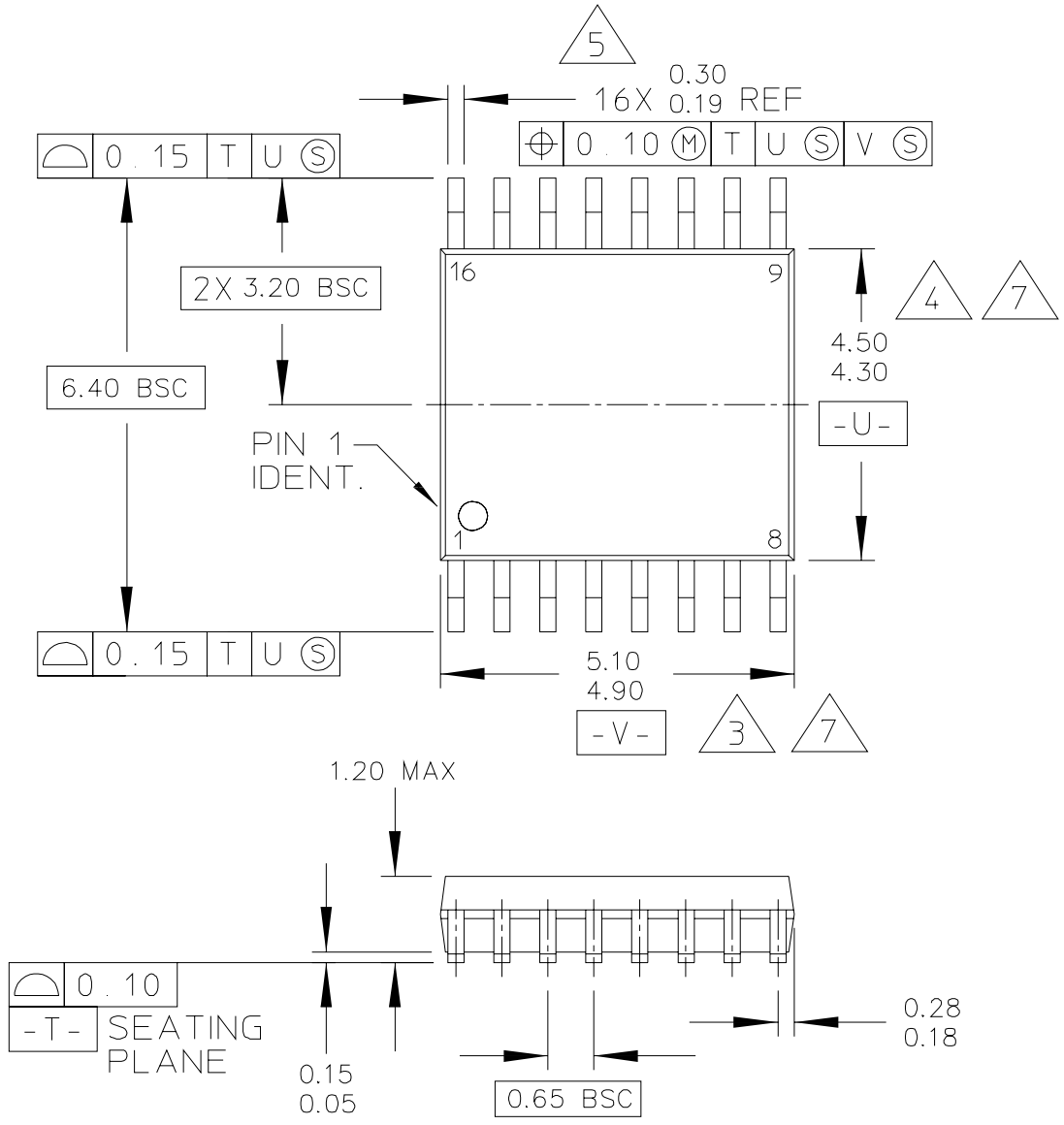
TITLE:

16 LD PDIP

DOCUMENT NO: 98ASB42431B | REV: T

CASE NUMBER: 648-08 | 19 MAY 2005

STANDARD: NON-JEDEC



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

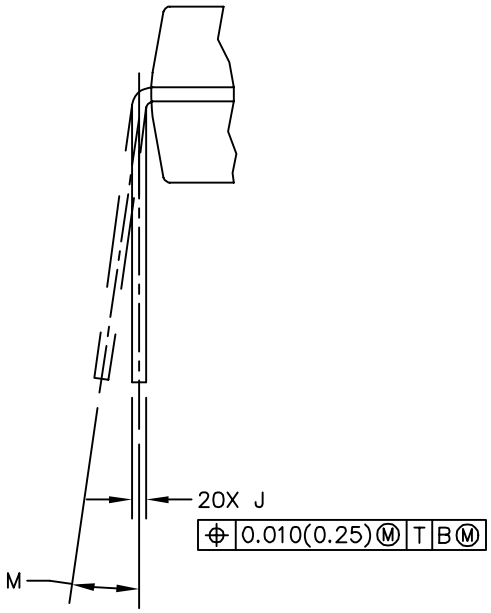
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	



VIEW D

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42899B	REV: B
20LD .300 PDIP	CASE NUMBER: 738C-01	24 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42343B	REV: J
20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751D–07	23 MAR 2005
	STANDARD: JEDEC MS–013AC	