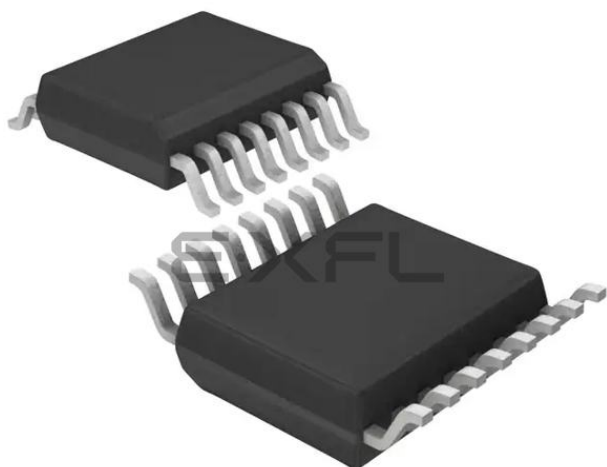




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	126 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08ka4ctgr

Table of Contents

1	MCU Block Diagram	3	3.9	AC Characteristics	18
2	Pin Assignments	3	3.9.1	Control Timing	19
3	Electrical Characteristics	5	3.9.2	TPM/MTIM Module Timing	20
3.1	Introduction	5	3.10	Analog Comparator (ACMP) Electrical	20
3.2	Parameter Classification	5	3.11	Internal Clock Source Characteristics	21
3.3	Absolute Maximum Ratings	6	3.12	ADC Characteristics	21
3.4	Thermal Characteristics	6	3.13	Flash Specifications	23
3.5	ESD Protection and Latch-Up Immunity	7	4	Ordering Information	26
3.6	DC Characteristics	8	5	Mechanical Drawings	26
3.7	Supply Current Characteristics	15			
3.8	External Oscillator (XOSC) Characteristics	18			

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	1/22/2008	Initial public release
2	10/7/2008	Updated Figure 4 and Figure 10 . Updated “How to Reach Us” information. Added 16-pin TSSOP package information.
3	11/4/2008	Updated operating voltage in Table 7 .
4	6/11/2009	Added output voltage of high drive at 5 V, $I_{load} = 10$ mA in the Table 7 .

Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9RS08KA8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9RS08KA8 MCU.

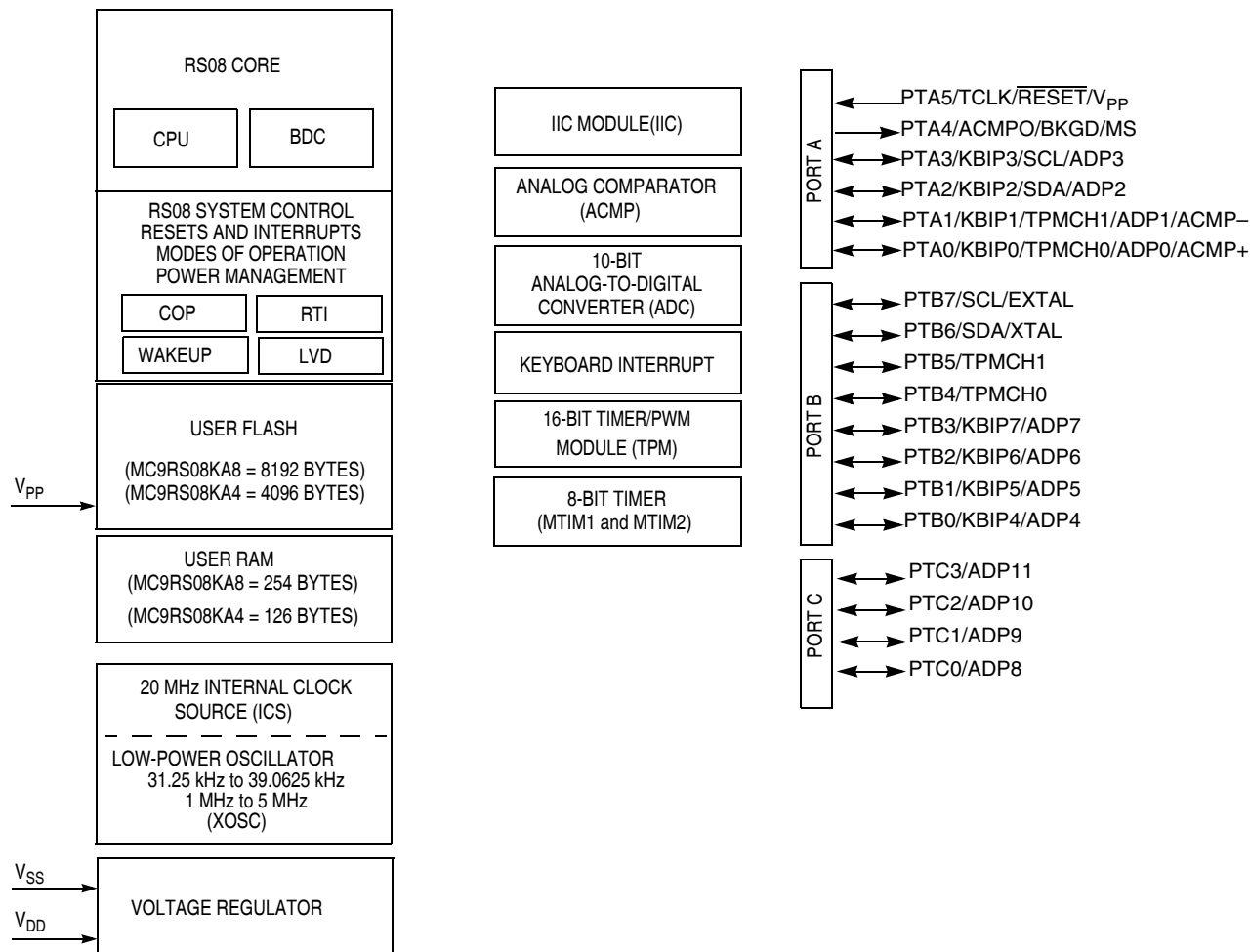


Figure 1. MC9RS08KA8 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KA8 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number		<-- Lowest Priority --> Highest				
20	16	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	PTA5		TCLK	RESET	V _{PP}
2	2	PTA4	ACMPO	BKGD	MS	
3	3					V _{DD}
4	4					V _{SS}
5	5	PTB7	SCL ¹			EXTAL
6	6	PTB6	SDA ¹			XTAL
7	7	PTB5	TPMCH1 ²			
8	8	PTB4	TPMCH0 ²			
9	—	PTC3			ADP11	
10	—	PTC2			ADP10	
11	—	PTC1			ADP9	
12	—	PTC0			ADP8	
13	9	PTB3	KBIP7		ADP7	
14	10	PTB2	KBIP6		ADP6	
15	11	PTB1	KBIP5		ADP5	
16	12	PTB0	KBIP4		ADP4	
17	13	PTA3	KBIP3	SCL ¹	ADP3	
18	14	PTA2	KBIP2	SDA ¹	ADP2	
19	15	PTA1	KBIP1	TPMCH1 ²	ADP1	ACMP–
20	16	PTA0	KBIP0	TPMCH0 ²	ADP0	ACMP+

¹ IIC pins can be remapped to PTA3 and PTA2

² TPM pins can be remapped to PTA0 and PTA1

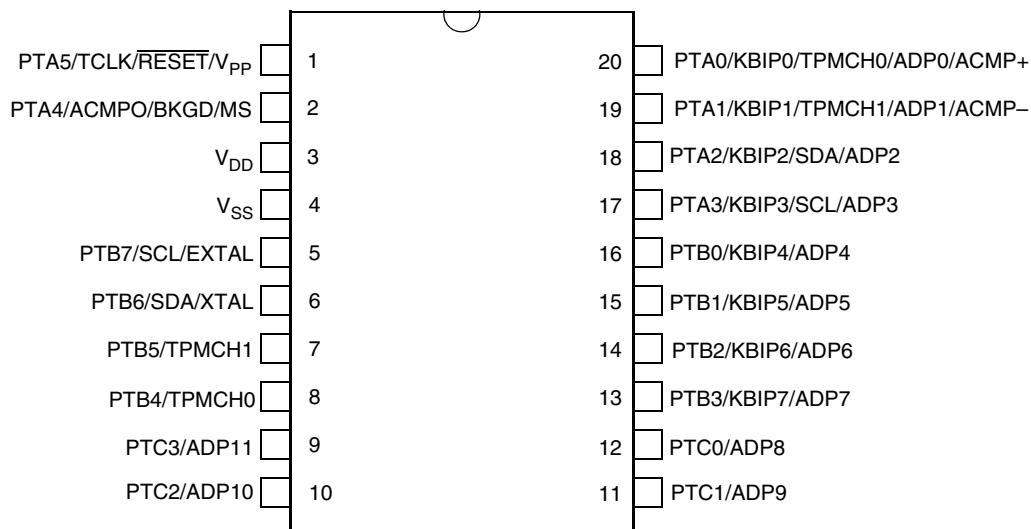


Figure 2. MC9RS08KA8 Series in 20-Pin PDIP/SOIC Package

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating ¹	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 500	—	V
4	Latch-up current at $T_A = 85^\circ\text{C}$ (applies to all pins except pin 9 PTC3/ADP11)	I_{LAT}	$\pm 100^2$	—	mA
	Latch-up current at $T_A = 85^\circ\text{C}$ (applies to pin 9 PTC3/ADP11)	I_{LAT}	$\pm 75^3$	—	mA

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

² These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of $\pm 100\text{mA}$.

³ This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to $\pm 75\text{mA}$. This pin is only present on 20 pin package types.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = -40 to 85°C Ambient)

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage (run, wait and stop modes.) $0 < f_{Bus} < 10\text{MHz}$ V_{DD} rising V_{DD} falling	V_{DD}	2.0 1.8	—	5.5	V
Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8 ¹	—	—	V
Low-voltage Detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.03	V
Power on RESET (POR) voltage	V_{POR}^1	0.9	—	1.7	V

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
Input high voltage ($V_{DD} > 2.3V$) (all digital inputs)	V_{IH}	$0.70 \times V_{DD}$	—	—	V
Input high voltage ($1.8V \leq V_{DD} \leq 2.3V$) (all digital inputs)	V_{IH}	$0.85 \times V_{DD}$	—	—	V
Input low voltage ($V_{DD} > 2.3V$) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
Input low voltage ($1.8V \leq V_{DD} \leq 2.3V$) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
Input hysteresis (all digital inputs)	V_{hys}^1	$0.06 \times V_{DD}$	—	—	V
Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input only pins	I_{In}	—	0.025	1.0	μA
High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input/output	I_{IOZ}	—	0.025	1.0	μA
Internal pullup resistors ² (all port pins)	R_{PU}	20	45	65	$k\Omega$
Internal pulldown resistors ² (all port pins except PTA5)	R_{PD}	20	45	65	$k\Omega$
PTA5 Internal pulldown resistor	—	45	—	95	$k\Omega$
Output high voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 2\text{ mA}$ 3 V, $I_{Load} = 1\text{ mA}$ 1.8 V, $I_{Load} = 0.5\text{ mA}$	V_{OH}	$V_{DD} - 0.8$	—	—	V
Output high voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 10\text{ mA}$ 5 V, $I_{Load} = 5\text{ mA}$ 3 V, $I_{Load} = 3\text{ mA}$ 1.8 V, $I_{Load} = 2\text{ mA}$		$V_{DD} - 0.8$	—	—	
Maximum total IOH for all port pins	I_{OHT}	—	—	40	mA
Output low voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 2\text{ mA}$ 3 V, $I_{Load} = 1\text{ mA}$ 1.8 V, $I_{Load} = 0.5\text{ mA}$	V_{OL}	—	—	0.8	V
Output low voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 10\text{ mA}$ 5 V, $I_{Load} = 5\text{ mA}$ 3 V, $I_{Load} = 3\text{ mA}$ 1.8 V, $I_{Load} = 2\text{ mA}$		—	—	0.8	
Maximum total IOL for all port pins	I_{OLT}	—	—	40	mA
DC injection current ^{3, 4, 5, 6} $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins		—	—	0.2 0.8	mA
Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

¹ This parameter is characterized and not tested on each device.

² Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

³ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{RESET}/V_{PP}$ which is internally clamped to V_{SS} only.

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁶ This parameter is characterized and not tested on each device.

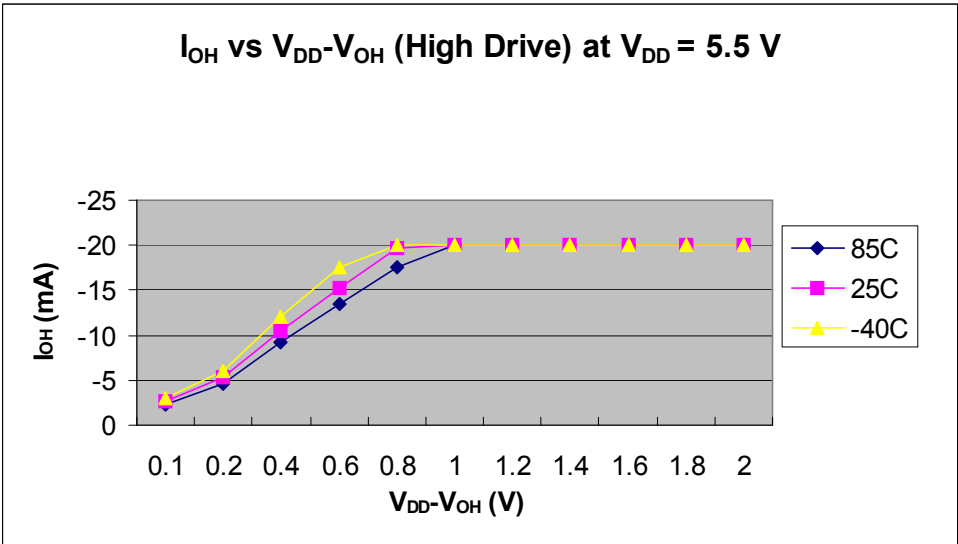


Figure 4. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 5.5\text{ V}$ (High Drive)

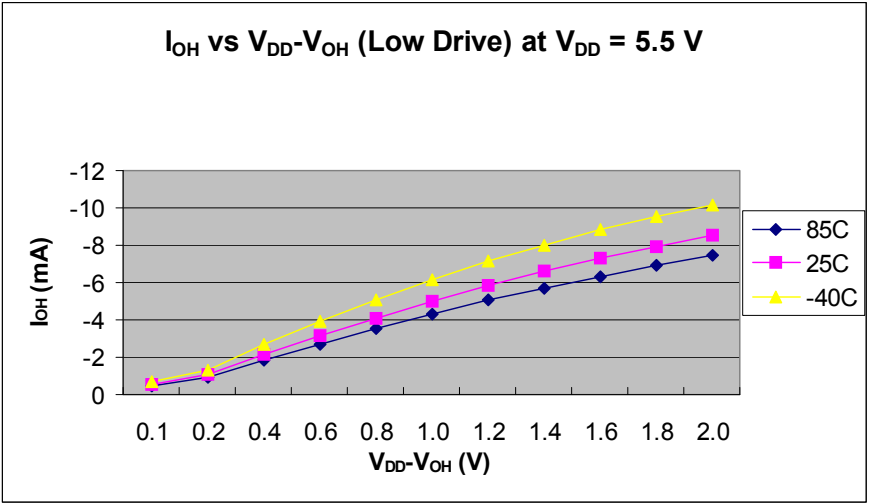


Figure 5. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 5.5\text{ V}$ (Low Drive)

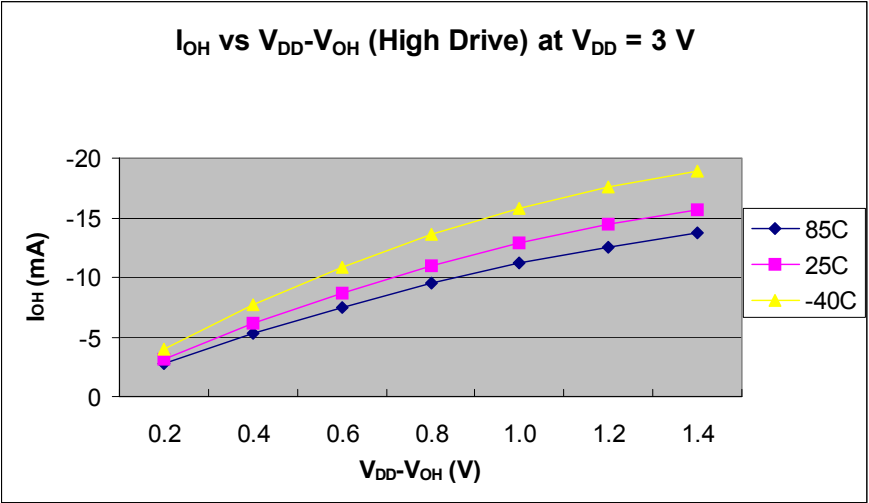


Figure 6. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 3$ V (High Drive)

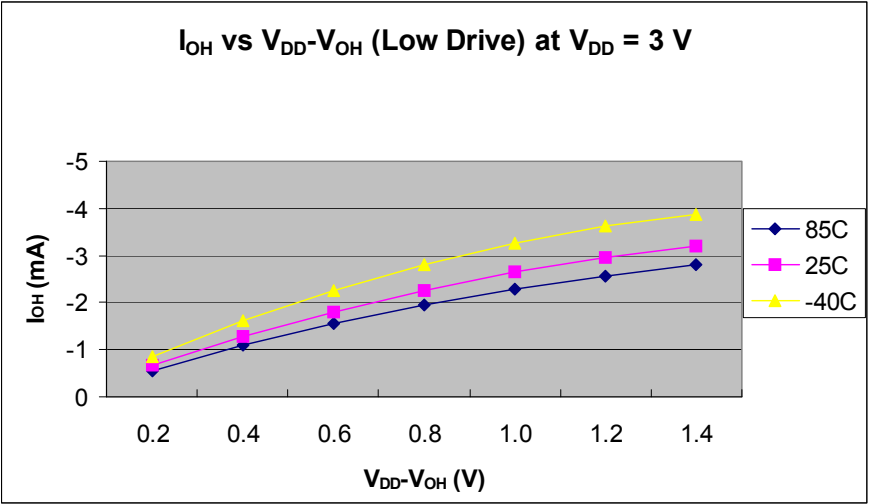
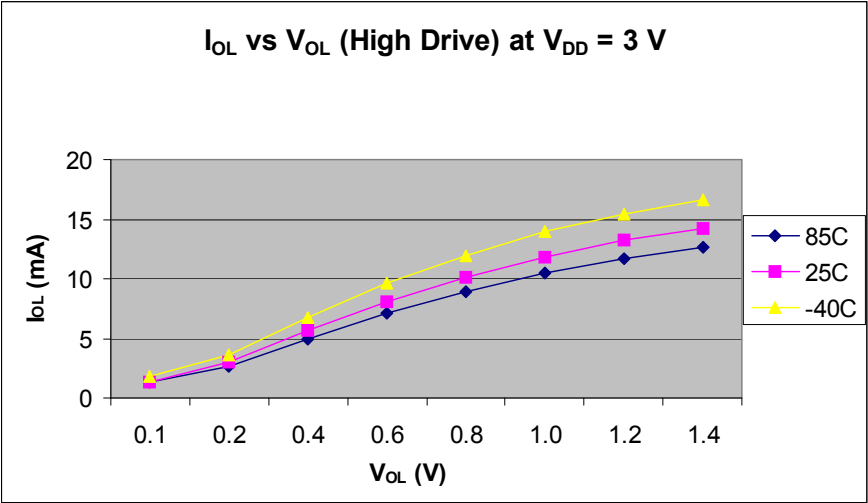
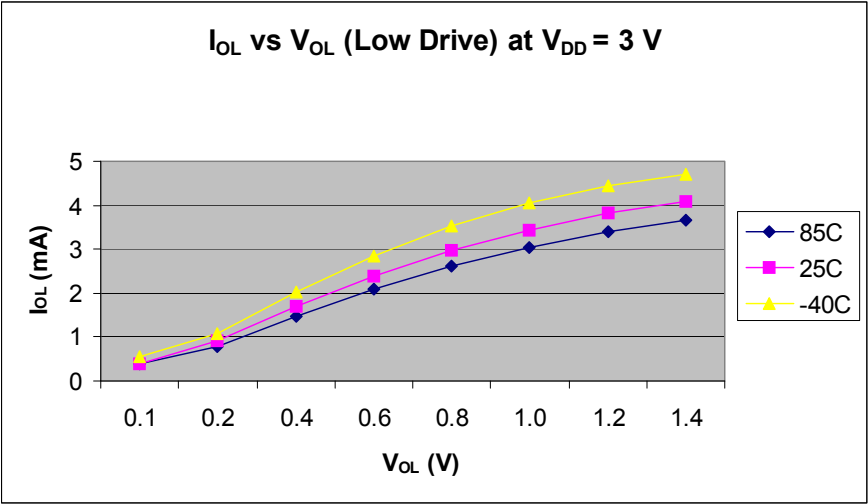


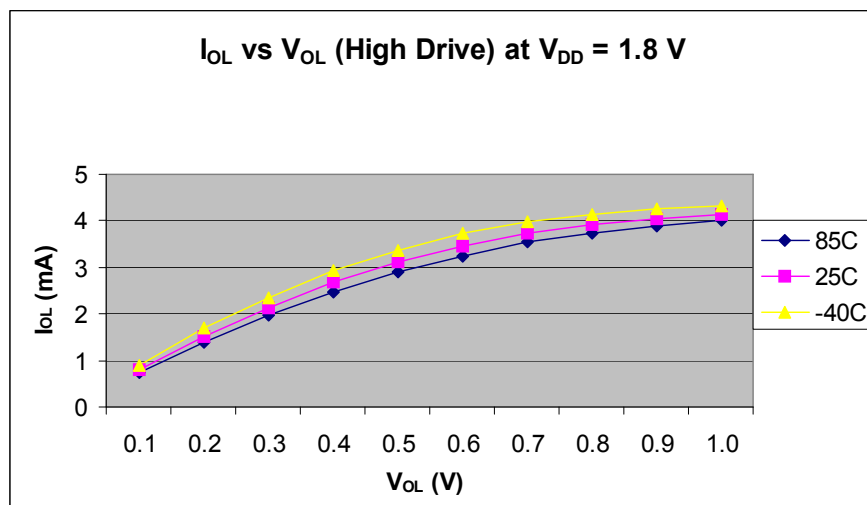
Figure 7. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 3$ V (Low Drive)



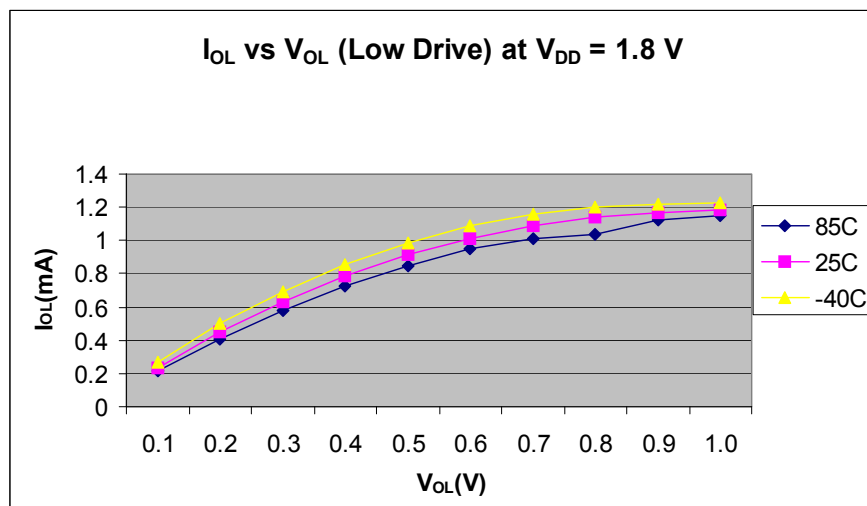
**Figure 12. Typical I_{OL} vs. $V_{DD}-V_{OL}$
 $V_{DD} = 3\text{ V}$ (High Drive)**



**Figure 13. Typical I_{OL} vs. $V_{DD}-V_{OL}$
 $V_{DD} = 3\text{ V}$ (Low Drive)**



**Figure 14. Typical I_{OL} vs. $V_{DD}-V_{OL}$
 $V_{DD} = 1.8$ V (High Drive)**



**Figure 15. Typical I_{OL} vs. $V_{DD}-V_{OL}$
 $V_{DD} = 1.8$ V (Low Drive)**

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

Parameter	Symbol	V_{DD} (V)	Typical ¹	Max ²	Temp. (°C)
Run supply current ³ measured at ($f_{Bus} = 10$ MHz)	R_{IDD10}	5	2.4 mA	5 mA	25 85
		3	2.4 mA	—	25 85
		1.80	1.7 mA	—	25 85

3.9.1 Control Timing

Table 10. Control Timing

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	0	—	10	MHz
2	D	Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	μs
3	D	External $\overline{RESET}$ pulse width ¹	t_{extrst}	150	—	—	ns
4	D	KBI pulse width ²	t_{KBIPW}	$1.5 t_{cyc}$	—	—	ns
5	D	KBI pulse width in stop ¹	t_{KBIPWS}	100	—	—	ns
6	D	Port rise and fall time (load = 50 pF) ³	t_{Rise}, t_{Fall}	—	11	—	ns
		Slew rate control disabled (PTxSE = 0)			35	—	
		Slew rate control enabled (PTxSE = 1)					

¹ This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

² This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

³ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40^{\circ}C$ to $85^{\circ}C$.

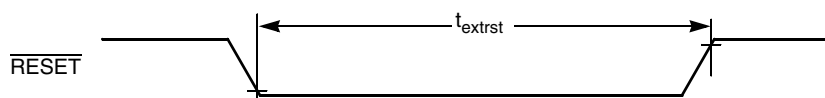


Figure 17. Reset Timing

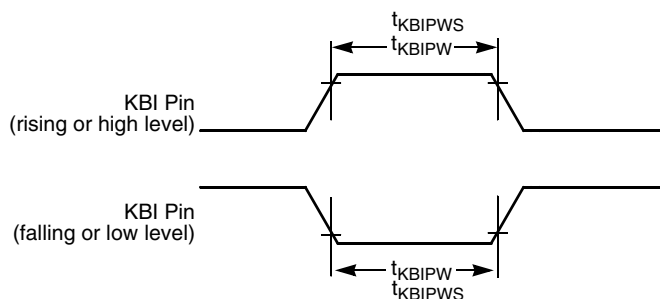


Figure 18. KBI Pulse Width

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{\text{Bus}}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

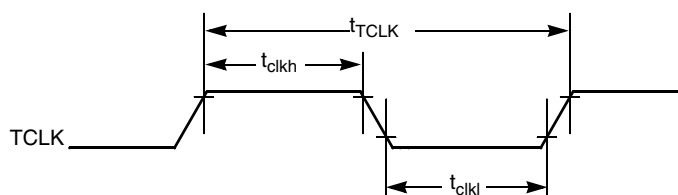


Figure 19. Timer External Clock

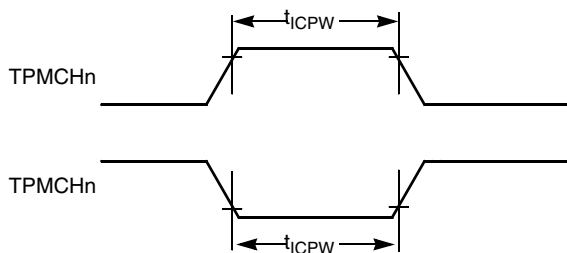


Figure 20. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage ¹	V_{AIN}	$V_{\text{SS}} - 0.3$	—	V_{DD}	V
4	P	Analog input offset voltage ¹	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis ¹	V_{H}	3.0	9.0	15.0	mV
6	C	Analog source impedance ¹	R_{AS}	—	—	10	$\text{k}\Omega$
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs

Table 12. Analog Comparator Electrical Specifications (continued)

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
9	P	Analog Comparator bandgap reference voltage	V_{BG}	1.1	1.208	1.3	V

¹ These data are characterized but not production tested.

3.11 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

Num	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	31.25	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	39.06	39.0625	kHz
3	C	DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
4	P	DCO output frequency range — trimmed	f_{dco_t}	16	20	20	MHz
5	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco_res_t}$	—	—	0.2	% f_{dco}
6	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	2	% f_{dco}
7	C	FLL acquisition time ^{2,3}	$t_{acquire}$	—	—	1	ms
8	C	Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	t_{wakeup}	—	100 86	—	μ s

¹ Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

² This parameter is characterized and not tested on each device.

³ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.12 ADC Characteristics

Table 14. 5 Volt 10-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min.	Typical	Max.	Unit
D	Input voltage	—	V_{ADIN}	V_{SS}	—	V_{DD}	V
C	Accuracy	$V_{DD} = 2$ V	—	—	8 bit	—	—
C	Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF
C	Input resistance	—	R_{ADIN}	—	3	5	k Ω
C	Analog source resistance external to MCU	10 bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz	R_{AS}	— —	— —	5 10	k Ω
		8 bit mode (all valid f_{ADCK})		—	—	10	

Table 14. 5 Volt 10-bit ADC Operating Conditions (continued)

C	Characteristic	Conditions	Symb	Min.	Typical	Max.	Unit
D	ADC conversion clock frequency	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz
		Low Power (ADLPC=1)		0.4	—	8.0	

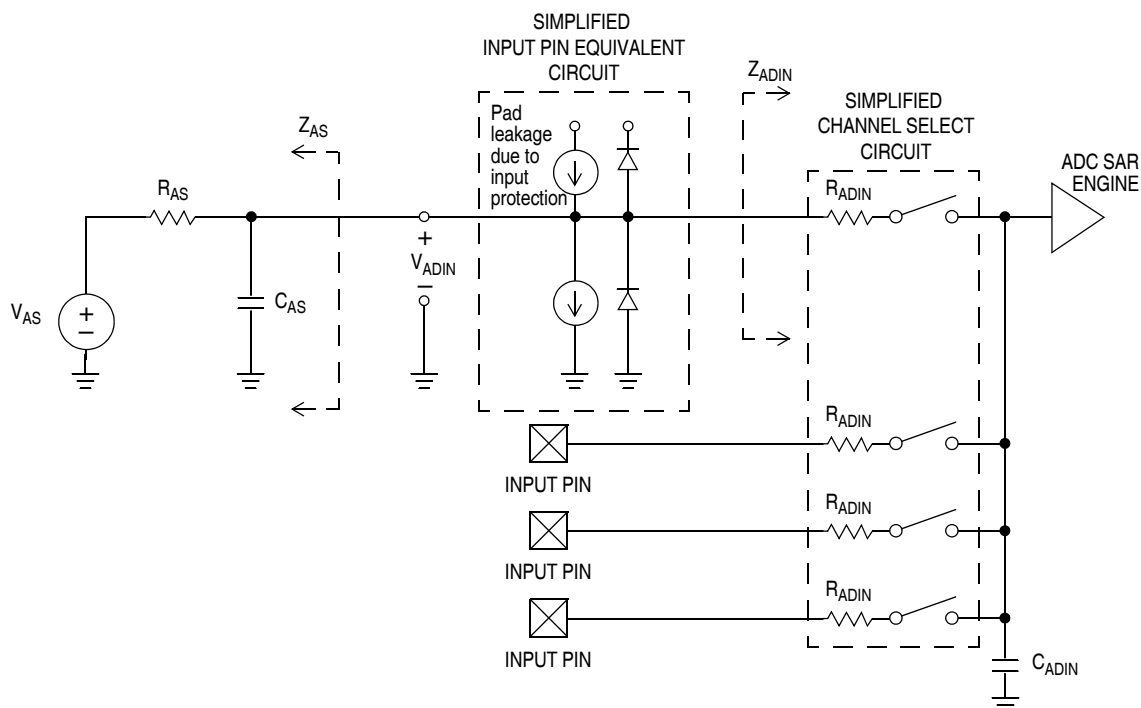


Figure 21. ADC Input Impedance Equivalency Diagram

Table 15. 10-bit ADC Characteristics

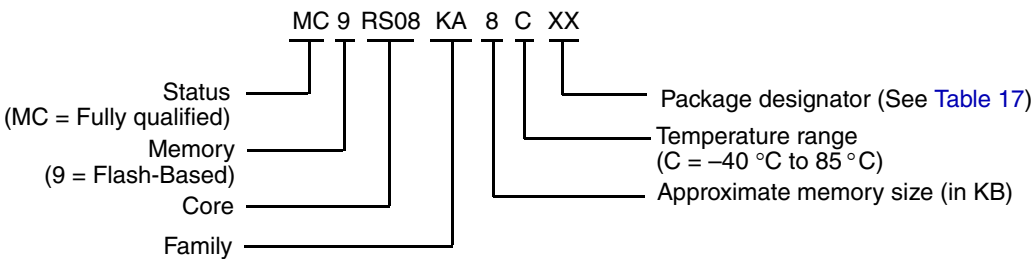
Characteristic	Conditions	C	Symb	Min	Typical ¹	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	T	I_{DDAD}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	T	I_{DDAD}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	T	I_{DDAD}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	C	I_{DDAD}	—	0.582	1	mA

4 Ordering Information

This section contains ordering numbers for MC9RS08KA8 series devices. See below for an example of the device numbering system.

Table 17. Device Numbering System

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KA8 MC9RS08KA4	8K bytes 4K bytes	254 bytes 126 bytes	16 PDIP	PG	98ASB42431B
			16 W-SOIC	WG	98ASB42567B
			16 TSSOP	TG	98ASH70247A
			20 PDIP	PJ	98ASB42899B
			20 W-SOIC	WJ	98ASB42343B



5 Mechanical Drawings

This following pages contain mechanical specifications for MC9RS08KA8 series package options.

- 16-pin PDIP (plastic dual in-line pin)
- 16-pin W-SOIC (wide body small outline integrated circuit)
- 16-pin TSSOP (thin shrink sSmall outline package)
- 20-pin PDIP (plastic dual in-line pin)
- 20-pin W-SOIC (wide body small outline integrated circuit)



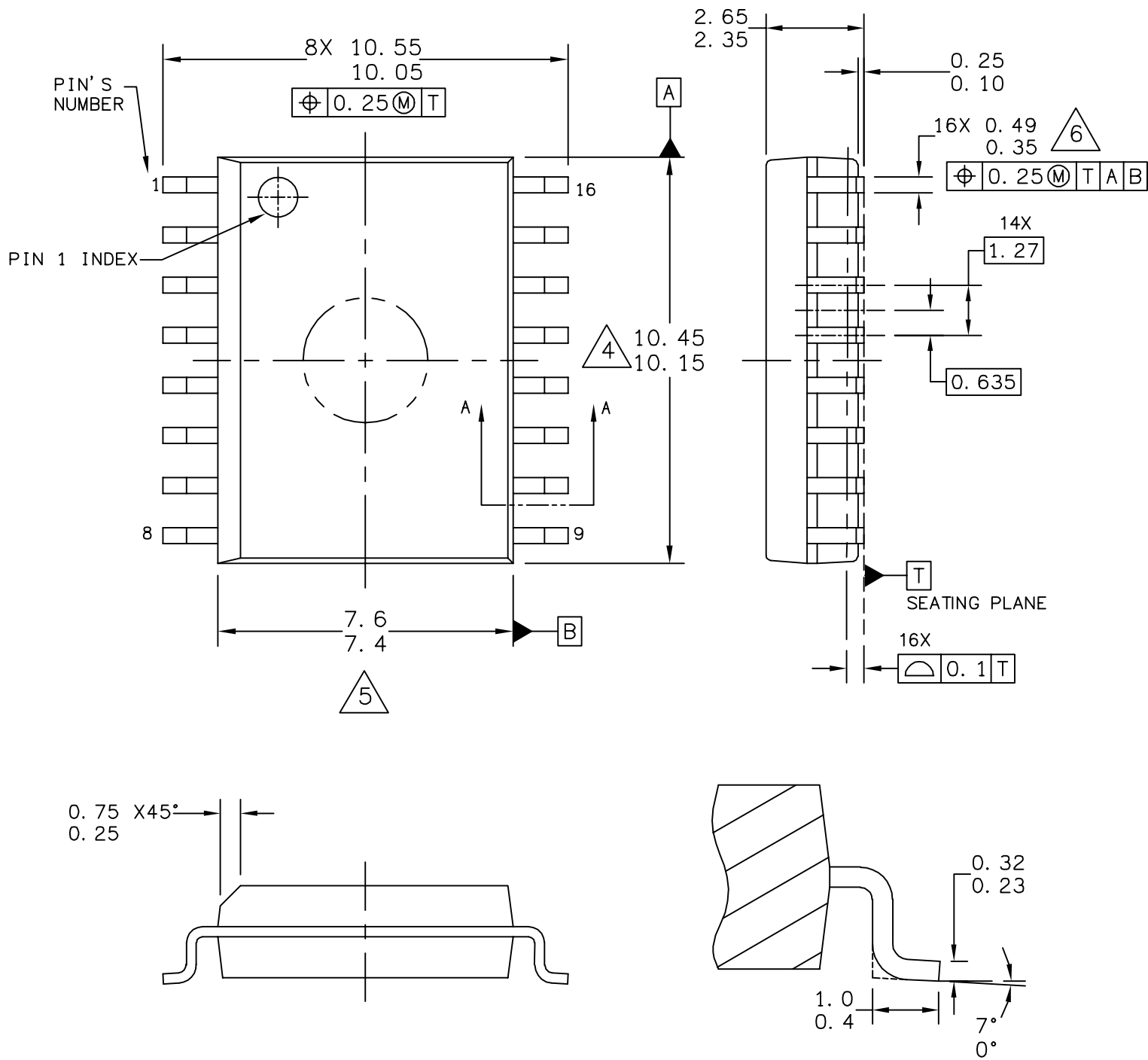
STYLE 1:

- PIN 1. CATHODE
- 2. CATHODE
- 3. CATHODE
- 4. CATHODE
- 5. CATHODE
- 6. CATHODE
- 7. CATHODE
- 8. CATHODE
- 9. ANODE
- 10. ANODE
- 11. ANODE
- 12. ANODE
- 13. ANODE
- 14. ANODE
- 15. ANODE
- 16. ANODE

STYLE 2:

- PIN 1. COMMON DRAIN
- 2. COMMON DRAIN
- 3. COMMON DRAIN
- 4. COMMON DRAIN
- 5. COMMON DRAIN
- 6. COMMON DRAIN
- 7. COMMON DRAIN
- 8. COMMON DRAIN
- 9. GATE
- 10. SOURCE
- 11. GATE
- 12. SOURCE
- 13. GATE
- 14. SOURCE
- 15. GATE
- 16. SOURCE

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: 16 LD PDIP			DOCUMENT NO: 98ASB42431B		REV: T
			CASE NUMBER: 648-08		19 MAY 2005
			STANDARD: NON-JEDEC		



SECTION A-A

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 16LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42567B		REV: F
	CASE NUMBER: 751G-04		02 JUN 2005
	STANDARD: JEDEC MS-013AA		



NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
- 3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: 16LD SOIC W/B, 1.27 PITCH, CASE OUTLINE			DOCUMENT NO: 98ASB42567B		REV: F
			CASE NUMBER: 751G–04		02 JUN 2005
			STANDARD: JEDEC MS–013AA		



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

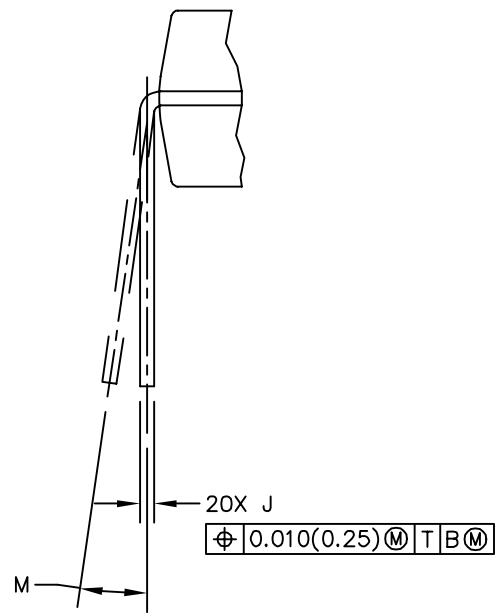
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A		REV: B
	CASE NUMBER: 948F-01		19 MAY 2005
	STANDARD: JEDEC		



VIEW D

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: 20LD .300 PDIP			DOCUMENT NO: 98ASB42899B		REV: B
			CASE NUMBER: 738C-01		24 MAY 2005
			STANDARD: NON-JEDEC		

