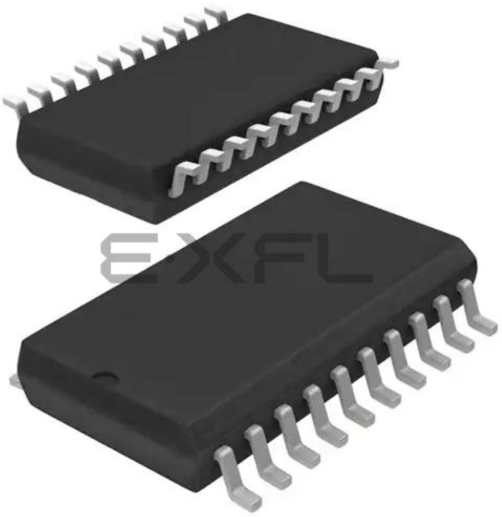


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	126 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08ka4cwj

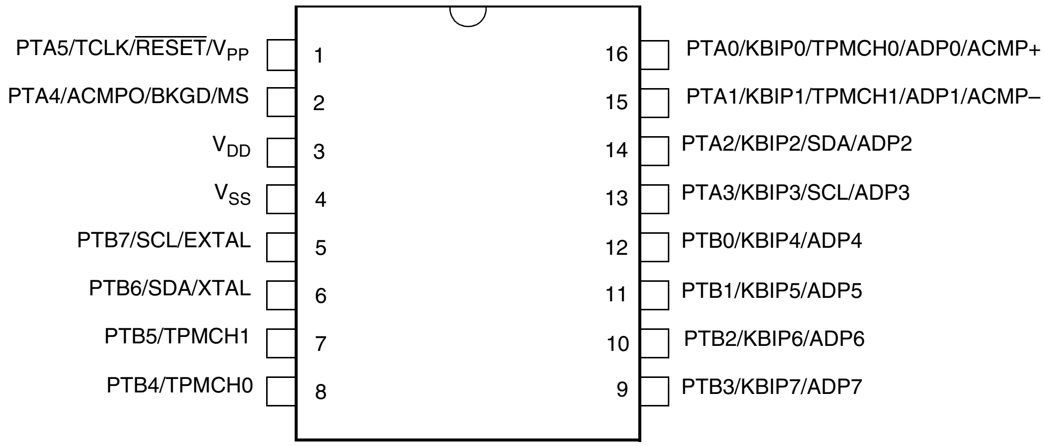


Figure 3. MC9RS08KA8 Series in 16-Pin PDIP/SOIC/TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KA8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 4. Thermal Characteristics (continued)

Rating	Symbol	Value	Unit
Thermal resistance 16-pin TSSOP	θ_{JA}	75	°C/W
Thermal resistance 20-pin PDIP	θ_{JA}	75	°C/W
Thermal resistance 20-pin SOIC	θ_{JA}	96	°C/W

The average chip-junction temperature (TJ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between PD and TJ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (PD)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
Input high voltage (V_{DD} > 2.3V) (all digital inputs)	V_{IH}	$0.70 \times V_{DD}$	—	—	V
Input high voltage (1.8 V $\leq V_{DD} \leq$ 2.3 V) (all digital inputs)	V_{IH}	$0.85 \times V_{DD}$	—	—	V
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
Input low voltage (1.8 V $\leq V_{DD} \leq$ 2.3 V) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
Input hysteresis (all digital inputs)	V_{hys}[1]	$0.06 \times V_{DD}$	—	—	V
Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input only pins	$\|I_{In}\|$	—	0.025	1.0	μA
High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input/output	$\|I_{OZ}\|$	—	0.025	1.0	μA
Internal pullup resistors[2](all port pins)	R_{PU}	20	45	65	kΩ
Internal pulldown resistors[2](all port pins except PTA5)	R_{PD}	20	45	65	kΩ
PTA5 Internal pulldown resistor	—	45	—	95	kΩ
Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OH}	$V_{DD} - 0.8$	— — —	— — —	V
Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		$V_{DD} - 0.8$	— — — —	— — — —	
Maximum total I_{OH} for all port pins	$\|I_{OHT}\|$	—	—	40	mA
Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OL}	— — —	— — —	0.8	V
Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		— — — —	— — — —	0.8	
Maximum total I_{OL} for all port pins	I_{OLT}	—	—	40	mA
DC injection current[3, 4, 5 ,6] $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins		— —	— —	0.2 0.8	mA
Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 This parameter is characterized and not tested on each device.

2 Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ which is internally clamped to V_{SS} only.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 This parameter is characterized and not tested on each device.

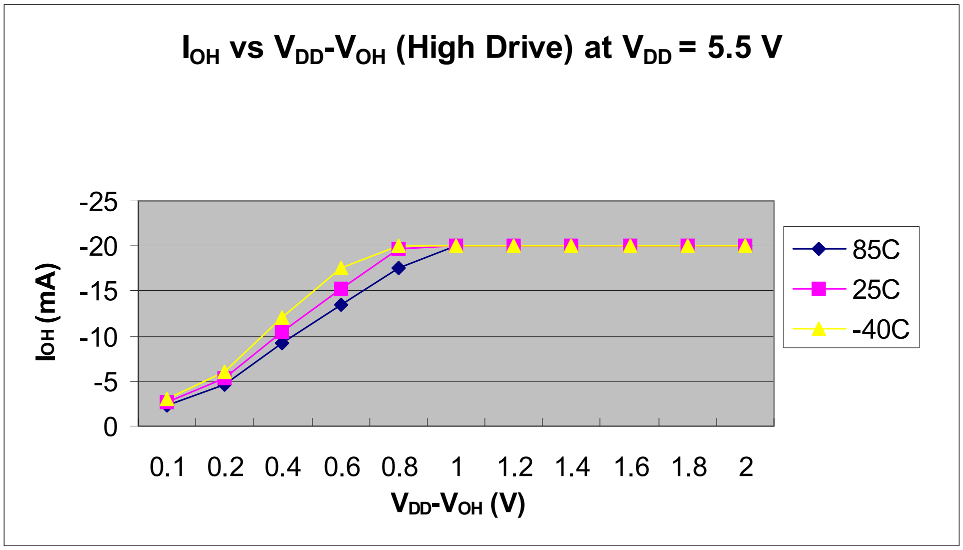


Figure 4. Typical I_{OH} vs. $V_{DD}–V_{OH}$
V_{DD} = 5.5 V (High Drive)

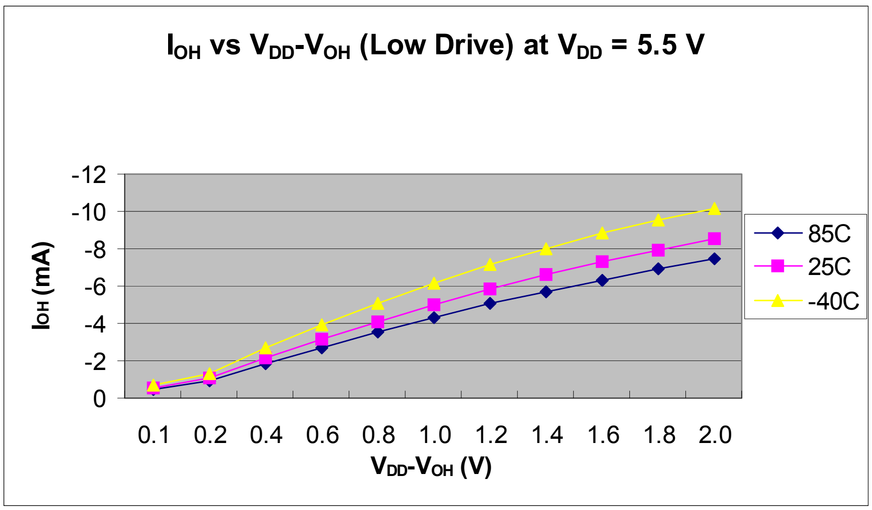


Figure 5. Typical I_{OH} vs. $V_{DD}–V_{OH}$
V_{DD} = 5.5 V (Low Drive)

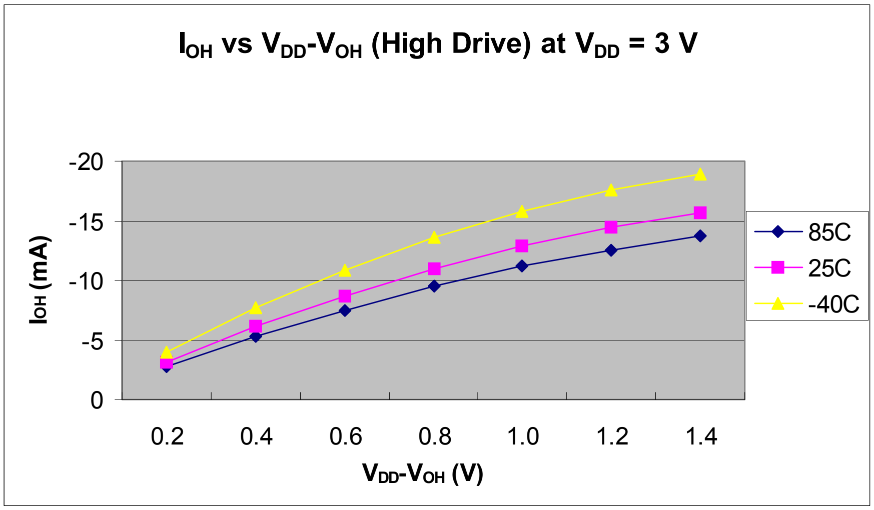


Figure 6. Typical I_{OH} vs. $V_{DD}–V_{OH}$
V_{DD} = 3 V (High Drive)

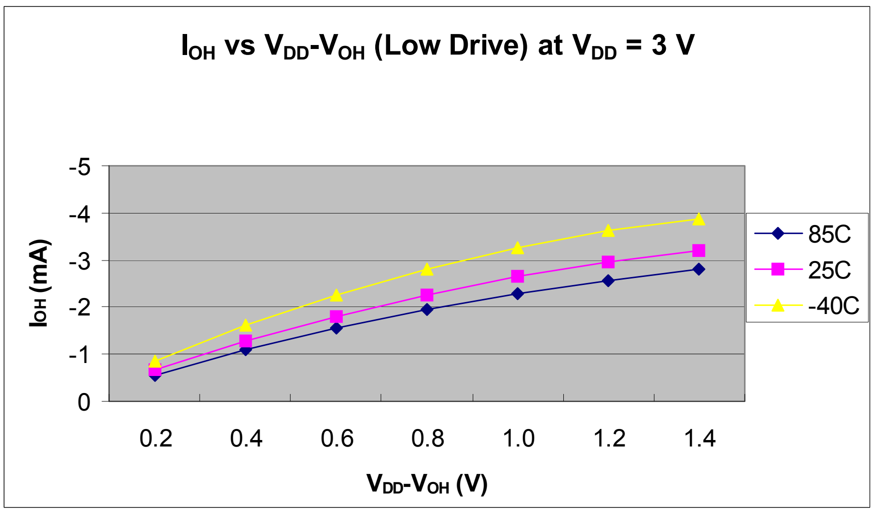


Figure 7. Typical I_{OH} vs. $V_{DD}–V_{OH}$
V_{DD} = 3 V (Low Drive)

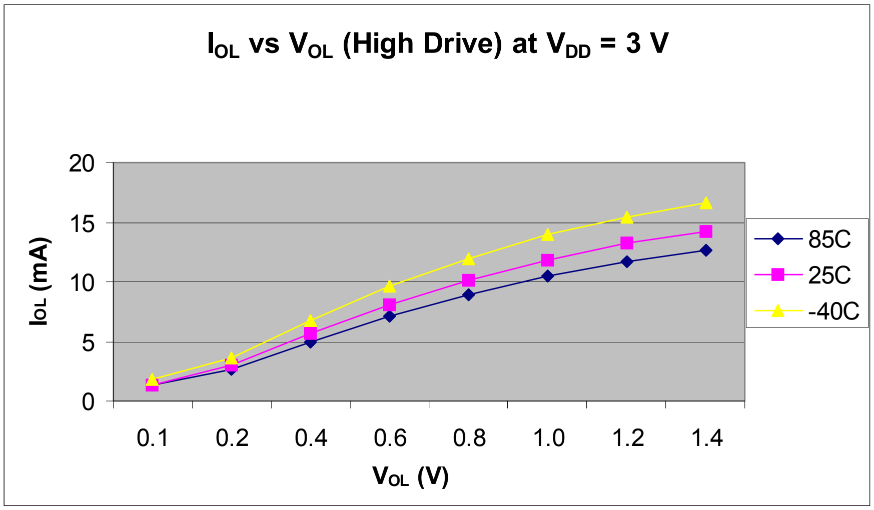


Figure 12. Typical I_{OL} vs. V_{DD}–V_{OL}
V_{DD} = 3 V (High Drive)

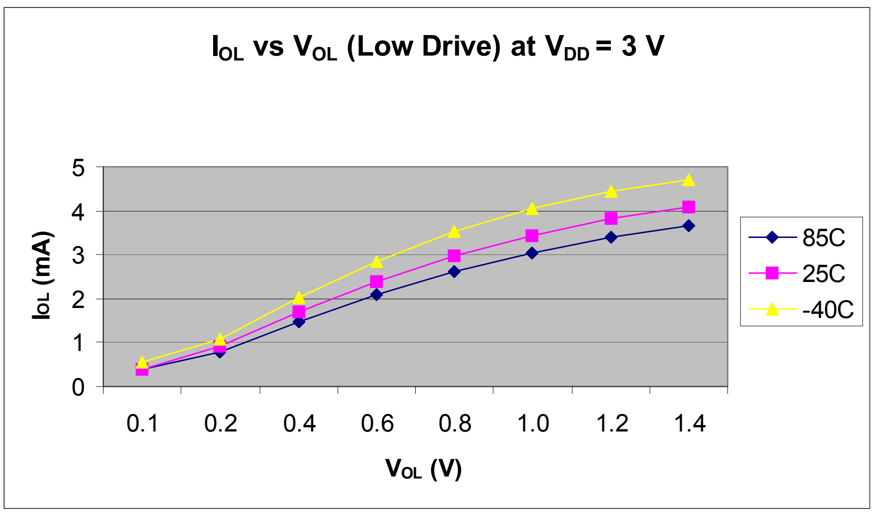


Figure 13. Typical I_{OL} vs. V_{DD}–V_{OL}
V_{DD} = 3 V (Low Drive)

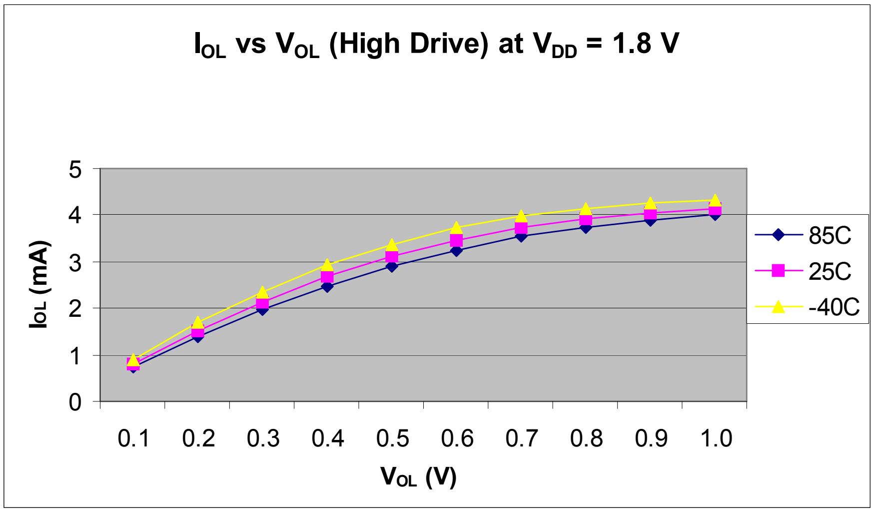


Figure 14. Typical I_{OL} vs. V_{DD}–V_{OL}
V_{DD} = 1.8 V (High Drive)

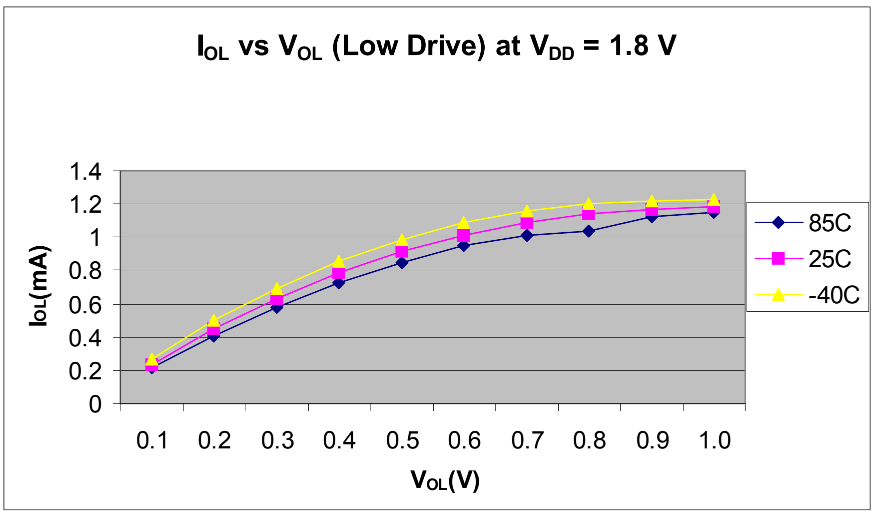


Figure 15. Typical I_{OL} vs. V_{DD}–V_{OL}
V_{DD} = 1.8 V (Low Drive)

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
Run supply current[3] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	2.4 mA	5 mA	25 85
		3	2.4 mA	—	25 85
		1.80	1.7 mA	—	25 85

[5] Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 1.3 mA at 3 V and 1 mA at 2 V with f_{Bus} = 1 MHz.

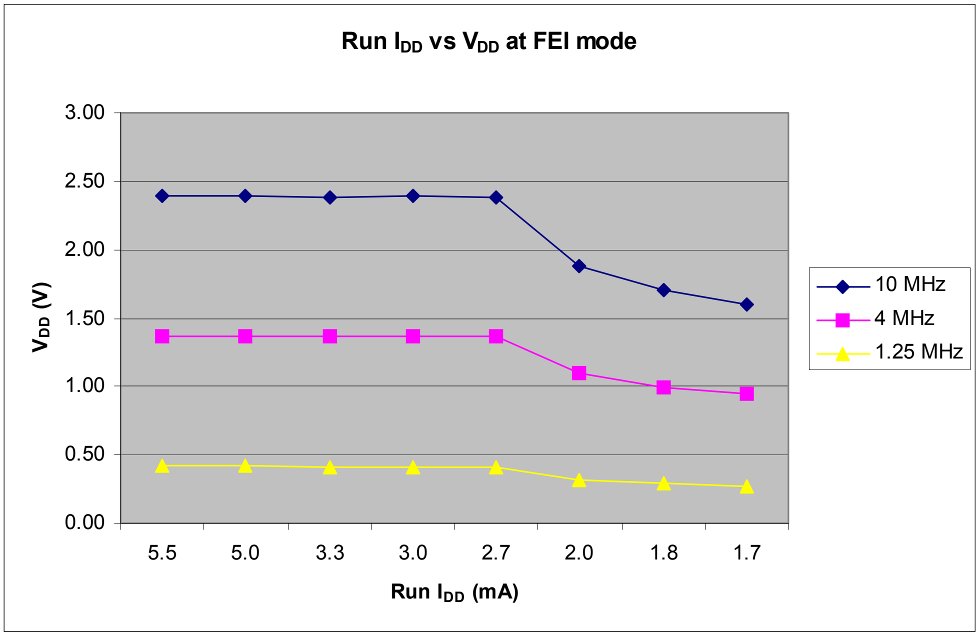


Figure 16. Typical Run I_{DD} vs. V_{DD} for FEI Mode

3.9.1 Control Timing

Table 10. Control Timing

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	0	—	10	MHz
2	D	Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	µs
3	D	External $\overline{\text{RESET}}$ pulse width[1]	t_{extrst}	150	—	—	ns
4	D	KBI pulse width[2]	t_{KBIPW}	1.5 t_{cyc}	—	—	ns
5	D	KBI pulse width in stop[1]	t_{KBIPWS}	100	—	—	ns
6	D	Port rise and fall time (load = 50 pF)[3] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	— —	ns

1 This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

2 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

3 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

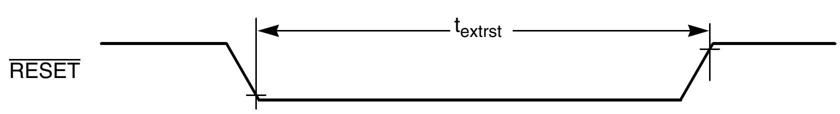


Figure 17. Reset Timing

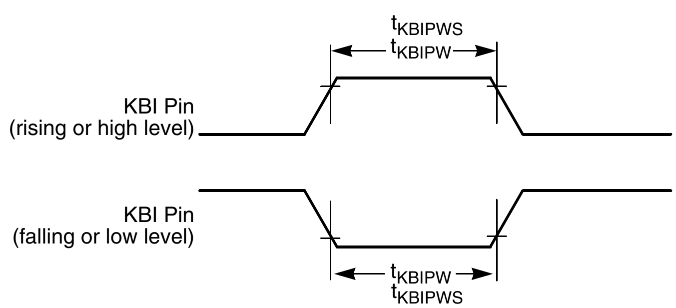


Figure 18. KBI Pulse Width

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

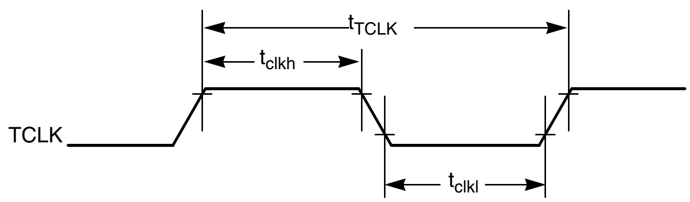


Figure 19. Timer External Clock

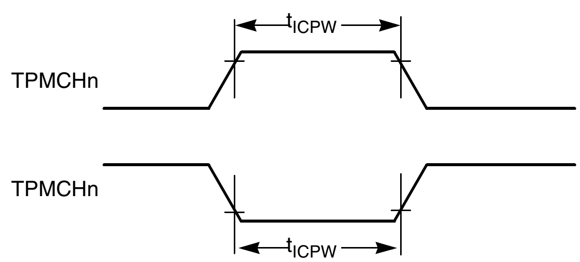


Figure 20. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage[1]	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4	P	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	kΩ
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs

Table 14. 5 Volt 10-bit ADC Operating Conditions (continued)

C	Characteristic	Conditions	Symb	Min.	Typical	Max.	Unit
D	ADC conversion clock frequency	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz
		Low Power (ADLPC=1)		0.4	—	8.0	

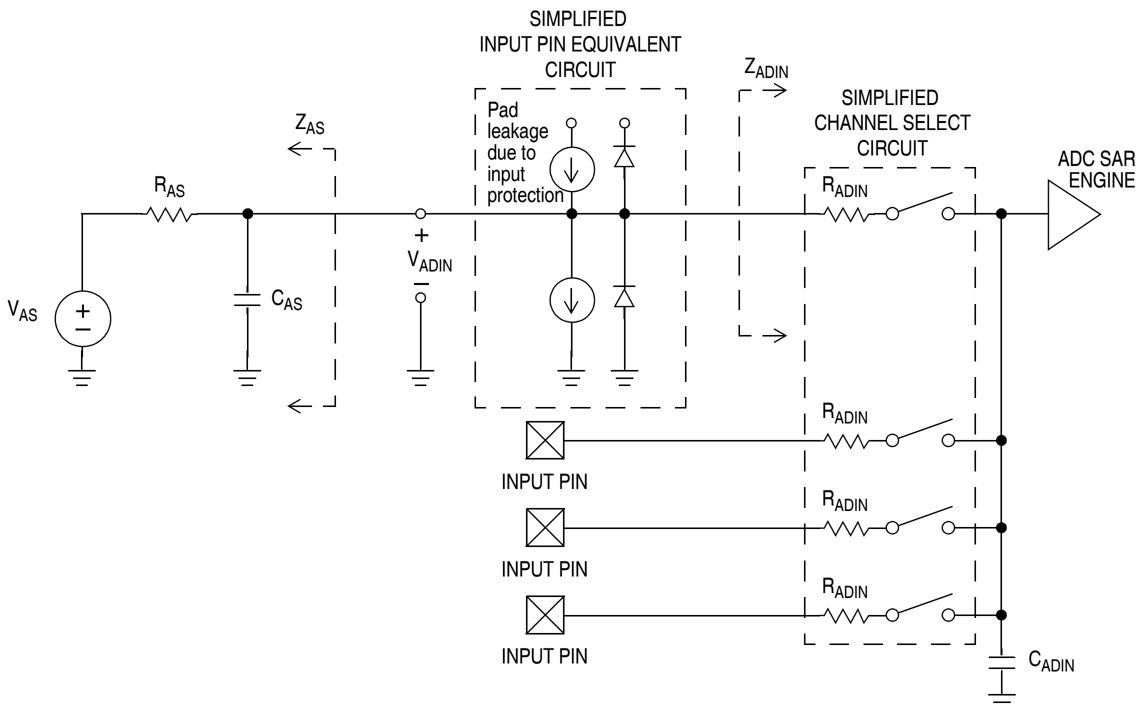
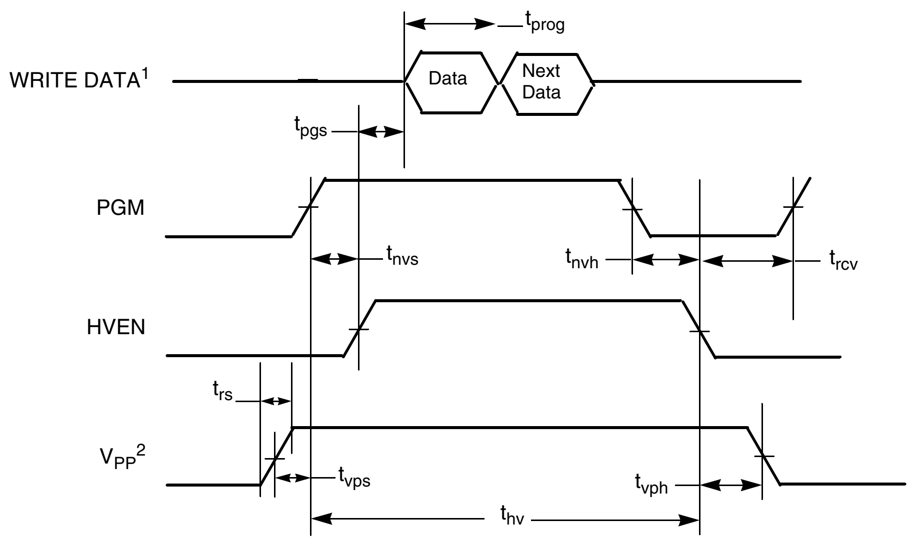


Figure 21. ADC Input Impedance Equivalency Diagram

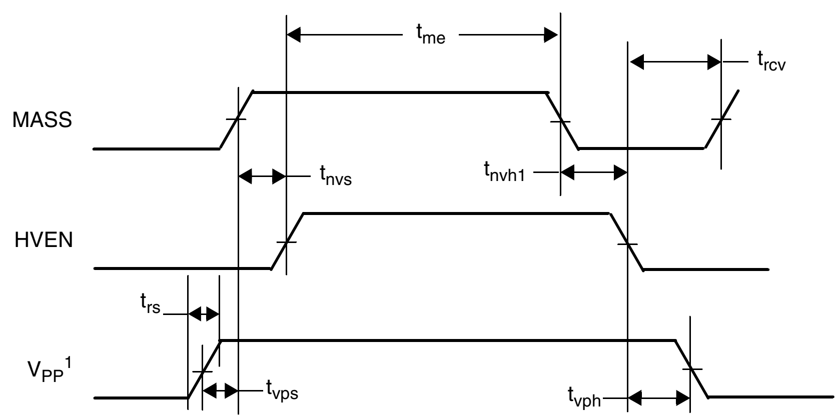
Table 15. 10-bit ADC Characteristics

Characteristic	Conditions	C	Symb	Min	Typical[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	T	I_{DDAD}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	T	I_{DDAD}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	T	I_{DDAD}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	C	I_{DDAD}	—	0.582	1	mA



[1] Next Data applies if programming multiple bytes in a single row, refer to MC9RS08KA8 Series *Reference Manual*.
[2] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 23. Flash Program Timing



[1] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

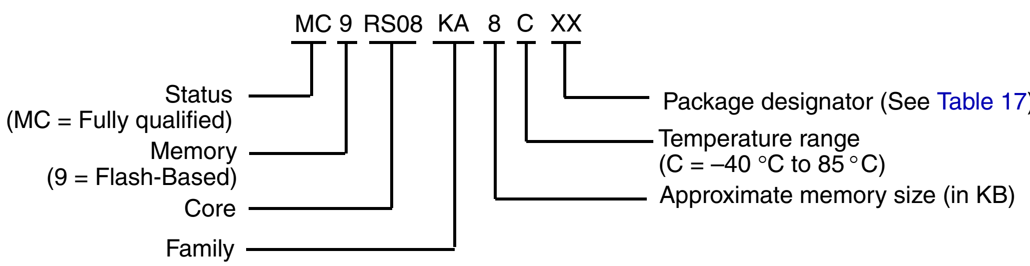
Figure 24. Flash Mass Erase Timing

4 Ordering Information

This section contains ordering numbers for MC9RS08KA8 series devices. See below for an example of the device numbering system.

Table 17. Device Numbering System

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KA8 **MC9RS08KA4**	8K bytes 4K bytes	254 bytes 126 bytes	16 PDIP	PG	98ASB42431B
			16 W-SOIC	WG	98ASB42567B
			16 TSSOP	TG	98ASH70247A
			20 PDIP	PJ	98ASB42899B
			20 W-SOIC	WJ	98ASB42343B



5 Mechanical Drawings

This following pages contain mechanical specifications for MC9RS08KA8 series package options.

- 16-pin PDIP (plastic dual in-line pin)
- 16-pin W-SOIC (wide body small outline integrated circuit)
- 16-pin TSSOP (thin shrink sSmall outline package)
- 20-pin PDIP (plastic dual in-line pin)
- 20-pin W-SOIC (wide body small outline integrated circuit)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

DIM	MILLIMETERS		INCHES		DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770					
B	6.35	6.85	0.250	0.270					
C	3.69	4.44	0.145	0.175					
D	0.39	0.53	0.015	0.021					
F	1.02	1.77	0.040	0.070					
G	2.54 BSC		0.100 BSC						
H	1.27 BSC		0.050 BSC						
J	0.21	0.38	0.008	0.015					
K	2.80	3.30	0.110	0.130					
L	7.50	7.74	0.295	0.305					
M	0°	10°	0°	10°					
S	0.51	1.01	0.020	0.040					

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

16 LD PDIP

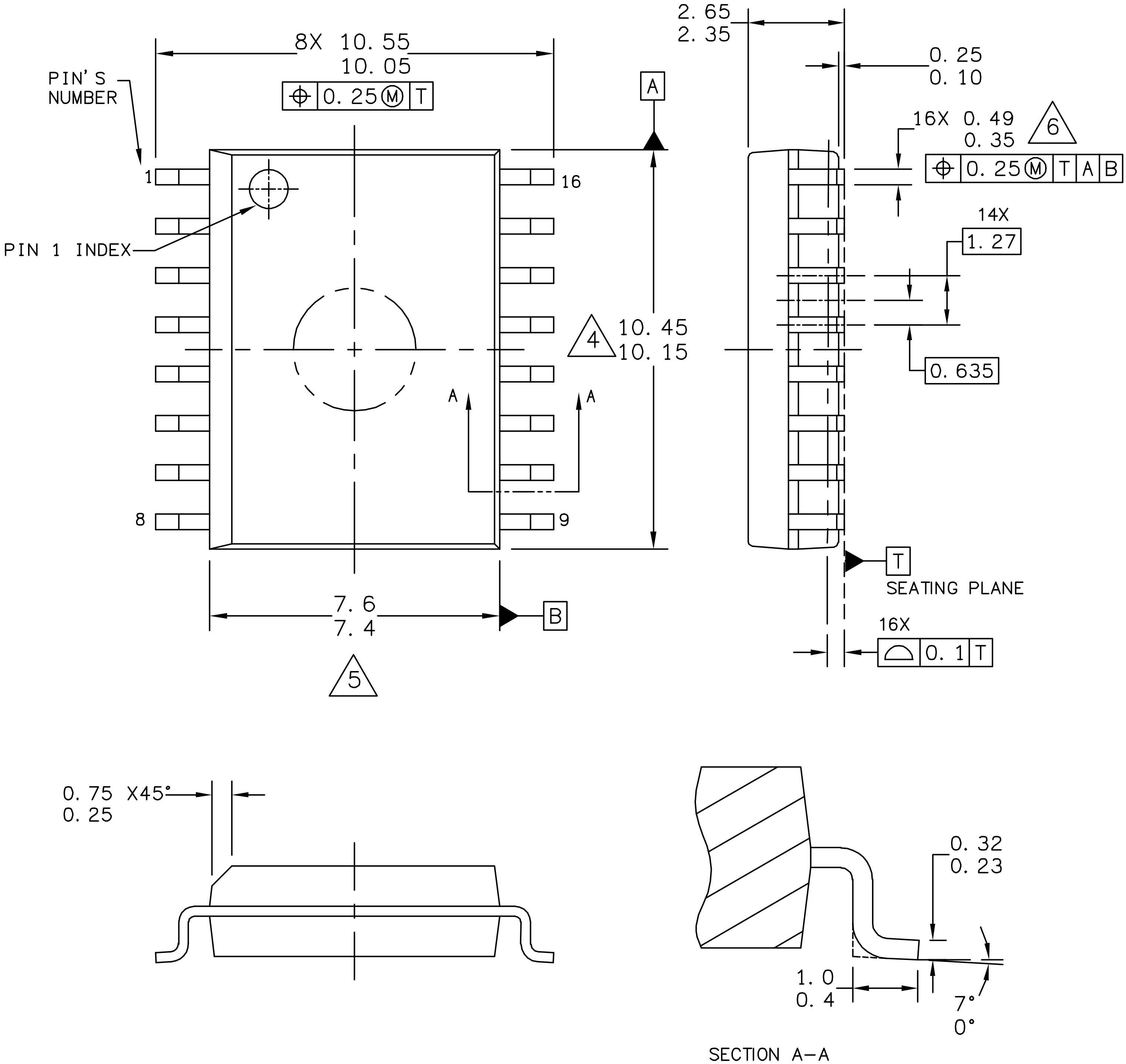
DOCUMENT NO: 98ASB42431B

REV: T

CASE NUMBER: 648-08

19 MAY 2005

STANDARD: NON-JEDEC



	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 16LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42567B	REV: F
	CASE NUMBER: 751G-04	02 JUN 2005
	STANDARD: JEDEC MS-013AA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

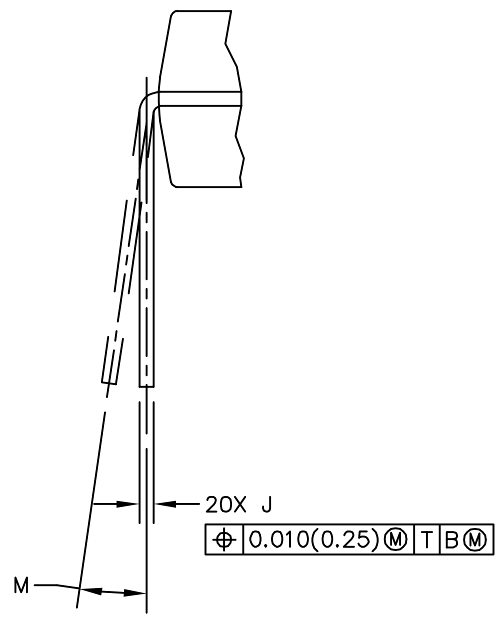
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

△4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

△5. THIS DIMENSION DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSIONS. INTER−LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

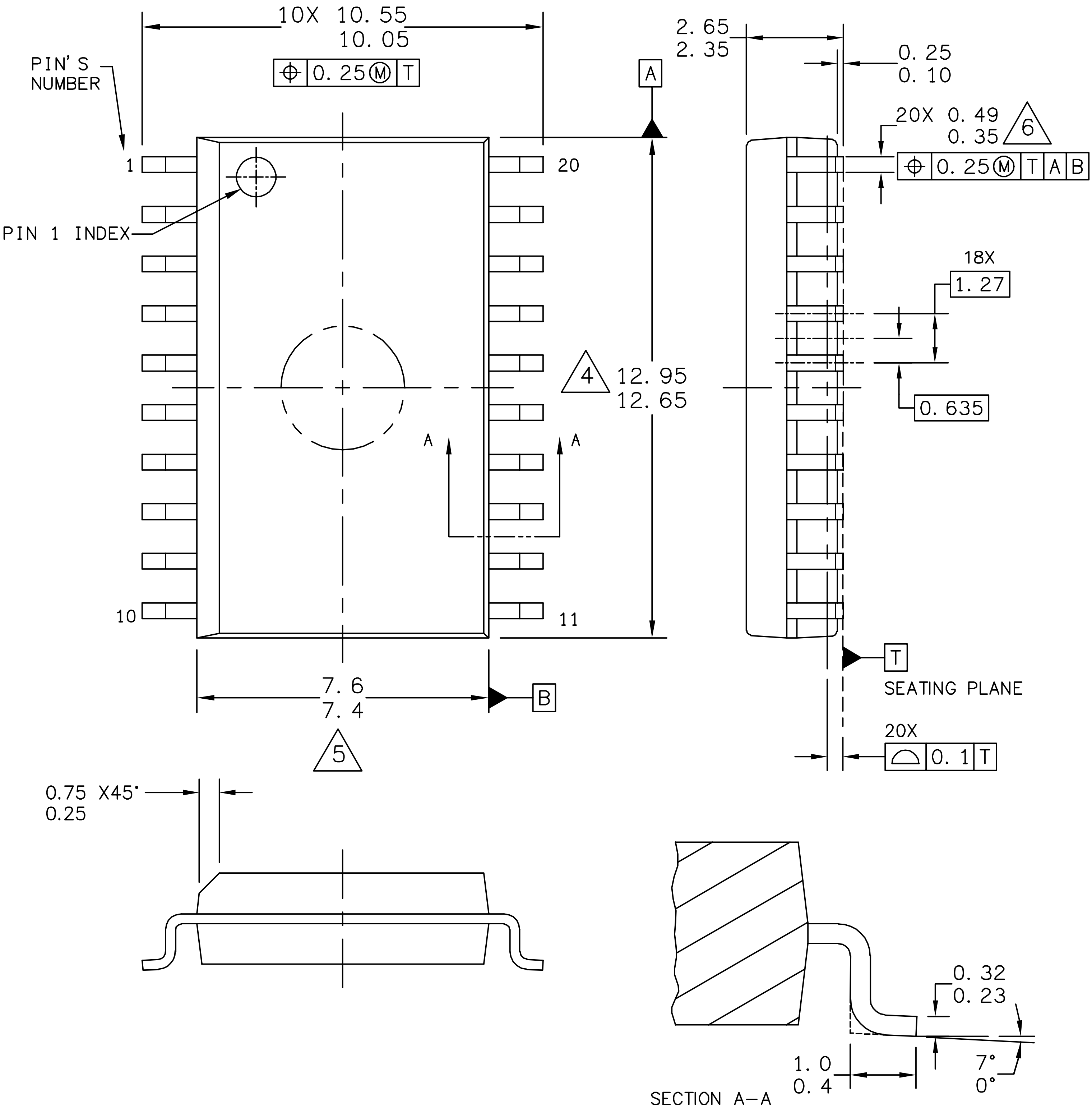
△6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 16LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASB42567B	REV: F
	CASE NUMBER: 751G−04	02 JUN 2005
	STANDARD: JEDEC MS−013AA	



VIEW D

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 20LD .300 PDIP	DOCUMENT NO: 98ASB42899B	REV: B
	CASE NUMBER: 738C-01	24 MAY 2005
	STANDARD: NON-JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: 20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42343B	REV: J
	CASE NUMBER: 751D–07	23 MAR 2005
	STANDARD: JEDEC MS–013AC	

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