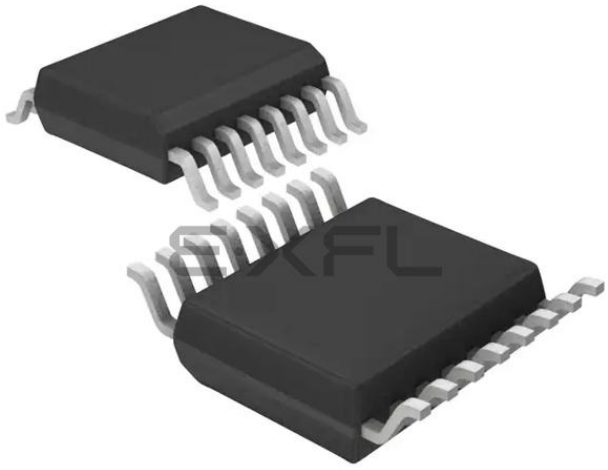


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08ka8ctg

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ pin which is internally clamped to V_{SS} only.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JMAX}	105	°C
Thermal resistance 16-pin PDIP	θ_{JA}	80	°C/W
Thermal resistance 16-pin SOIC	θ_{JA}	112	°C/W

Table 4. Thermal Characteristics (continued)

Rating	Symbol	Value	Unit
Thermal resistance 16-pin TSSOP	θ_{JA}	75	°C/W
Thermal resistance 20-pin PDIP	θ_{JA}	75	°C/W
Thermal resistance 20-pin SOIC	θ_{JA}	96	°C/W

The average chip-junction temperature (TJ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between PD and TJ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (PD)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
Input high voltage (V_{DD} > 2.3V) (all digital inputs)	V_{IH}	0.70 × V_{DD}	—	—	V
Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	0.85 × V_{DD}	—	—	V
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
Input hysteresis (all digital inputs)	V_{hys}[1]	0.06 × V_{DD}	—	—	V
Input leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input only pins	|I_{In}|	—	0.025	1.0	μA
High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	|I_{OZ}|	—	0.025	1.0	μA
Internal pullup resistors[2](all port pins)	R_{PU}	20	45	65	kΩ
Internal pulldown resistors[2](all port pins except PTA5)	R_{PD}	20	45	65	kΩ
PTA5 Internal pulldown resistor	—	45	—	95	kΩ
Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OH}	V_{DD} – 0.8	— — —	— — —	V
Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		V_{DD} – 0.8	— — — —	— — — —	
Maximum total I_{OH} for all port pins	|I_{OHT}|	—	—	40	mA
Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OL}	— — —	— — —	0.8	V
Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		— — — —	— — — —	0.8	
Maximum total I_{OL} for all port pins	I_{OLT}	—	—	40	mA
DC injection current[3, 4, 5, 6] V_{In} < V_{SS}, V_{In} > V_{DD} Single pin limit Total MCU limit, includes sum of all stressed pins		— —	— —	0.2 0.8	mA
Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 This parameter is characterized and not tested on each device.

2 Measurement condition for pull resistors: V_{In} = V_{SS} for pullup and V_{In} = V_{DD} for pulldown.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}$/V_{PP} which is internally clamped to V_{SS} only.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 This parameter is characterized and not tested on each device.

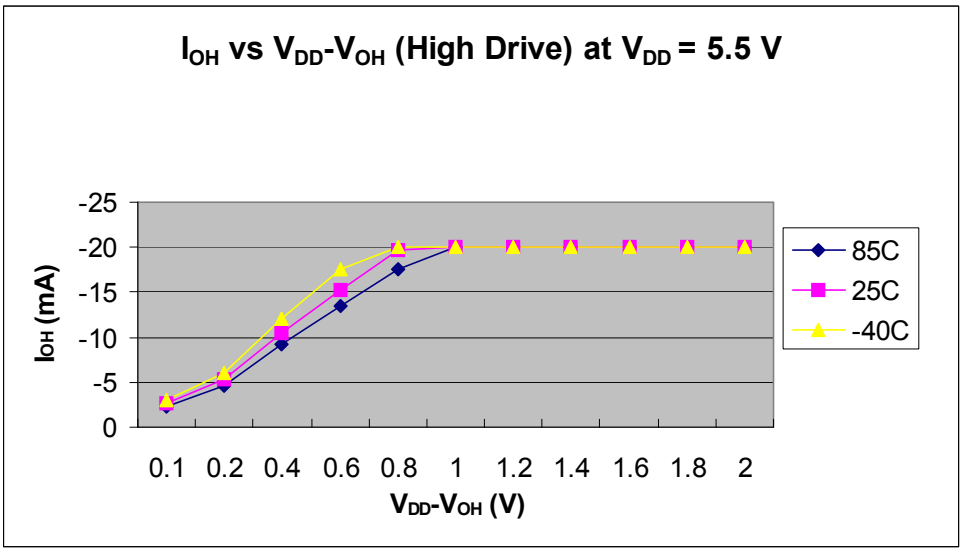


Figure 4. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 5.5 V (High Drive)

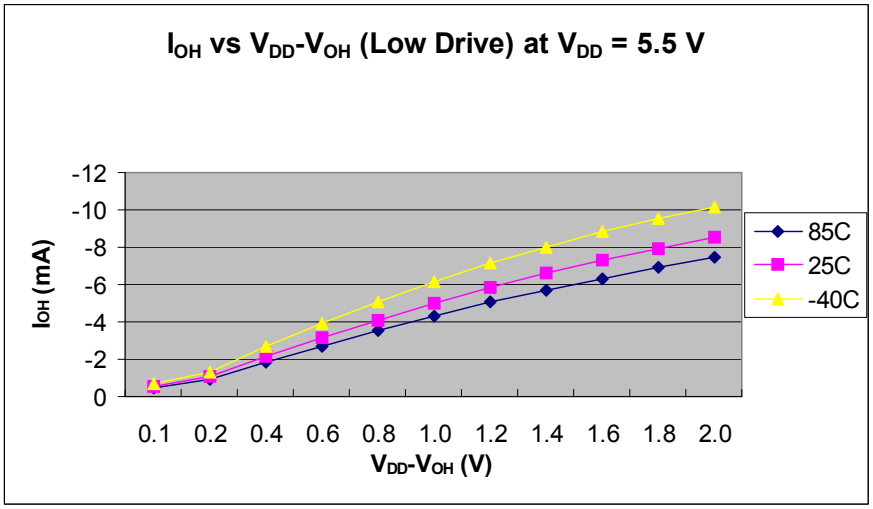


Figure 5. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 5.5 V (Low Drive)

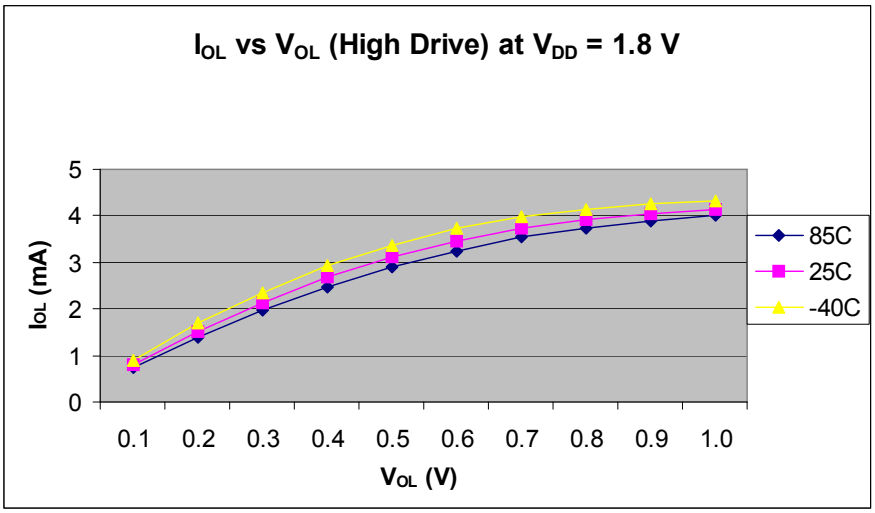


Figure 14. Typical I_{OL} vs. V_{DD}–V_{OL} V_{DD} = 1.8 V (High Drive)

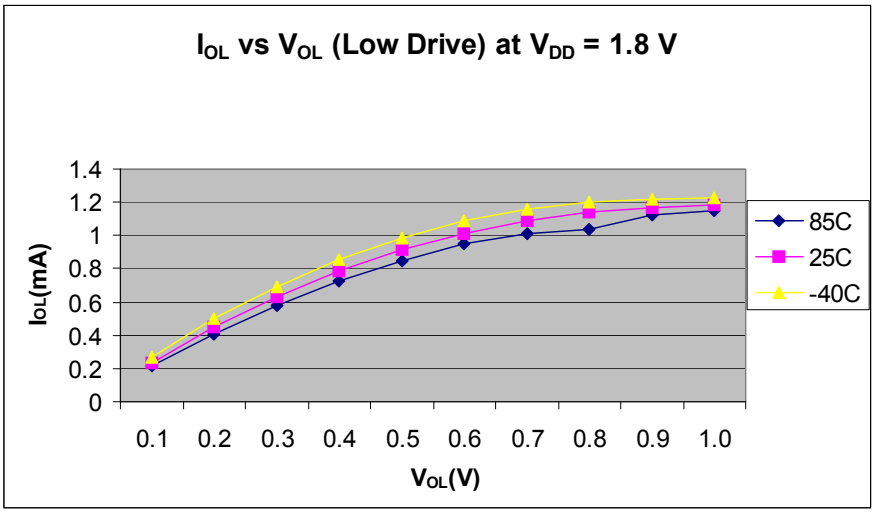


Figure 15. Typical I_{OL} vs. V_{DD}–V_{OL} V_{DD} = 1.8 V (Low Drive)

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
Run supply current[3] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	2.4 mA	5 mA	25 85
		3	2.4 mA	—	25 85
		1.80	1.7 mA	—	25 85

5 Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 1.3 mA at 3 V and 1 mA at 2 V with f_{Bus} = 1 MHz.

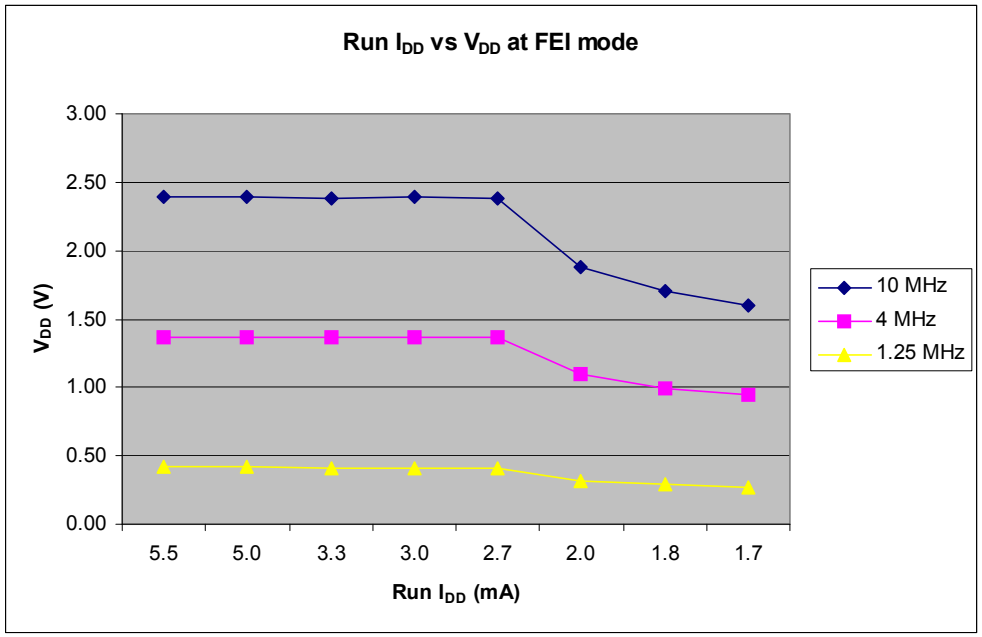


Figure 16. Typical Run I_{DD} vs. V_{DD} for FEI Mode

3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = –40 to 125°C Ambient)

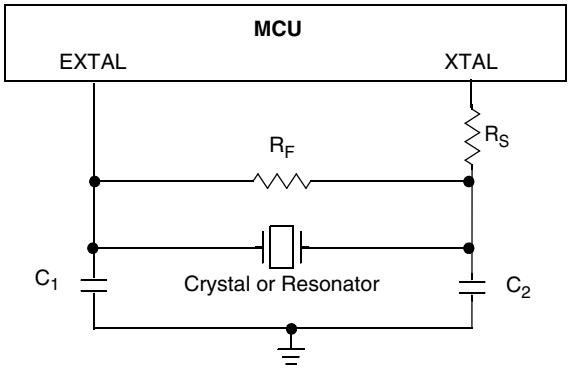
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	D	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	 MΩ
4	D	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	 kΩ
5	C	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 20	 — — — —	 ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] FBELP mode	f_{extal}	0.03125 0	—	5 40	MHz

1 Typical data was characterized at 5.0 V, 25 °C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal.



3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

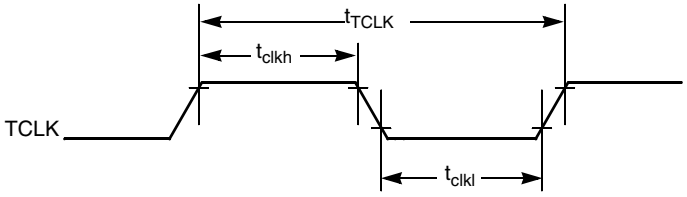


Figure 19. Timer External Clock

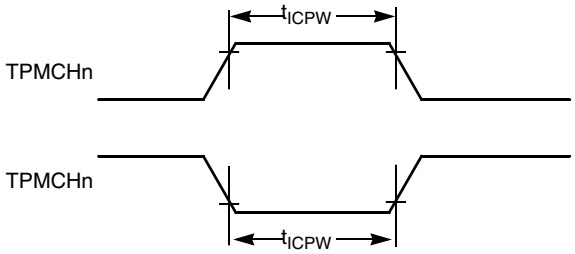


Figure 20. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage[1]	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	P	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	kΩ
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs

Table 12. Analog Comparator Electrical Specifications (continued)

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
9	P	Analog Comparator bandgap reference voltage	V_{BG}	1.1	1.208	1.3	V

1 These data are characterized but not production tested.

3.11 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	31.25	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	39.06	39.0625	kHz
3	C	DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
4	P	DCO output frequency range — trimmed	f_{dco_t}	16	20	20	MHz
5	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	0.2	$\%f_{dco}$
6	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	2	$\%f_{dco}$
7	C	FLL acquisition time[2,3]	$t_{acquire}$	—	—	1	ms
8	C	Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	t_wakeup	—	 100 86	—	µs

1 Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

2 This parameter is characterized and not tested on each device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.12 ADC Characteristics

Table 14. 5 Volt 10-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min.	Typical	Max.	Unit
D	Input voltage	—	V_{ADIN}	V_{SS}	—	V_{DD}	V
C	Accuracy	V_{DD} = 2 V	—	—	8 bit	—	—
C	Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF
C	Input resistance	—	R_{ADIN}	—	3	5	kΩ
C	Analog source resistance external to MCU	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ
		8 bit mode (all valid f_{ADCK})		—	—	10	

Table 15. 10-bit ADC Characteristics (continued)

Characteristic	Conditions	C	Symb	Min	Typical[1]	Max	Unit
Supply current	Stop, reset, module off	T	I_{DDAD}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	T	f_{ADACK}	—	3.3	—	MHz
	Low power (ADLPC = 1)			—	2	—	
Conversion time (including sample time)	Short sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP=1)			—	40	—	
Sample time	Short sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP=1)			—	23.5	—	
Total unadjusted error	10 bit mode	C	E_{TUE}	—	±1	±2.5	LSB[2]
	8 bit mode			—	±0.5	±1.0	
Differential non-linearity	10 bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8 bit mode	T		—	±0.3	±0.5	
	Monotonicity and No-Missing-Codes guaranteed						
Integral non-linearity	10 bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8 bit mode			—	±0.3	±0.5	
Zero-scale error	10 bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8 bit mode	T		—	±0.5	±0.5	
Full-Scale error $V_{ADIN} = V_{DDA}$	10 bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8 bit mode	T		—	±0.5	±0.5	
Quantization error	10 bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8 bit mode			—	—	±0.5	
Input leakage error pad leakage[3] * R_{AS}	10 bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[2]
	8 bit mode			—	±0.1	±1	

1 Typical values assume Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electrical.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 16. Flash Characteristics

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V

Table 16. Flash Characteristics (continued)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Program/Erase voltage	V_{PP}	11.8	12	12.2	V
V_{PP} current Program Mass erase	 I_{VPP_prog} I_{VPP_erase}	 — —	 — —	 200 100	 µA µA
Supply voltage for read operation 0 < f_{Bus} < 10 MHz	V_{Read}	1.8	—	5.5	V
Byte program time	t_{prog}	20	—	40	µs
Mass erase time	t_{me}	500	—	—	ms
Cumulative program HV time[2]	t_{hv}	—	—	8	ms
Total cumulative HV time (total of t_{me} & t_{hv} applied to device)	t_{hv_total}	—	—	2	hours
HVEN to program setup time	t_{pgs}	10	—	—	µs
PGM/MASS to HVEN setup time	t_{nvs}	5	—	—	µs
HVEN hold time for PGM	t_{nvh}	5	—	—	µs
HVEN hold time for MASS	t_{nvh1}	100	—	—	µs
V_{PP} to PGM/MASS setup time	t_{vps}	20	—	—	ns
HVEN to V_{PP} hold time	t_{vph}	20	—	—	ns
V_{PP} rise time[3]	t_{vrs}	200	—	—	ns
Recovery time	t_{rcv}	1	—	—	µs
Program/erase endurance T_L to T_H = –40°C to 85°C	—	1000	—	—	cycles
Data retention	t_{D_ret}	15	—	—	years

1 Typicals are measured at 25 °C.

2 t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

3 Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 22.

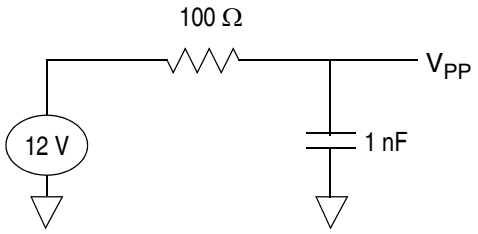


Figure 22. Example V_{PP} Filtering

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.55	0.740	0.770					
B	6.35	6.85	0.250	0.270					
C	3.69	4.44	0.145	0.175					
D	0.39	0.53	0.015	0.021					
F	1.02	1.77	0.040	0.070					
G	2.54 BSC		0.100 BSC						
H	1.27 BSC		0.050 BSC						
J	0.21	0.38	0.008	0.015					
K	2.80	3.30	0.110	0.130					
L	7.50	7.74	0.295	0.305					
M	0°	10°	0°	10°					
S	0.51	1.01	0.020	0.040					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:

16 LD PDIP

DOCUMENT NO: 98ASB42431B | REV: T

CASE NUMBER: 648-08 | 19 MAY 2005

STANDARD: NON-JEDEC

STYLE 1:

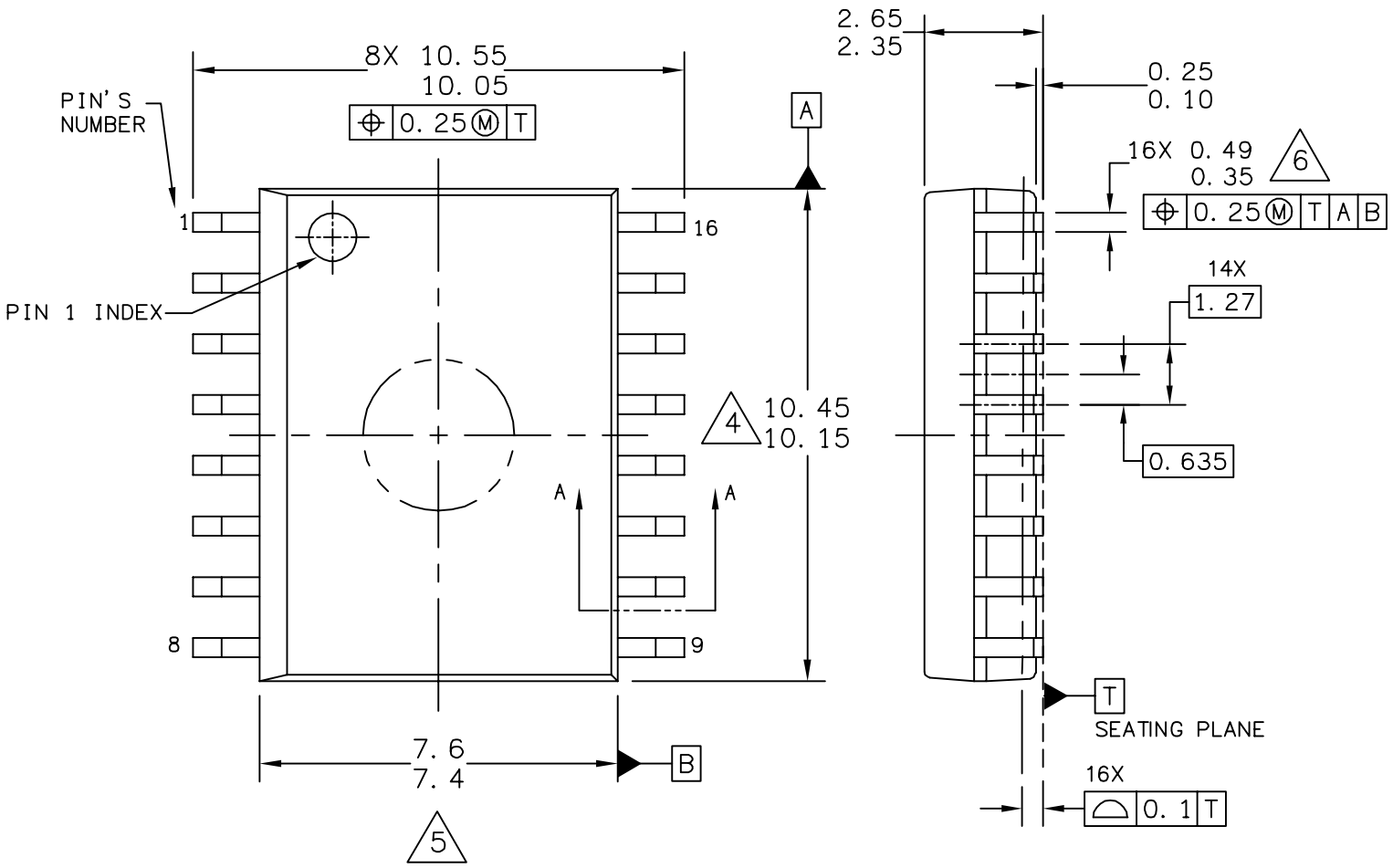
PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

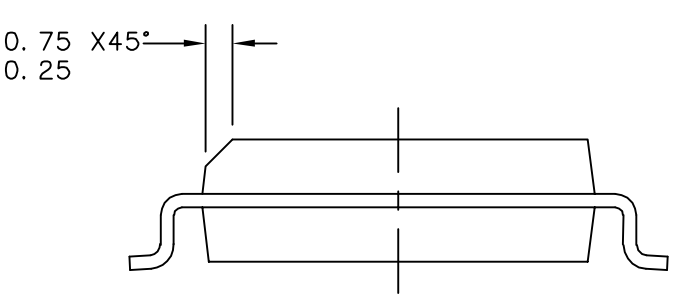
STYLE 2:

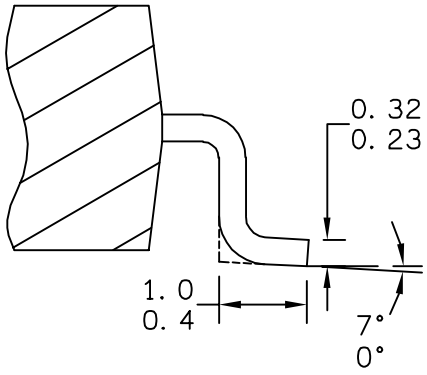
PIN	
1.	COMMON DRAIN
2.	COMMON DRAIN
3.	COMMON DRAIN
4.	COMMON DRAIN
5.	COMMON DRAIN
6.	COMMON DRAIN
7.	COMMON DRAIN
8.	COMMON DRAIN
9.	GATE
10.	SOURCE
11.	GATE
12.	SOURCE
13.	GATE
14.	SOURCE
15.	GATE
16.	SOURCE

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42431B	REV: T
16 LD PDIP	CASE NUMBER: 648-08	19 MAY 2005
	STANDARD: NON-JEDEC	







SECTION A–A

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 16LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42567B	REV: F
	CASE NUMBER: 751G-04	02 JUN 2005
	STANDARD: JEDEC MS-013AA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

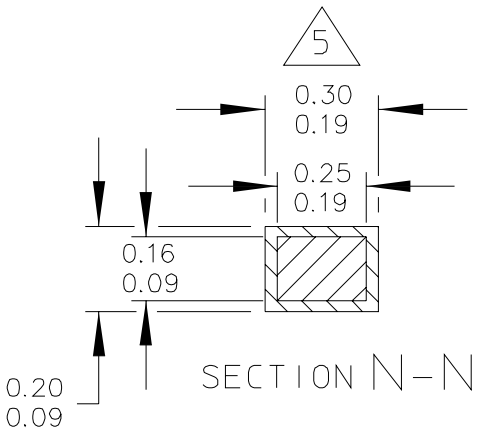
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

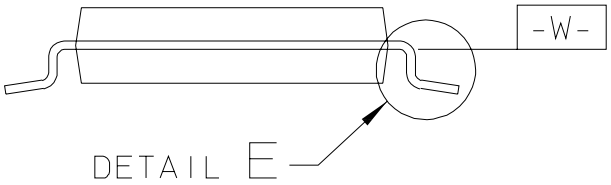
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

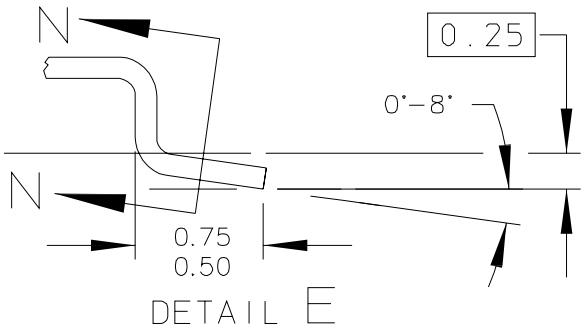
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42567B	REV: F
16LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751G–04	02 JUN 2005
	STANDARD: JEDEC MS–013AA	

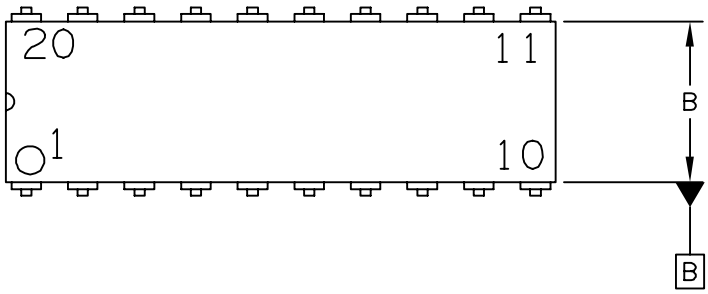


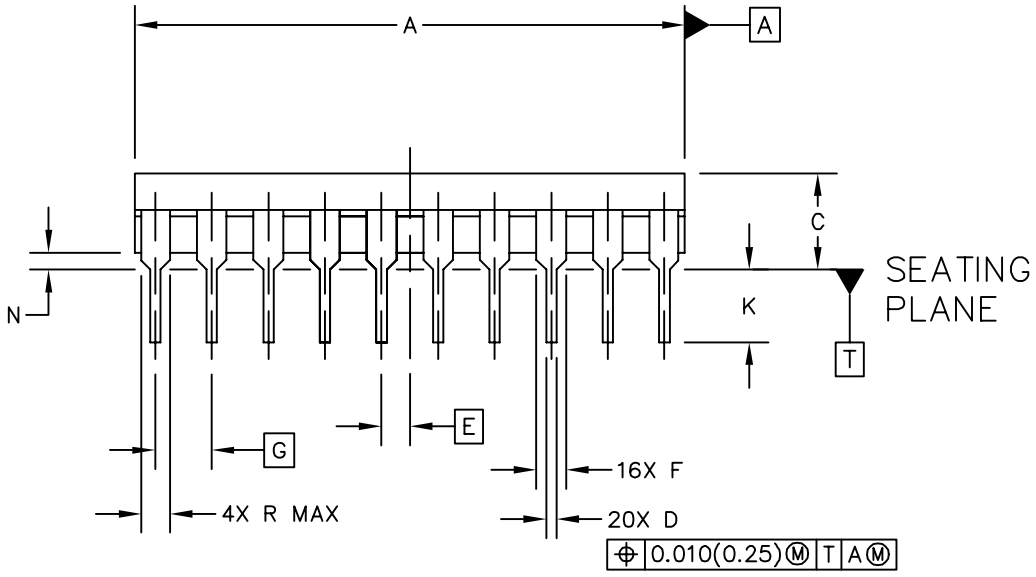


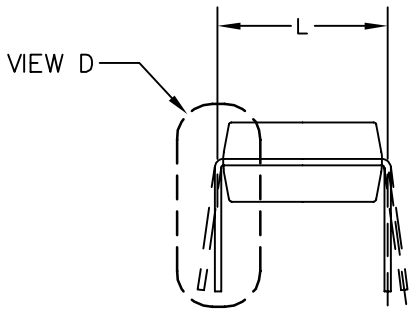


MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	







MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42899B	REV: B
20LD .300 PDIP	CASE NUMBER: 738C-01	24 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS MIN	MAX	DIM	INCHES MIN	MAX	DIM	MILLIMETERS MIN	MAX	DIM	INCHES MIN	MAX
A	24.39	24.99		0.960	0.984						
B	6.96	7.49		0.274	0.295						
C	3.56	5.08		0.140	0.200						
D	0.38	0.56		0.015	0.022						
E	1.27 BSC			0.050 BSC							
F	1.14	1.52		0.045	0.060						
G	2.54 BSC			0.100 BSC							
J	0.20	0.38		0.008	0.015						
K	2.79	3.76		0.110	0.148						
L	7.62 BSC			0.300 BSC							
M	0°	15°		0°	15°						
N	0.50	1.01		0.020	0.040						
R	.....	1.29		.....	0.051						

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

20LD .300 PDIP

DOCUMENT NO: 98ASB42899B

REV: B

CASE NUMBER: 738C-01

24 MAY 2005

STANDARD: NON-JEDEC

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MC9RS08KA8
Rev. 4
6/2009

freescale™
semiconductor