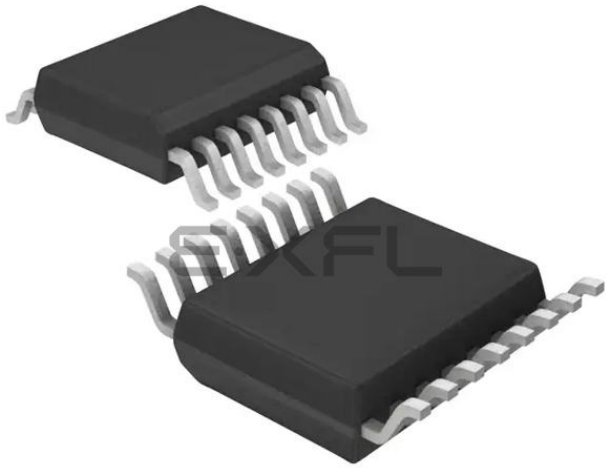

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Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08ka8ctgr

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	1/22/2008	Initial public release
2	10/7/2008	Updated Figure 4 and Figure 10. Updated “How to Reach Us” information. Added 16-pin TSSOP package information.
3	11/4/2008	Updated operating voltage in Table 7.
4	6/11/2009	Added output voltage of high drive at 5 V, I_{load} = 10 mA in the Table 7.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9RS08KA8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

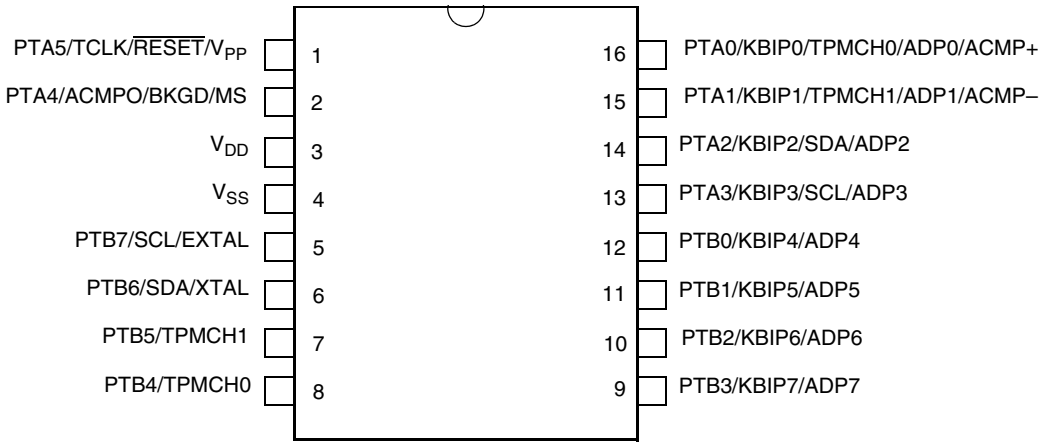


Figure 3. MC9RS08KA8 Series in 16-Pin PDIP/SOIC/TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KA8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C (applies to all pins except pin 9 PTC3/ADP11)	I_{LAT}	±100[2]	—	mA
	Latch-up current at T_A = 85°C (applies to pin 9 PTC3/ADP11)	I_{LAT}	±75[3]	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2 These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ±100mA.

3 This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ±75mA. This pin is only present on 20 pin package types.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage (run, wait and stop modes.) 0 < f_{Bus} <10MHz V_{DD} rising V_{DD} falling	V_{DD}	2.0 1.8	—	5.5	V
Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
Low-voltage Detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.03	V
Power on RESET (POR) voltage	V_{POR}[1]	0.9	—	1.7	V

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Parameter	Symbol	Min	Typical	Max	Unit
Input high voltage (V_{DD} > 2.3V) (all digital inputs)	V_{IH}	0.70 × V_{DD}	—	—	V
Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	0.85 × V_{DD}	—	—	V
Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
Input hysteresis (all digital inputs)	V_{hys}[1]	0.06 × V_{DD}	—	—	V
Input leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input only pins	|I_{In}|	—	0.025	1.0	μA
High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	|I_{OZ}|	—	0.025	1.0	μA
Internal pullup resistors[2](all port pins)	R_{PU}	20	45	65	kΩ
Internal pulldown resistors[2](all port pins except PTA5)	R_{PD}	20	45	65	kΩ
PTA5 Internal pulldown resistor	—	45	—	95	kΩ
Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OH}	V_{DD} – 0.8	— — —	— — —	V
Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		V_{DD} – 0.8	— — — —	— — — —	
Maximum total I_{OH} for all port pins	|I_{OHT}|	—	—	40	mA
Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OL}	— — —	— — —	0.8	V
Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		— — — —	— — — —	0.8	
Maximum total I_{OL} for all port pins	I_{OLT}	—	—	40	mA
DC injection current[3, 4, 5, 6] V_{In} < V_{SS}, V_{In} > V_{DD} Single pin limit Total MCU limit, includes sum of all stressed pins		— —	— —	0.2 0.8	mA
Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 This parameter is characterized and not tested on each device.

2 Measurement condition for pull resistors: V_{In} = V_{SS} for pullup and V_{In} = V_{DD} for pulldown.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}$/V_{PP} which is internally clamped to V_{SS} only.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 This parameter is characterized and not tested on each device.

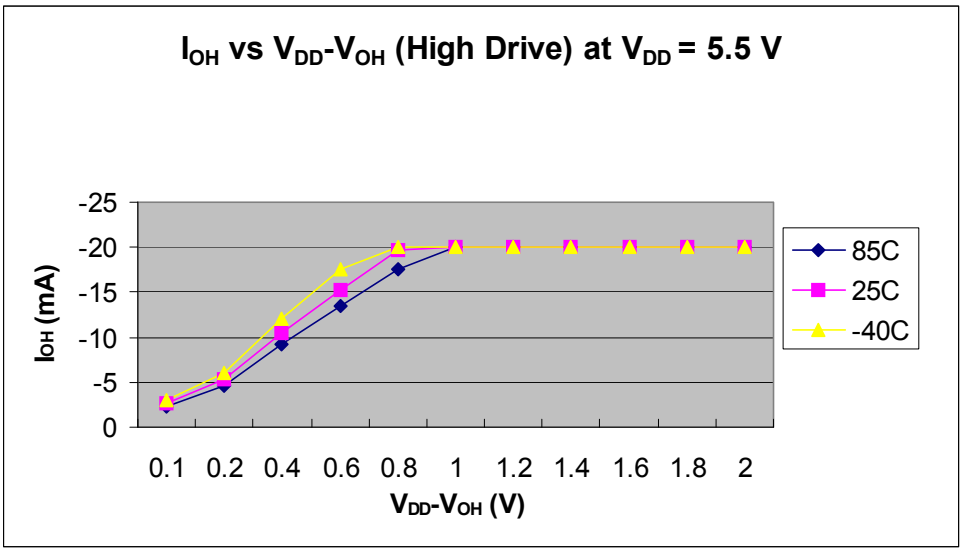


Figure 4. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 5.5 V (High Drive)

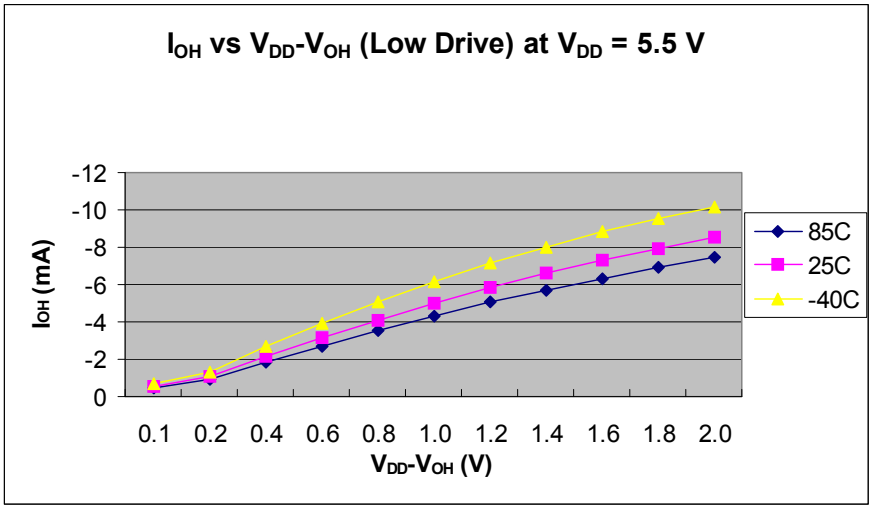


Figure 5. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 5.5 V (Low Drive)

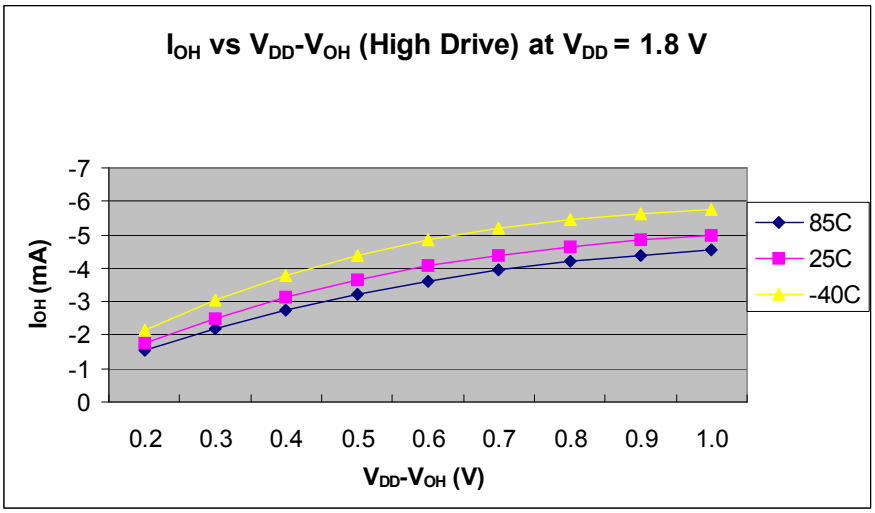


Figure 8. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 1.8 V (High Drive)

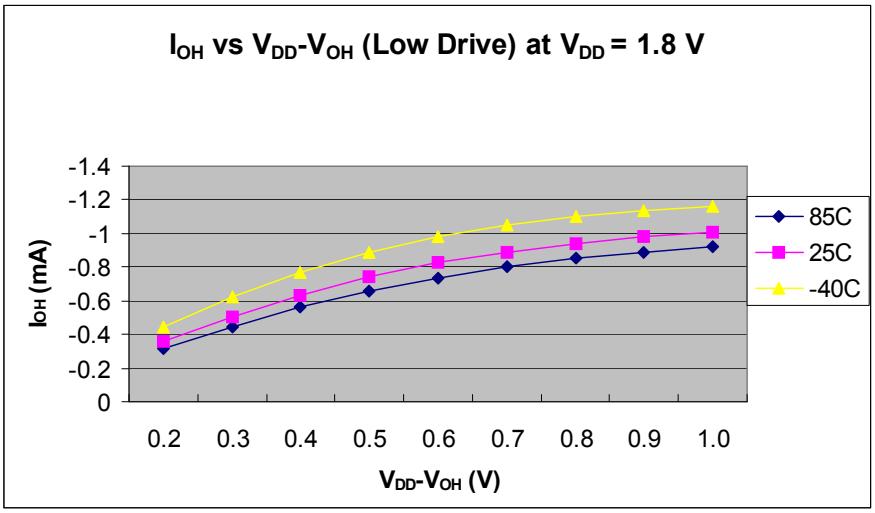


Figure 9. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 1.8 V (Low Drive)

Table 8. Supply Current Characteristics (continued)

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
Run supply current[3] measured at (f_{Bus} = 1.25 MHz)	RI_{DD1}	5	0.42 mA	2 mA	25 85
		3	0.42 mA	—	25 85
		1.80	0.3 mA	—	25 85
Stop mode supply current	SI_{DD}	5	2.4 µA	5 µA 8 µA	25 85
		3	2 µA	—	25 85
		1.80	1.5 µA	—	25 85
ADC adder from stop[4]	—	5	128 µA	150 µA 165 µA	25 85
		3	121 µA	—	25 85
		1.80	79 µA	—	25 85
ACMP adder from stop (ACME = 1)	—	5	21 µA	22 µA	25 85
		3	18.5 µA	—	25 85
		1.80	17.5 µA	—	25 85
RTI adder from stop with 1 kHz clock source enabled[5]	—	5	2.4 µA	2 µA	25 85
		3	1.9 µA	—	25 85
		1.80	1.5 µA	—	25 85
RTI adder from stop with 1 MHz external clock source reference enabled	—	5	2.1 µA	2 µA	25 85
		3	1.6 µA	—	25 85
		1.80	1.2 µA	—	25 85
LVI adder from stop (LVDE=1 and LVDSE=1)	—	5	70 µA	80 µA	25 85
		3	65 µA	—	25 85
		1.80	60 µA	—	25 85

1 Typicals are measured at 25°C.

2 Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

3 Not include any DC loads on port pins.

4 Required asynchronous ADC clock and LVD to be enabled.

3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = –40 to 125°C Ambient)

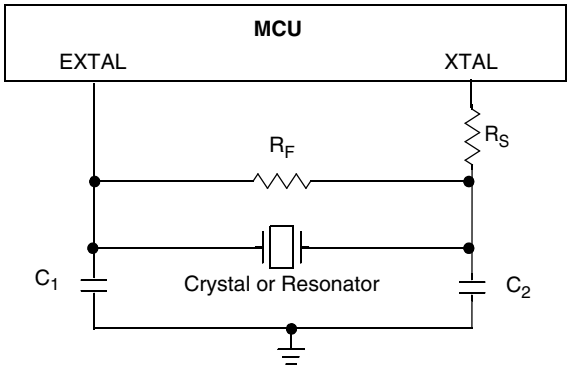
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	D	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	 MΩ
4	D	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	 kΩ
5	C	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 20	 — — — —	 ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] FBELP mode	f_{extal}	0.03125 0	—	5 40	MHz

1 Typical data was characterized at 5.0 V, 25 °C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal.



3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.1 Control Timing

Table 10. Control Timing

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	0	—	10	MHz
2	D	Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	µs
3	D	External $\overline{\text{RESET}}$ pulse width[1]	t_{extrst}	150	—	—	ns
4	D	KBI pulse width[2]	t_{KBIPW}	1.5 t_{cyc}	—	—	ns
5	D	KBI pulse width in stop[1]	t_{KBIPWS}	100	—	—	ns
6	D	Port rise and fall time (load = 50 pF)[3] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	— —	ns

1 This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

2 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

3 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

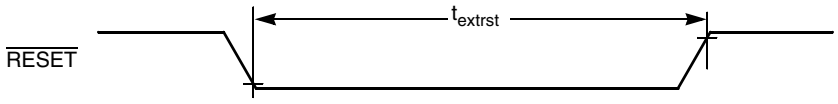


Figure 17. Reset Timing

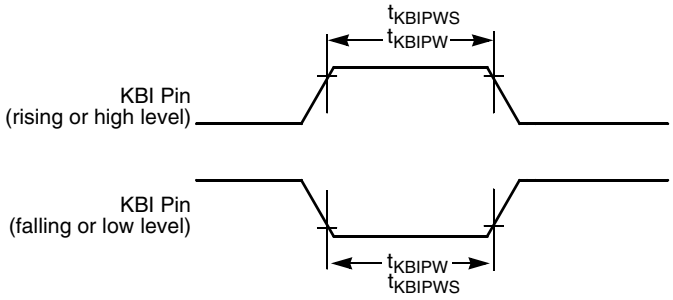


Figure 18. KBI Pulse Width

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

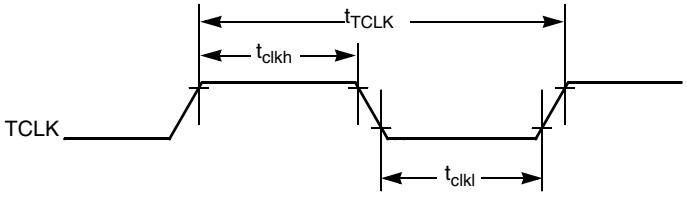


Figure 19. Timer External Clock

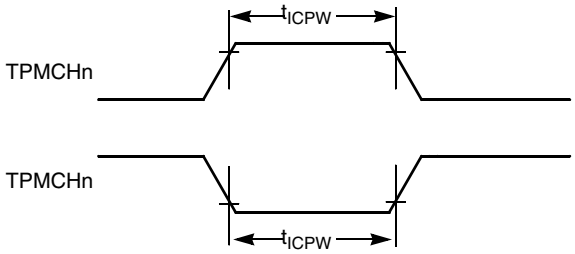


Figure 20. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage[1]	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	P	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	kΩ
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs

Table 12. Analog Comparator Electrical Specifications (continued)

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
9	P	Analog Comparator bandgap reference voltage	V_{BG}	1.1	1.208	1.3	V

1 These data are characterized but not production tested.

3.11 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	31.25	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	39.06	39.0625	kHz
3	C	DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
4	P	DCO output frequency range — trimmed	f_{dco_t}	16	20	20	MHz
5	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	0.2	$\%f_{dco}$
6	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	2	$\%f_{dco}$
7	C	FLL acquisition time[2,3]	$t_{acquire}$	—	—	1	ms
8	C	Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	t_wakeup	—	 100 86	—	µs

1 Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

2 This parameter is characterized and not tested on each device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.12 ADC Characteristics

Table 14. 5 Volt 10-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min.	Typical	Max.	Unit
D	Input voltage	—	V_{ADIN}	V_{SS}	—	V_{DD}	V
C	Accuracy	V_{DD} = 2 V	—	—	8 bit	—	—
C	Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF
C	Input resistance	—	R_{ADIN}	—	3	5	kΩ
C	Analog source resistance external to MCU	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ
		8 bit mode (all valid f_{ADCK})		—	—	10	

Table 15. 10-bit ADC Characteristics (continued)

Characteristic	Conditions	C	Symb	Min	Typical[1]	Max	Unit
Supply current	Stop, reset, module off	T	I_{DDAD}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	T	f_{ADACK}	—	3.3	—	MHz
	Low power (ADLPC = 1)			—	2	—	
Conversion time (including sample time)	Short sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP=1)			—	40	—	
Sample time	Short sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP=1)			—	23.5	—	
Total unadjusted error	10 bit mode	C	E_{TUE}	—	±1	±2.5	LSB[2]
	8 bit mode			—	±0.5	±1.0	
Differential non-linearity	10 bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8 bit mode	T		—	±0.3	±0.5	
	Monotonicity and No-Missing-Codes guaranteed						
Integral non-linearity	10 bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8 bit mode			—	±0.3	±0.5	
Zero-scale error	10 bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8 bit mode	T		—	±0.5	±0.5	
Full-Scale error $V_{ADIN} = V_{DDA}$	10 bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8 bit mode	T		—	±0.5	±0.5	
Quantization error	10 bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8 bit mode			—	—	±0.5	
Input leakage error pad leakage[3] * R_{AS}	10 bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[2]
	8 bit mode			—	±0.1	±1	

1 Typical values assume Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electrical.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 16. Flash Characteristics

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V

Table 16. Flash Characteristics (continued)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Program/Erase voltage	V_{PP}	11.8	12	12.2	V
V_{PP} current Program Mass erase	 I_{VPP_prog} I_{VPP_erase}	 — —	 — —	 200 100	 µA µA
Supply voltage for read operation 0 < f_{Bus} < 10 MHz	V_{Read}	1.8	—	5.5	V
Byte program time	t_{prog}	20	—	40	µs
Mass erase time	t_{me}	500	—	—	ms
Cumulative program HV time[2]	t_{hv}	—	—	8	ms
Total cumulative HV time (total of t_{me} & t_{hv} applied to device)	t_{hv_total}	—	—	2	hours
HVEN to program setup time	t_{pgs}	10	—	—	µs
PGM/MASS to HVEN setup time	t_{nvs}	5	—	—	µs
HVEN hold time for PGM	t_{nvh}	5	—	—	µs
HVEN hold time for MASS	t_{nvh1}	100	—	—	µs
V_{PP} to PGM/MASS setup time	t_{vps}	20	—	—	ns
HVEN to V_{PP} hold time	t_{vph}	20	—	—	ns
V_{PP} rise time[3]	t_{vrs}	200	—	—	ns
Recovery time	t_{rcv}	1	—	—	µs
Program/erase endurance T_L to T_H = –40°C to 85°C	—	1000	—	—	cycles
Data retention	t_{D_ret}	15	—	—	years

1 Typicals are measured at 25 °C.

2 t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

3 Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 22.

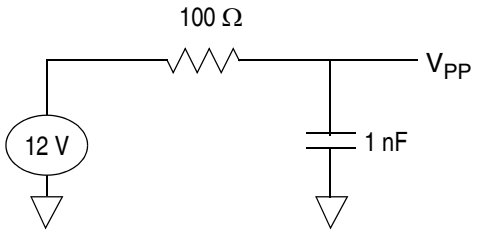
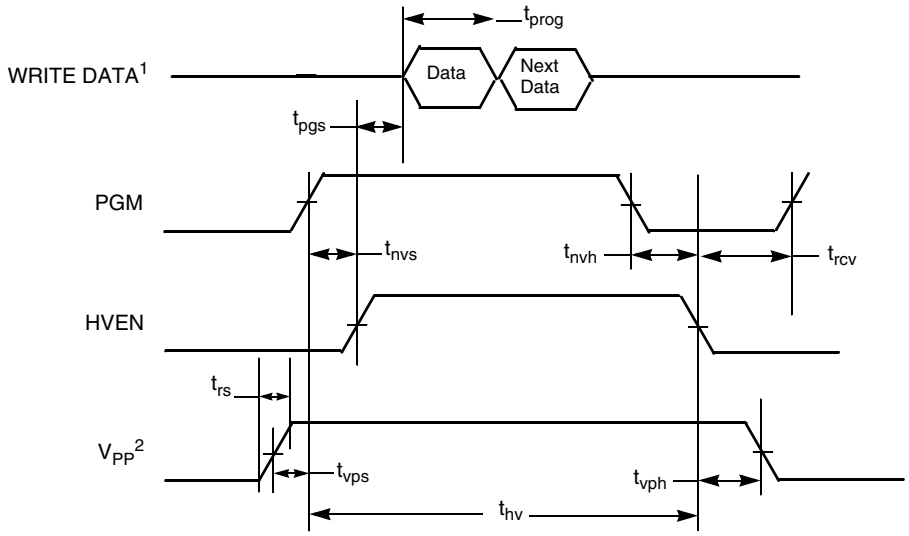
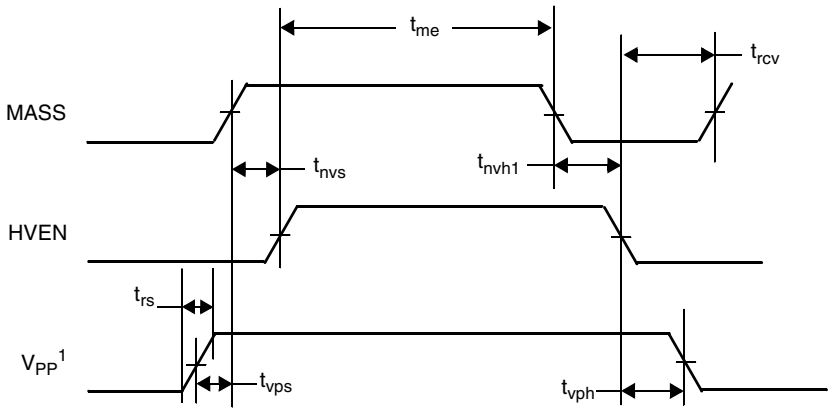


Figure 22. Example V_{PP} Filtering



[1] Next Data applies if programming multiple bytes in a single row, refer to MC9RS08KA8 Series *Reference Manual*.
[2] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 23. Flash Program Timing



[1] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

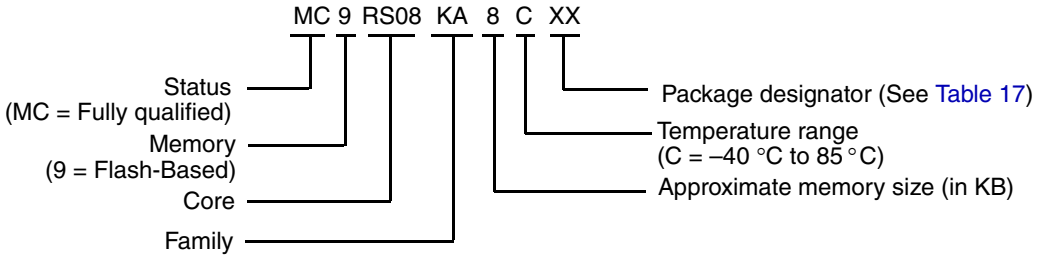
Figure 24. Flash Mass Erase Timing

4 Ordering Information

This section contains ordering numbers for MC9RS08KA8 series devices. See below for an example of the device numbering system.

Table 17. Device Numbering System

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KA8 **MC9RS08KA4**	8K bytes 4K bytes	254 bytes 126 bytes	16 PDIP	PG	98ASB42431B
			16 W-SOIC	WG	98ASB42567B
			16 TSSOP	TG	98ASH70247A
			20 PDIP	PJ	98ASB42899B
			20 W-SOIC	WJ	98ASB42343B



5 Mechanical Drawings

This following pages contain mechanical specifications for MC9RS08KA8 series package options.

- 16-pin PDIP (plastic dual in-line pin)
- 16-pin W-SOIC (wide body small outline integrated circuit)
- 16-pin TSSOP (thin shrink sSmall outline package)
- 20-pin PDIP (plastic dual in-line pin)
- 20-pin W-SOIC (wide body small outline integrated circuit)

STYLE 1:

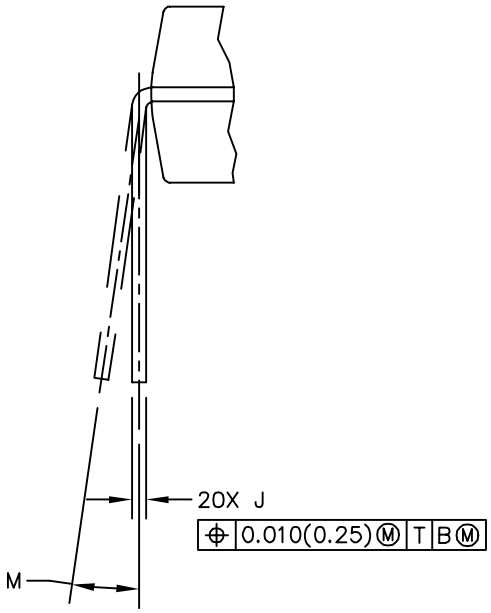
PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 2:

PIN	
1.	COMMON DRAIN
2.	COMMON DRAIN
3.	COMMON DRAIN
4.	COMMON DRAIN
5.	COMMON DRAIN
6.	COMMON DRAIN
7.	COMMON DRAIN
8.	COMMON DRAIN
9.	GATE
10.	SOURCE
11.	GATE
12.	SOURCE
13.	GATE
14.	SOURCE
15.	GATE
16.	SOURCE

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

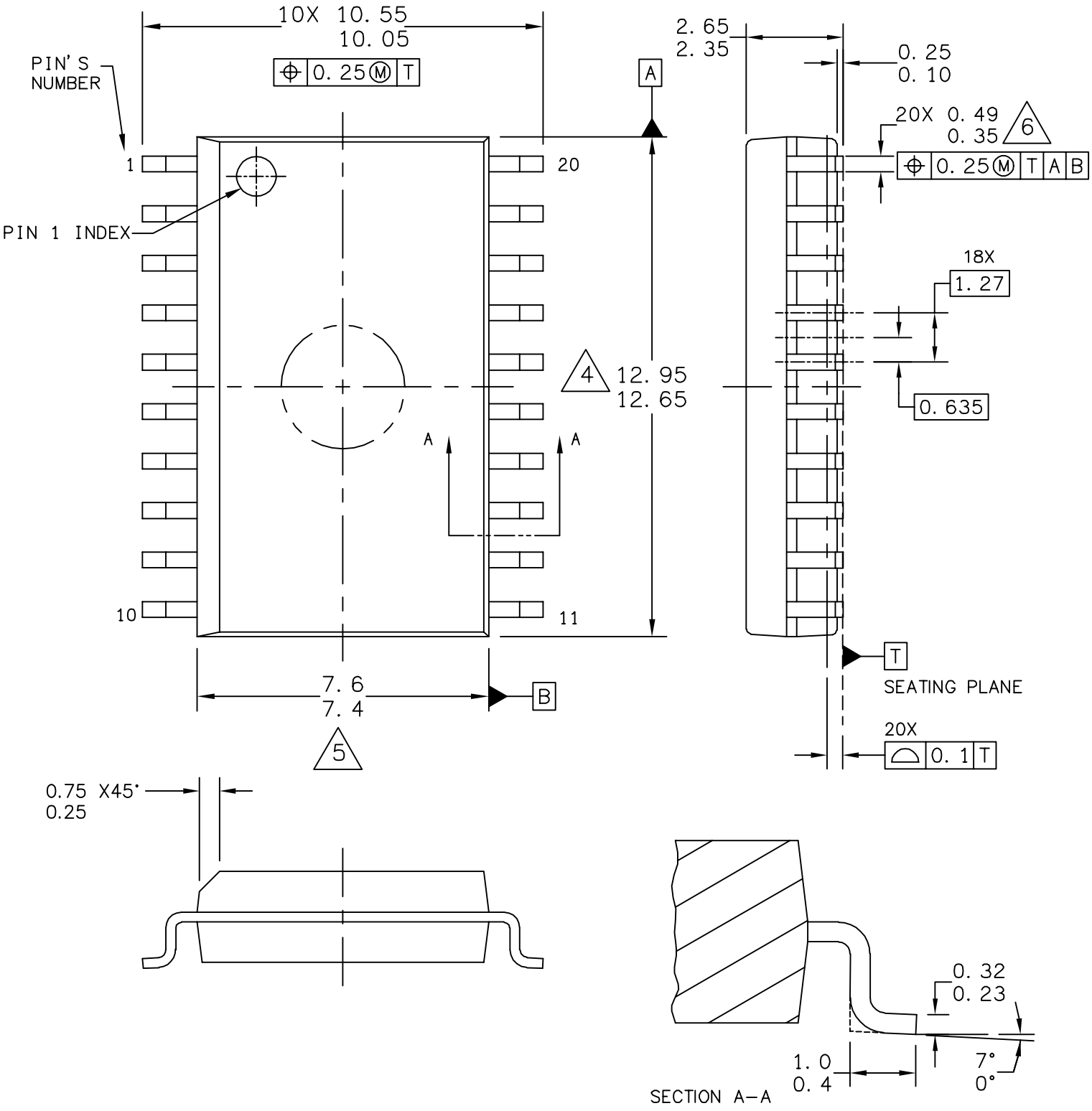
TITLE:	DOCUMENT NO: 98ASB42431B	REV: T
16 LD PDIP	CASE NUMBER: 648-08	19 MAY 2005
	STANDARD: NON-JEDEC	



VIEW D

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42899B	REV: B
20LD .300 PDIP	CASE NUMBER: 738C-01	24 MAY 2005
	STANDARD: NON-JEDEC	



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42343B	REV: J
20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	