Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08ka8cwgr

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	1/22/2008	Initial public release
2	10/7/2008	Updated Figure 4 and Figure 10. Updated “How to Reach Us” information. Added 16-pin TSSOP package information.
3	11/4/2008	Updated operating voltage in Table 7.
4	6/11/2009	Added output voltage of high drive at 5 V, I_{load} = 10 mA in the Table 7.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9RS08KA8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9RS08KA8 MCU.

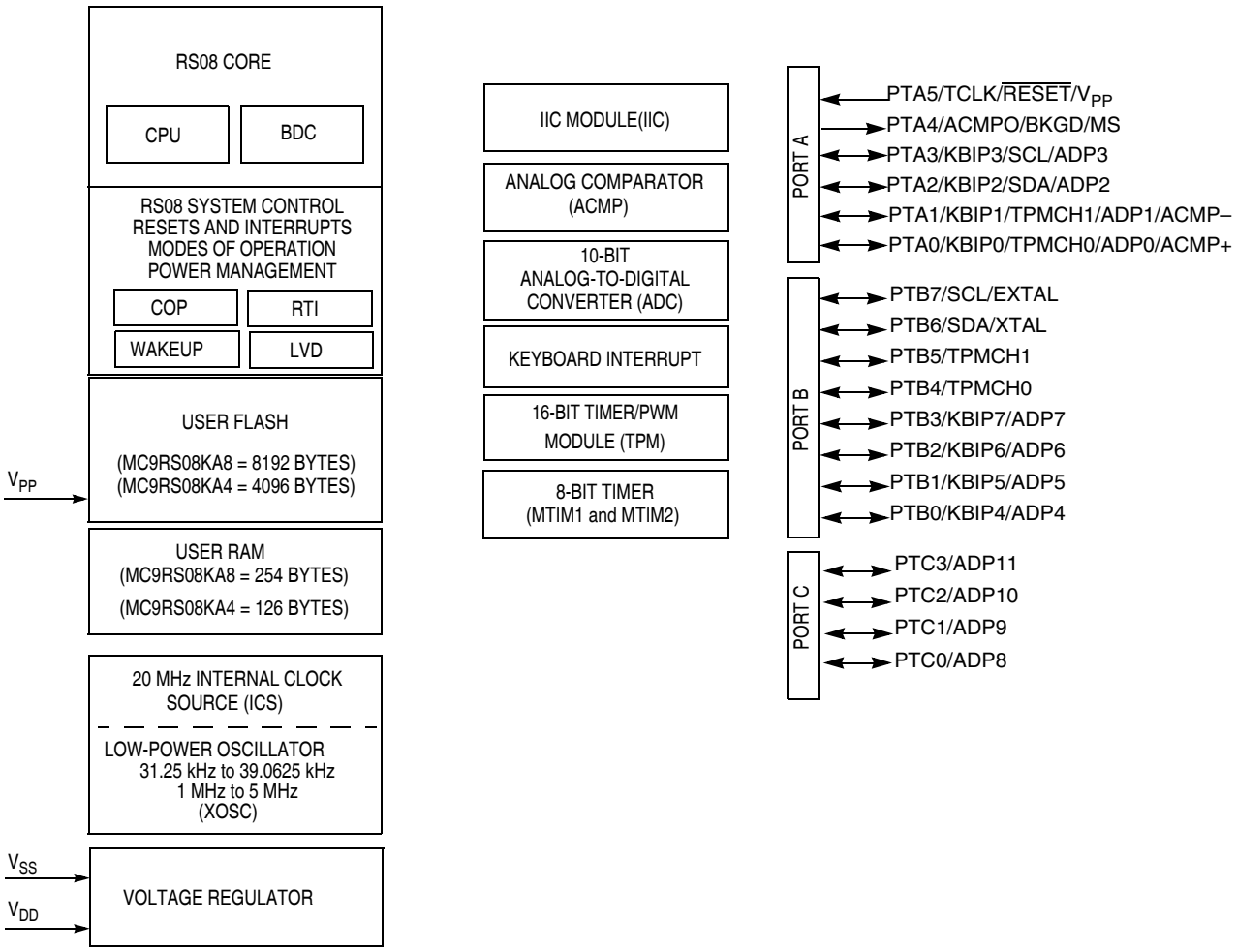


Figure 1. MC9RS08KA8 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KA8 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number		<-- Lowest **Priority** --> Highest				
20	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	PTA5		TCLK	$\overline{\text{RESET}}$	V_{PP}
2	2	PTA4	ACMPO	BKGD	MS	
3	3					V_{DD}
4	4					V_{SS}
5	5	PTB7	SCL[1]			EXTAL
6	6	PTB6	SDA[1]			XTAL
7	7	PTB5	TPMCH1[2]			
8	8	PTB4	TPMCH0[2]			
9	—	PTC3			ADP11	
10	—	PTC2			ADP10	
11	—	PTC1			ADP9	
12	—	PTC0			ADP8	
13	9	PTB3	KBIP7		ADP7	
14	10	PTB2	KBIP6		ADP6	
15	11	PTB1	KBIP5		ADP5	
16	12	PTB0	KBIP4		ADP4	
17	13	PTA3	KBIP3	SCL[1]	ADP3	
18	14	PTA2	KBIP2	SDA[1]	ADP2	
19	15	PTA1	KBIP1	TPMCH1[2]	ADP1	ACMP–
20	16	PTA0	KBIP0	TPMCH0[2]	ADP0	ACMP+

1 IIC pins can be remapped to PTA3 and PTA2

2 TPM pins can be remapped to PTA0 and PTA1

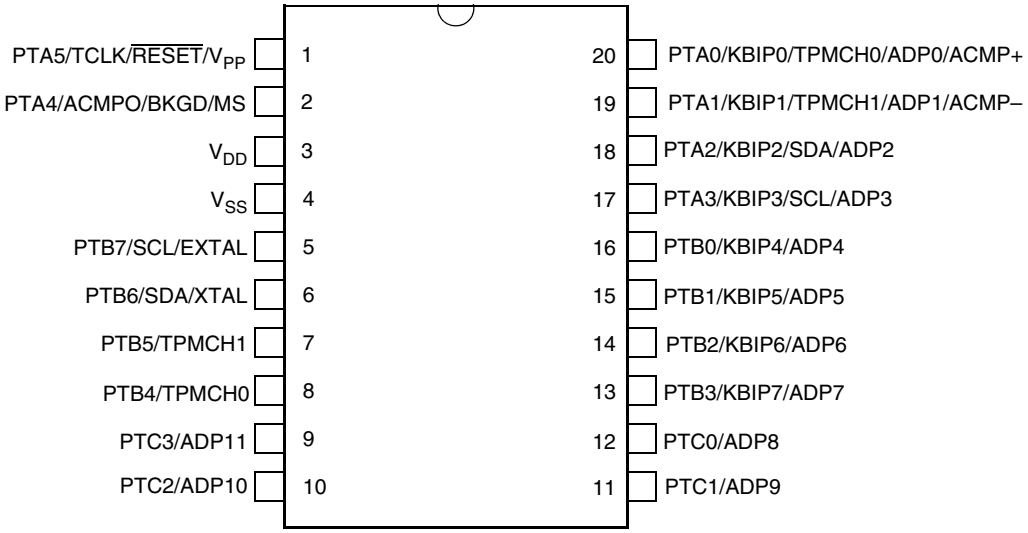


Figure 2. MC9RS08KA8 Series in 20-Pin PDIP/SOIC Package

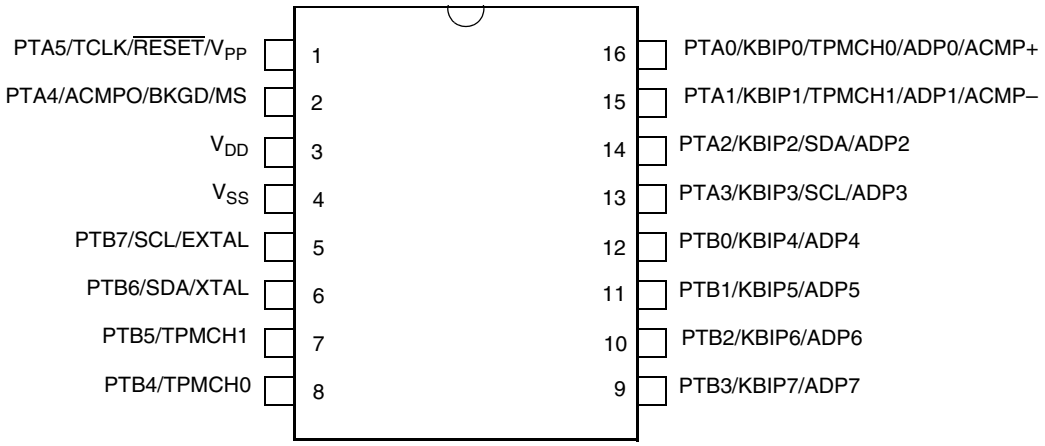


Figure 3. MC9RS08KA8 Series in 16-Pin PDIP/SOIC/TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KA8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ pin which is internally clamped to V_{SS} only.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JMAX}	105	°C
Thermal resistance 16-pin PDIP	θ_{JA}	80	°C/W
Thermal resistance 16-pin SOIC	θ_{JA}	112	°C/W

Table 4. Thermal Characteristics (continued)

Rating	Symbol	Value	Unit
Thermal resistance 16-pin TSSOP	θ_{JA}	75	°C/W
Thermal resistance 20-pin PDIP	θ_{JA}	75	°C/W
Thermal resistance 20-pin SOIC	θ_{JA}	96	°C/W

The average chip-junction temperature (TJ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between PD and TJ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (PD)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C (applies to all pins except pin 9 PTC3/ADP11)	I_{LAT}	±100[2]	—	mA
	Latch-up current at T_A = 85°C (applies to pin 9 PTC3/ADP11)	I_{LAT}	±75[3]	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2 These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of ±100mA.

3 This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to ±75mA. This pin is only present on 20 pin package types.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage (run, wait and stop modes.) 0 < f_{Bus} <10MHz V_{DD} rising V_{DD} falling	V_{DD}	2.0 1.8	—	5.5	V
Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
Low-voltage Detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.03	V
Power on RESET (POR) voltage	V_{POR}[1]	0.9	—	1.7	V

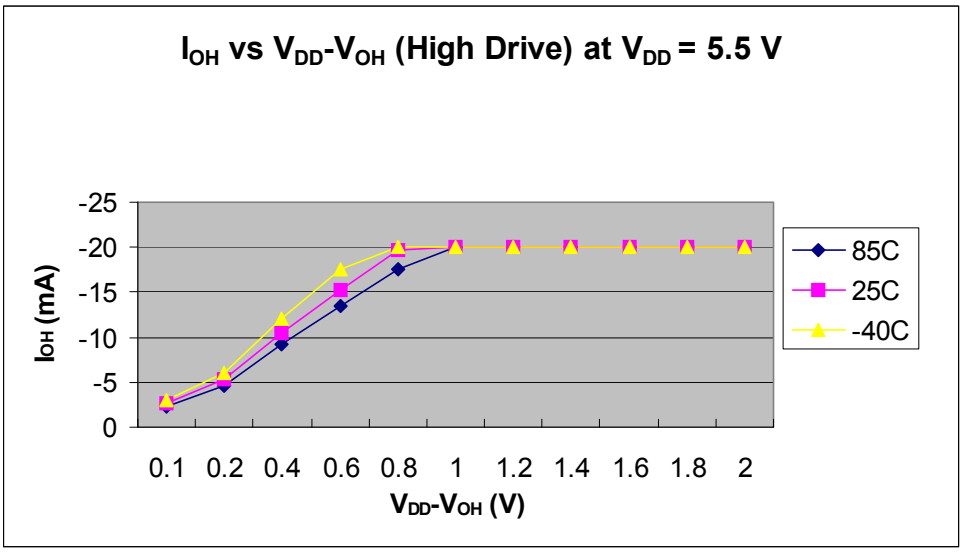


Figure 4. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 5.5 V (High Drive)

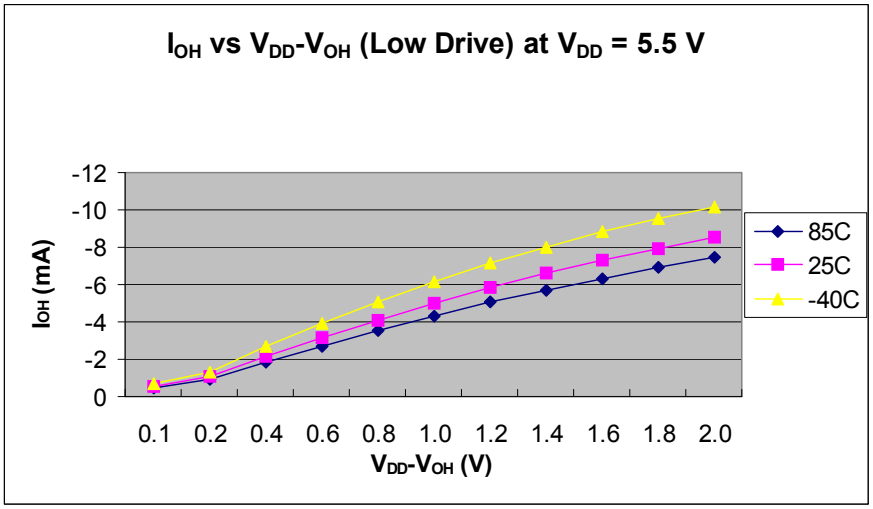


Figure 5. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 5.5 V (Low Drive)

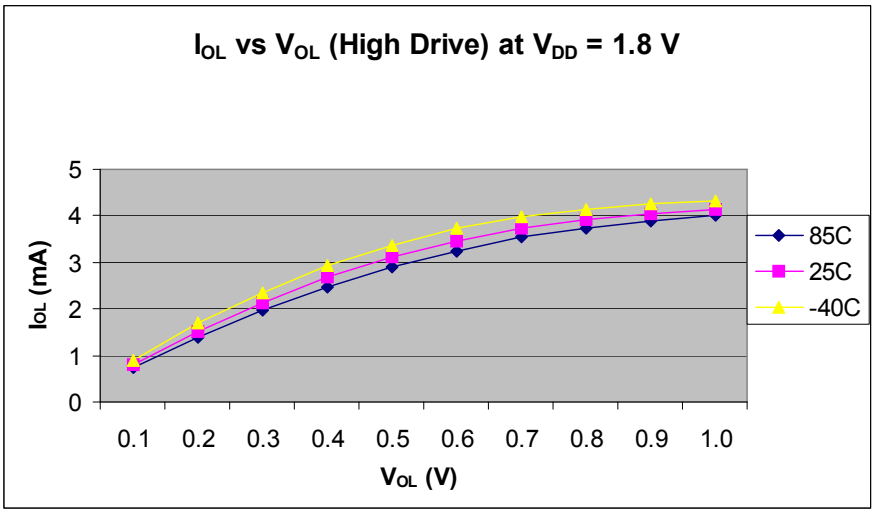


Figure 14. Typical I_{OL} vs. V_{DD}–V_{OL} V_{DD} = 1.8 V (High Drive)

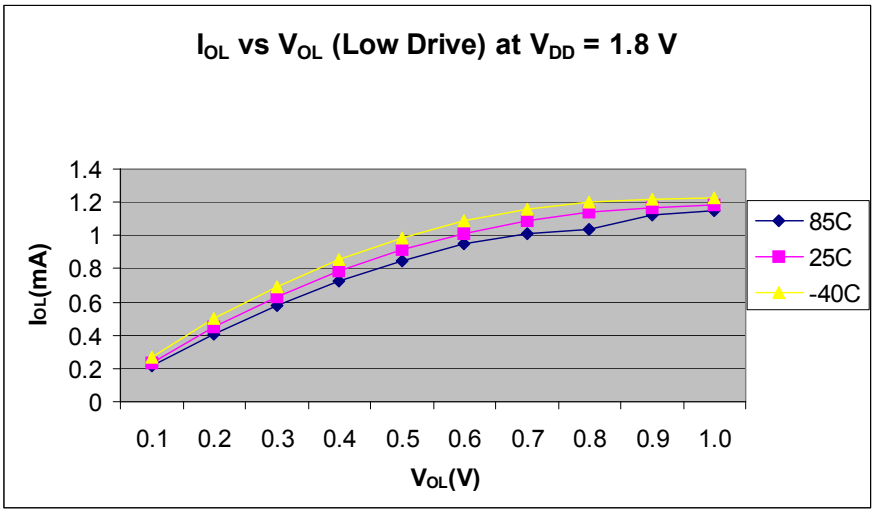


Figure 15. Typical I_{OL} vs. V_{DD}–V_{OL} V_{DD} = 1.8 V (Low Drive)

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
Run supply current[3] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	2.4 mA	5 mA	25 85
		3	2.4 mA	—	25 85
		1.80	1.7 mA	—	25 85

Table 8. Supply Current Characteristics (continued)

Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Temp. (°C)
Run supply current[3] measured at (f_{Bus} = 1.25 MHz)	RI_{DD1}	5	0.42 mA	2 mA	25 85
		3	0.42 mA	—	25 85
		1.80	0.3 mA	—	25 85
Stop mode supply current	SI_{DD}	5	2.4 µA	5 µA 8 µA	25 85
		3	2 µA	—	25 85
		1.80	1.5 µA	—	25 85
ADC adder from stop[4]	—	5	128 µA	150 µA 165 µA	25 85
		3	121 µA	—	25 85
		1.80	79 µA	—	25 85
ACMP adder from stop (ACME = 1)	—	5	21 µA	22 µA	25 85
		3	18.5 µA	—	25 85
		1.80	17.5 µA	—	25 85
RTI adder from stop with 1 kHz clock source enabled[5]	—	5	2.4 µA	2 µA	25 85
		3	1.9 µA	—	25 85
		1.80	1.5 µA	—	25 85
RTI adder from stop with 1 MHz external clock source reference enabled	—	5	2.1 µA	2 µA	25 85
		3	1.6 µA	—	25 85
		1.80	1.2 µA	—	25 85
LVI adder from stop (LVDE=1 and LVDSE=1)	—	5	70 µA	80 µA	25 85
		3	65 µA	—	25 85
		1.80	60 µA	—	25 85

1 Typicals are measured at 25°C.

2 Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

3 Not include any DC loads on port pins.

4 Required asynchronous ADC clock and LVD to be enabled.

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

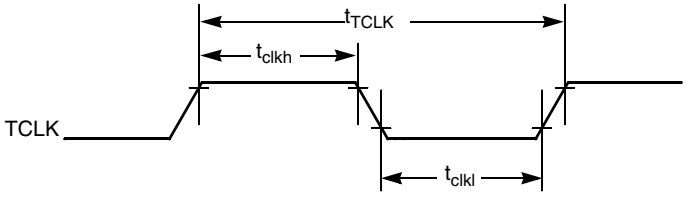


Figure 19. Timer External Clock

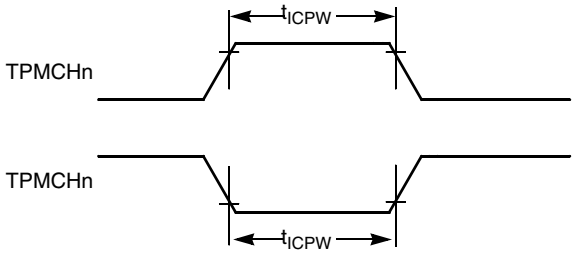


Figure 20. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage[1]	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	P	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	kΩ
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs

Table 15. 10-bit ADC Characteristics (continued)

Characteristic	Conditions	C	Symb	Min	Typical[1]	Max	Unit
Supply current	Stop, reset, module off	T	I_{DDAD}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	T	f_{ADACK}	—	3.3	—	MHz
	Low power (ADLPC = 1)			—	2	—	
Conversion time (including sample time)	Short sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP=1)			—	40	—	
Sample time	Short sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP=1)			—	23.5	—	
Total unadjusted error	10 bit mode	C	E_{TUE}	—	±1	±2.5	LSB[2]
	8 bit mode			—	±0.5	±1.0	
Differential non-linearity	10 bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8 bit mode	T		—	±0.3	±0.5	
	Monotonicity and No-Missing-Codes guaranteed						
Integral non-linearity	10 bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8 bit mode			—	±0.3	±0.5	
Zero-scale error	10 bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8 bit mode	T		—	±0.5	±0.5	
Full-Scale error $V_{ADIN} = V_{DDA}$	10 bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8 bit mode	T		—	±0.5	±0.5	
Quantization error	10 bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8 bit mode			—	—	±0.5	
Input leakage error pad leakage[3] * R_{AS}	10 bit mode	D	E_{IL}	—	±0.2	±2.5	LSB[2]
	8 bit mode			—	±0.1	±1	

1 Typical values assume Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

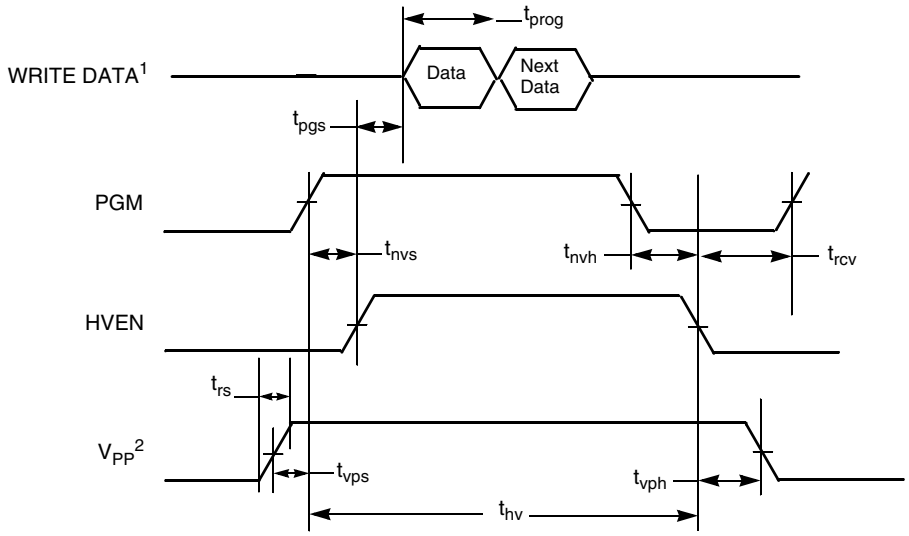
3 Based on input pad leakage current. Refer to pad electrical.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

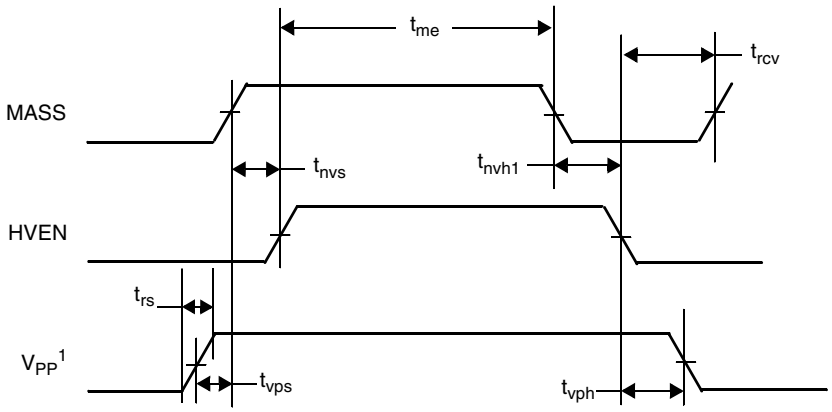
Table 16. Flash Characteristics

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V



[1] Next Data applies if programming multiple bytes in a single row, refer to MC9RS08KA8 Series *Reference Manual*.
[2] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 23. Flash Program Timing



[1] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 24. Flash Mass Erase Timing

STYLE 1:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 2:

PIN	
1.	COMMON DRAIN
2.	COMMON DRAIN
3.	COMMON DRAIN
4.	COMMON DRAIN
5.	COMMON DRAIN
6.	COMMON DRAIN
7.	COMMON DRAIN
8.	COMMON DRAIN
9.	GATE
10.	SOURCE
11.	GATE
12.	SOURCE
13.	GATE
14.	SOURCE
15.	GATE
16.	SOURCE

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42431B	REV: T
16 LD PDIP	CASE NUMBER: 648-08	19 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

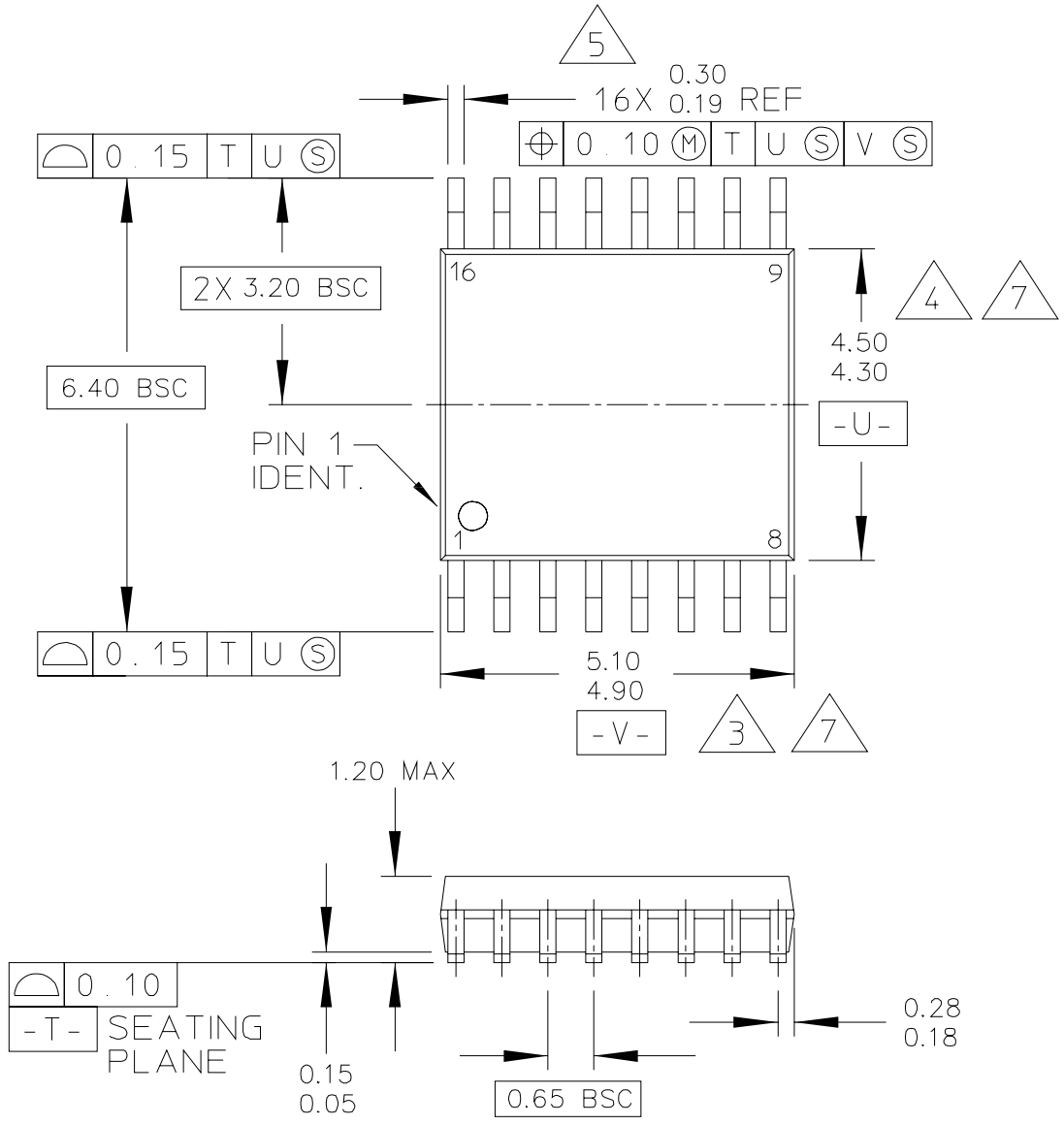
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

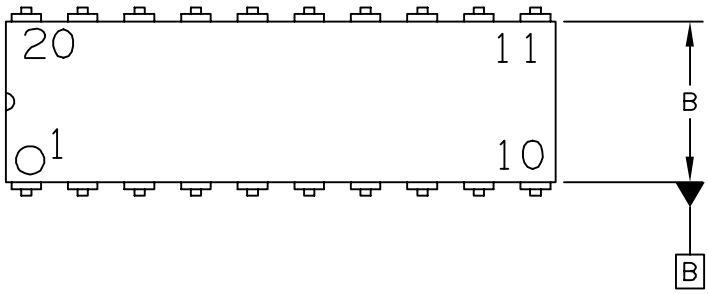
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

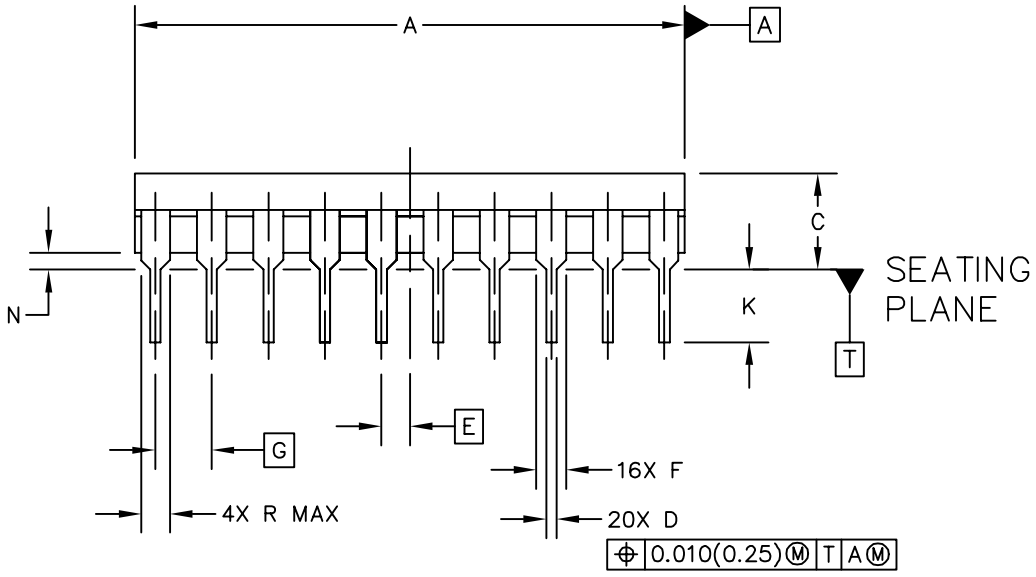
TITLE:	DOCUMENT NO: 98ASB42567B	REV: F
16LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751G–04	02 JUN 2005
	STANDARD: JEDEC MS–013AA	

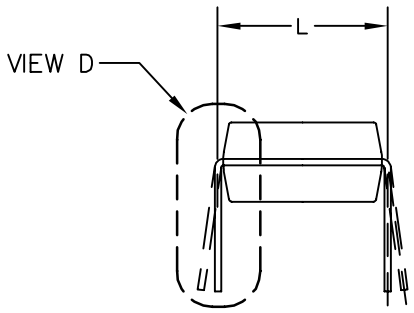


MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	







MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42899B	REV: B
20LD .300 PDIP	CASE NUMBER: 738C-01	24 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS MIN	MAX	DIM	INCHES MIN	MAX	DIM	MILLIMETERS MIN	MAX	DIM	INCHES MIN	MAX
A	24.39	24.99		0.960	0.984						
B	6.96	7.49		0.274	0.295						
C	3.56	5.08		0.140	0.200						
D	0.38	0.56		0.015	0.022						
E	1.27 BSC			0.050 BSC							
F	1.14	1.52		0.045	0.060						
G	2.54 BSC			0.100 BSC							
J	0.20	0.38		0.008	0.015						
K	2.79	3.76		0.110	0.148						
L	7.62 BSC			0.300 BSC							
M	0°	15°		0°	15°						
N	0.50	1.01		0.020	0.040						
R	.....	1.29		.....	0.051						

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

20LD .300 PDIP

DOCUMENT NO: 98ASB42899B

REV: B

CASE NUMBER: 738C-01

24 MAY 2005

STANDARD: NON-JEDEC