Renesas Electronics America Inc - R5F61632N50FPV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f61632n50fpv

			Addressing Mode								
Classification	Instruction	Size	#xx	Rn	@ERn	@(d,ERn)	@(d, RnL.B/ Rn.W/ ERn.L)	@-ERn/ @Ern+/ @Ern-/ @+ERn	@aa:8	@aa:16/ @aa:32	—
Bit manipulation	BFLD	B		D	S				S	S	
	BFST	B		S	D				D	D	
Branch	BRA/BS, BRA/BC*[8]	B			S				S	S	
	BSR/BS, BSR/BC*[8]	B			S				S	S	
System control	LDC (CCR, EXR)	B/W*[9]	S	S	S	S		S*[10]		S	
	LDC (VBR, SBR)	L		S							
	STC (CCR, EXR)	B/W*[9]		D	D	D		D*[11]		D	
	STC (VBR, SBR)	L		D							
	ANDC, ORC, XORC	B	S								
	SLEEP	—									O
	NOP	—									O

[Legend]

d: d:16 or d:32

S: Can be specified as a source operand.

D: Can be specified as a destination operand.

SD: Can be specified as either a source or destination operand or both.

S/D: Can be specified as either a source or destination operand.

S:4: 4-bit immediate data can be specified as a source operand.

Notes:
1. Only @aa:16 is available.
2. @ERn+ as a source operand and @−ERn as a destination operand
3. Specified by ER5 as a source address and ER6 as a destination address for data transfer.
4. Size of data to be added with a displacement
5. Only @ERn− is available
6. When the number of bits to be shifted is 1, 2, 4, 8, or 16
7. When the number of bits to be shifted is specified by 5-bit immediate data or a general register
8. Size of data to specify a branch condition
9. Byte when immediate or register direct, otherwise, word
10. Only @ERn+ is available
11. Only @−ERn is available
12. Not available in this LSI.

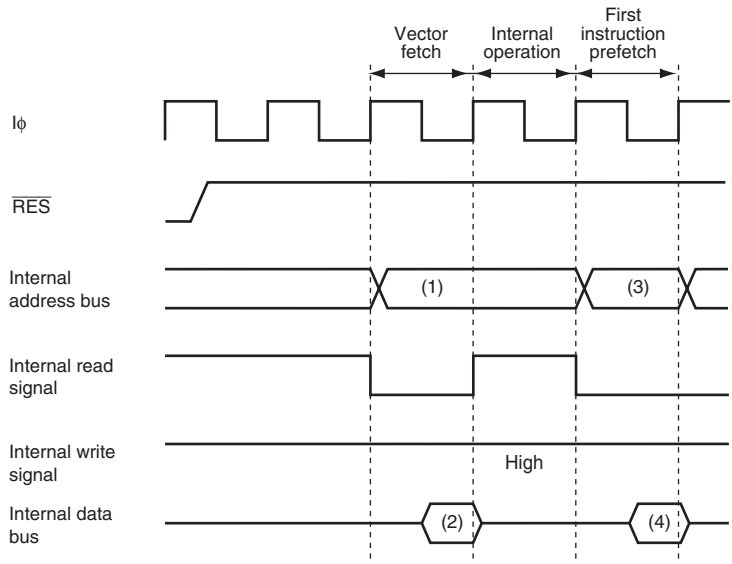
6.3.2 Interrupts after Reset

If an interrupt is accepted after a reset but before the stack pointer (SP) is initialized, the PC and CCR will not be saved correctly, leading to a program crash. To prevent this, all interrupt requests, including NMI, are disabled immediately after a reset. Since the first instruction of a program is always executed immediately after the reset state ends, make sure that this instruction initializes the stack pointer (example: MOV.L #xx: 32, SP).

6.3.3 On-Chip Peripheral Functions after Reset Release

After the reset state is released, MSTPCRA and MSTPCRB are initialized to H'0FFF and H'FFFF, respectively, and all modules except the DTC and DMAC enter the module stop state.

Consequently, on-chip peripheral module registers cannot be read or written to. Register reading and writing is enabled when the module stop state is canceled.



(1): Reset exception handling vector address (when reset, (1) = H'000000)
(2): Start address (contents of reset exception handling vector address)
(3) Start address ((3) = (2))
(4) First instruction in the exception handling routine

Figure 6.1 Reset Sequence (On-chip ROM Enabled Advanced Mode)

8.4 Operation

The UBC does not detect condition matches in standby states (sleep mode, all module clock stop mode, software standby mode, deep software standby mode, and hardware standby mode).

8.4.1 Setting of Break Control Conditions

1. The address condition for the break is set in break address register n (BARn). A mask for the address is set in break address mask register n (BAMRn).
2. The bus and break conditions are set in break control register n (BRCRn). Bus conditions consist of CPU cycle, PC break, and reading. Condition comparison is not performed when the CPU cycle setting is CPn = B'000, the PC break setting is IDn = B'00, or the read setting is RWn = B'00.
3. The condition match CPU flag (CMFCPn) is set in the event of a break condition match on the corresponding channel. These flags are set when the break condition matches but are not cleared when it no longer does. To confirm setting of the same flag again, read the flag once from the break interrupt handling routine, and then write 0 to it (the flag is cleared by writing 0 to it after reading it as 1).

[Legend]

n = Channels A to D

8.4.2 PC Break

1. When specifying a PC break, specify the address as the first address of the required instruction. If the address for a PC break condition is not the first address of an instruction, a break will never be generated.
2. The break occurs after fetching and execution of the target instruction have been confirmed. In cases of contention between a break before instruction execution and a user maskable interrupt, priority is given to the break before instruction execution.
3. A break will not be generated even if a break before instruction execution is set in a delay slot.
4. The PC break condition is generated by specifying CPU cycles as the bus condition in break control register n (BRCRn.CPn0 = 1), PC break as the break condition (IDn0 = 1), and read cycles as the bus-cycle condition (RWn0 = 1).

[Legend]

n = Channels A to D

9.2.4 Read Strobe Timing Control Register (RDNCR)

RDNCR selects the negation timing of the read strobe signal ($\overline{RD}$) when reading the external address spaces specified as a basic bus interface or the address/data multiplexed I/O interface.

Bit	15	14	13	12	11	10	9	8
Bit Name	RDN7	RDN6	RDN5	RDN4	RDN3	RDN2	RDN1	RDN0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	RDN7	0	R/W	Read Strobe Timing Control
14	RDN6	0	R/W	RDN7 to RDN0 set the negation timing of the read strobe in a corresponding area read access.
13	RDN5	0	R/W	
12	RDN4	0	R/W	As shown in figure 9.2, the read strobe for an area for which the RDNn bit is set to 1 is negated one half-cycle earlier than that for an area for which the RDNn bit is cleared to 0. The read data setup and hold time are also given one half-cycle earlier.
11	RDN3	0	R/W	
10	RDN2	0	R/W	
9	RDN1	0	R/W	
8	RDN0	0	R/W	0: In an area n read access, the $\overline{RD}$ signal is negated at the end of the read cycle 1: In an area n read access, the $\overline{RD}$ signal is negated one half-cycle before the end of the read cycle (n = 7 to 0)
7 to 0	—	All 0	R	Reserved These are read-only bits and cannot be modified.

Notes: 1. In an external address space which is specified as byte control SRAM interface, the RDNCR setting is ignored and the same operation when RDNn = 1 is performed.
2. In an external address space which is specified as burst ROM interface, the RDNCR setting is ignored during CPU read accesses and the same operation when RDNn = 0 is performed.

9.10 Idle Cycle

In this LSI, idle cycles can be inserted between the consecutive external accesses. By inserting the idle cycle, data conflicts between ROM read cycle whose output floating time is long and an access cycle from/to high-speed memory or I/O interface can be prevented.

9.10.1 Operation

When this LSI consecutively accesses external address space, it can insert an idle cycle between bus cycles in the following four cases. These conditions are determined by the sequence of read and write and previously accessed area.

1. When read cycles of different areas in the external address space occur consecutively
2. When an external write cycle occurs immediately after an external read cycle
3. When an external read cycle occurs immediately after an external write cycle
4. When an external access occurs immediately after a DMAC single address transfer (write cycle)

Up to four idle cycles can be inserted under the conditions shown above. The number of idle cycles to be inserted should be specified to prevent data conflicts between the output data from a previously accessed device and data from a subsequently accessed device.

Under conditions 1 and 2, which are the conditions to insert idle cycles after read, the number of idle cycles can be selected from setting A specified by bits IDLCA1 and IDLCA0 in IDLCR or setting B specified by bits IDLCB1 and IDLCB0 in IDLCR: Setting A can be selected from one to four cycles, and setting B can be selected from one or two to four cycles. Setting A or B can be specified for each area by setting bits IDLSEL7 to IDLSEL0 in IDLCR. Note that bits IDLSEL7 to IDLSEL0 correspond to the previously accessed area of the consecutive accesses.

The number of idle cycles to be inserted under conditions 3 and 4, which are conditions to insert idle cycles after write, can be determined by setting A as described above.

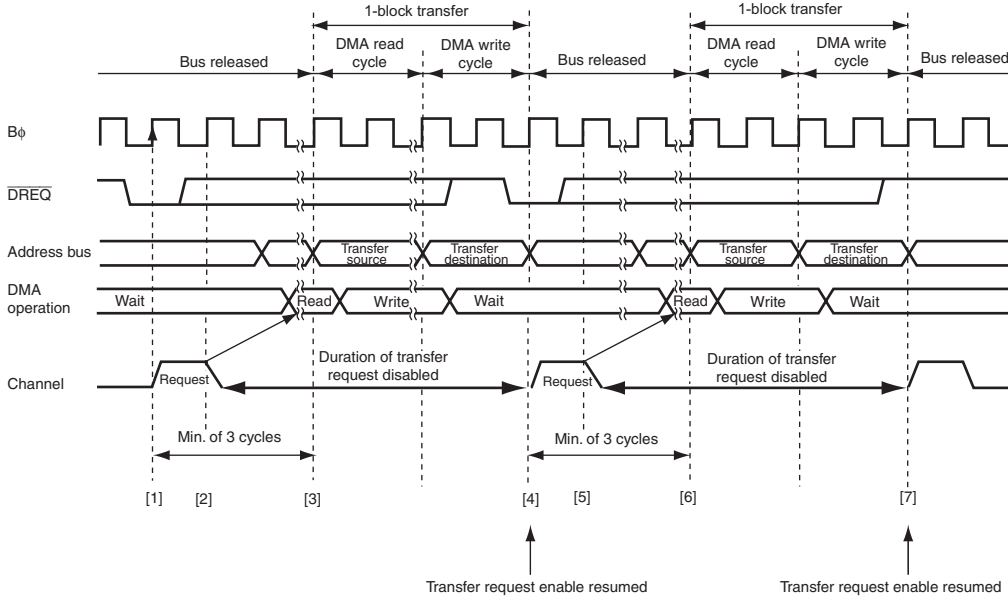
After the reset release, IDLCR is initialized to four idle cycle insertion under all conditions 1 to 4 shown above.

Table 9.20 shows the correspondence between conditions 1 to 4 and number of idle cycles to be inserted for each area. Table 9.21 shows the correspondence between the number of idle cycles to be inserted specified by settings A and B, and number of cycles to be inserted.

Figure 10.32 shows an example of block transfer mode activated by the $\overline{\text{DREQ}}$ signal low level.

The $\overline{\text{DREQ}}$ signal is sampled every cycle from the next rising edge of the Bϕ signal immediately after the DTE bit write cycle.

When a low level of the $\overline{\text{DREQ}}$ signal is detected while a transfer request by the $\overline{\text{DREQ}}$ signal is enabled, a transfer request is held in the DMAC. When the DMAC is activated, the transfer request is cleared. Receiving the next transfer request resumes after completion of the write cycle and then a low level of the $\overline{\text{DREQ}}$ signal is detected. This operation is repeated until the transfer is completed.



[1] After DMA transfer request is enabled, a low level of the $\overline{\text{DREQ}}$ signal is detected at the rising edge of the Bϕ signal and a transfer request is held.
[2][5] The DMAC is activated and the transfer request is cleared.
[3][6] A DMA cycle is started.
[4][7] Transfer request enable is resumed after completion of the write cycle.
(A low level of the $\overline{\text{DREQ}}$ signal is detected at the rising edge of the Bϕ signal and a transfer request is held. This is the same as [1].)

Figure 10.32 Example of Transfer in Block Transfer Mode Activated by $\overline{\text{DREQ}}$ Low Level

Bit	Bit Name	Initial Value	R/W	Description
15	DTCE15	0	R/W	DTC Activation Enable 15 to 0
14	DTCE14	0	R/W	Setting this bit to 1 specifies a relevant interrupt source to a DTC activation source.
13	DTCE13	0	R/W	[Clearing conditions]
12	DTCE12	0	R/W	• When writing 0 to the bit to be cleared after reading 1
11	DTCE11	0	R/W	• When the DISEL bit is 1 and the data transfer has ended
10	DTCE10	0	R/W	• When the specified number of transfers have ended
9	DTCE9	0	R/W	These bits are not cleared when the DISEL bit is 0 and the specified number of transfers have not ended
8	DTCE8	0	R/W	
7	DTCE7	0	R/W	
6	DTCE6	0	R/W	
5	DTCE5	0	R/W	
4	DTCE4	0	R/W	
3	DTCE3	0	R/W	
2	DTCE2	0	R/W	
1	DTCE1	0	R/W	
0	DTCE0	0	R/W	

11.2.8 DTC Control Register (DTCCR)

DTCCR specifies transfer information read skip.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	RRS	RCHNE	—	—	ERR
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/(W)*

Note: * Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

(3) P35/PO13/TIOCA1/TIOCB1/TCLKC-A/$\overline{\text{DACK1}}$-B

The pin function is switched as shown below according to the combination of the DMAC, TPU, and PPG register settings and P35DDR bit setting.

		Setting			
		DMAC	TPU	PPG	I/O Port
Module Name	Pin Function	$\overline{\text{DACK1B}}$_OE	TIOCB1_OE	PO13_OE	P35DDR
DMAC	$\overline{\text{DACK1}}$-B output	1	—	—	—
TPU	TIOCB1 output	0	1	—	—
PPG	PO13 output	0	0	1	—
I/O port	P35 output	0	0	0	1
	P35 input (initial setting)	0	0	0	0

(4) P34/PO12/TIOCA1/$\overline{\text{TEND1}}$-B

The pin function is switched as shown below according to the combination of the DMAC, TPU, and PPG register settings and P34DDR bit setting.

		Setting			
		DMAC	TPU	PPG	I/O Port
Module Name	Pin Function	$\overline{\text{TEND1B}}$_OE	TIOCA1_OE	PO12_OE	P34DDR
DMAC	$\overline{\text{TEND1}}$-B output	1	—	—	—
TPU	TIOCA1 output	0	1	—	—
PPG	PO12 output	0	0	1	—
I/O port	P34 output	0	0	0	1
	P34 input (initial setting)	0	0	0	0

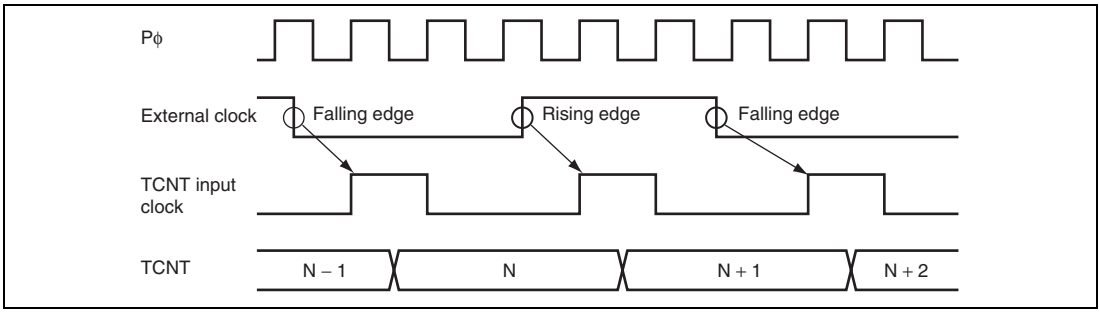


Figure 13.32 Count Timing in External Clock Operation

(2) Output Compare Output Timing

A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the output value set in TIOR is output at the output compare output pin (TIOC pin). After a match between TCNT and TGR, the compare match signal is not generated until the TCNT input clock is generated.

Figure 13.33 shows output compare output timing.

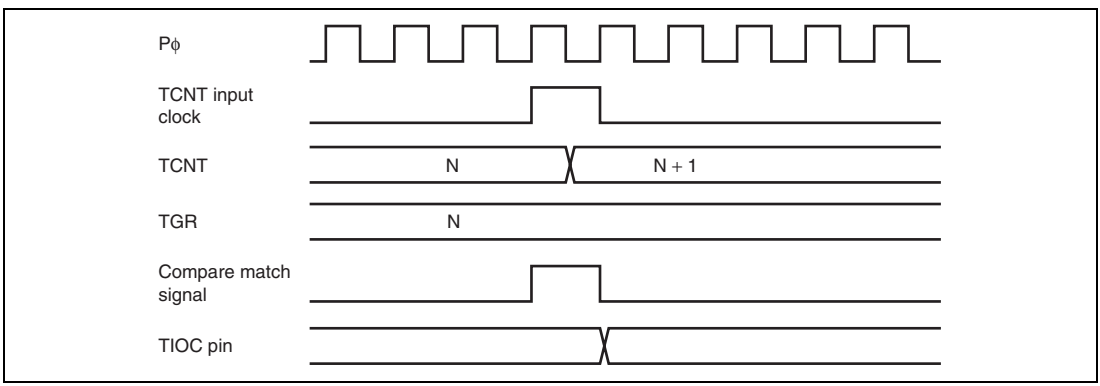


Figure 13.33 Output Compare Output Timing

- NDRH_1

  If pulse output groups 6 and 7 have the same output trigger, all eight bits are mapped to the same address and can be accessed at one time, as shown below.

Bit	Bit Name	Initial Value	R/W	Description
7	NDR31	0	R/W	Next Data Register 31 to 24
6	NDR30	0	R/W	The register contents are transferred to the corresponding PODRH_1 bits by the output trigger specified with PCR_1.
5	NDR29	0	R/W	
4	NDR28	0	R/W	
3	NDR27	0	R/W	
2	NDR26	0	R/W	
1	NDR25	0	R/W	
0	NDR24	0	R/W	

If pulse output groups 6 and 7 have different output triggers, the upper four bits and lower four bits are mapped to different addresses as shown below.

Bit	Bit Name	Initial Value	R/W	Description
7	NDR31	0	R/W	Next Data Register 31 to 28
6	NDR30	0	R/W	The register contents are transferred to the corresponding PODRH_1 bits by the output trigger specified with PCR_1.
5	NDR29	0	R/W	
4	NDR28	0	R/W	
3 to 0	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
3	NDR27	0	R/W	Next Data Register 27 to 24
2	NDR26	0	R/W	The register contents are transferred to the corresponding PODRH_1 bits by the output trigger specified with PCR_1.
1	NDR25	0	R/W	
0	NDR24	0	R/W	

14.3.5 PPG Output Mode Register (PMR)

PMR selects the pulse output mode of the PPG for each group. If inverted output is selected, a low-level pulse is output when PODRH is 1 and a high-level pulse is output when PODRH is 0. If non-overlapping operation is selected, PPG updates its output values at compare match A or B of the TPU that becomes the output trigger. For details, refer to section 14.4.4, Non-Overlapping Pulse Output.

Bit	7	6	5	4	3	2	1	0
Bit Name	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV
Initial Value	1	1	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	G3INV	1	R/W	Group 3 Inversion Selects direct output or inverted output for pulse output group 3. 0: Inverted output 1: Direct output
6	G2INV	1	R/W	Group 2 Inversion Selects direct output or inverted output for pulse output group 2. 0: Inverted output 1: Direct output
5	G1INV	1	R/W	Group 1 Inversion Selects direct output or inverted output for pulse output group 1. 0: Inverted output 1: Direct output
4	G0INV	1	R/W	Group 0 Inversion Selects direct output or inverted output for pulse output group 0. 0: Inverted output 1: Direct output

14.4.8 Pulse Output Triggered by Input Capture

Pulse output of PPG0 can be triggered by TPU0 input capture as well as by compare match. If TGRA functions as an input capture register in the TPU0 channel selected by PCR, pulse output will be triggered by the input capture signal.

Figure 14.14 shows the timing of this output.

PPG1 cannot be used to trigger pulse output by input capturer.

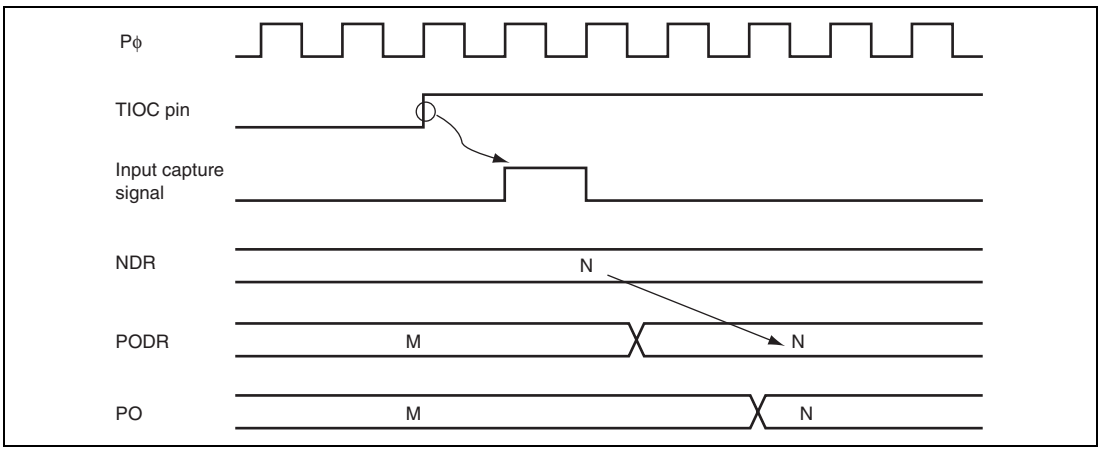


Figure 14.14 Pulse Output Triggered by Input Capture (Example)

(3) Pin Output

- Control of output from the TMO0 pin by the bits OS3 to OS0 in TCSR_0 is in accordance with the 16-bit compare match conditions.
- Control of output from the TMO1 pin by the bits OS3 to OS0 in TCSR_1 is in accordance with the lower 8-bit compare match conditions.

15.6.2 Compare Match Count Mode

When the bits CKS2 to CKS0 in TCR_1 are set to B'100, TCNT_1 counts compare match A for channel 0. Channels 0 and 1 are controlled independently. Conditions such as setting of the CMF flag, generation of interrupts, output from the TMO pin, and counter clear are in accordance with the settings for each channel.

15.7 Interrupt Sources

15.7.1 Interrupt Sources and DTC Activation

- Interrupt in unit 0 and unit 1

There are three interrupt sources for the 8-bit timer (TMR_0 or TMR_1): CMIA, CMIB, and OVI. Their interrupt sources and priorities are shown in Table 15.6. Each interrupt source is enabled or disabled by the corresponding interrupt enable bit in TCR or TCSR, and independent interrupt requests are sent for each to the interrupt controller. It is also possible to activate the DTC by means of CMIA and CMIB interrupts (This is available in unit 0 and unit 1 only).

Table 15.6 8-Bit Timer (TMR_0 or TMR_1) Interrupt Sources (in Unit 0 and Unit 1)

Signal Name	Name	Interrupt Source	Interrupt Flag	DTC Activation	Priority
CMIA0	CMIA0	TCORA_0 compare match	CMFA	Possible	High
CMIB0	CMIB0	TCORB_0 compare match	CMFB	Possible	↑
OVI0	OVI0	TCNT_0 overflow	OVF	Not possible	Low
CMIA1	CMIA1	TCORA_1 compare match	CMFA	Possible	High
CMIB1	CMIB1	TCORB_1 compare match	CMFB	Possible	↑
OVI1	OVI1	TCNT_1 overflow	OVF	Not possible	Low

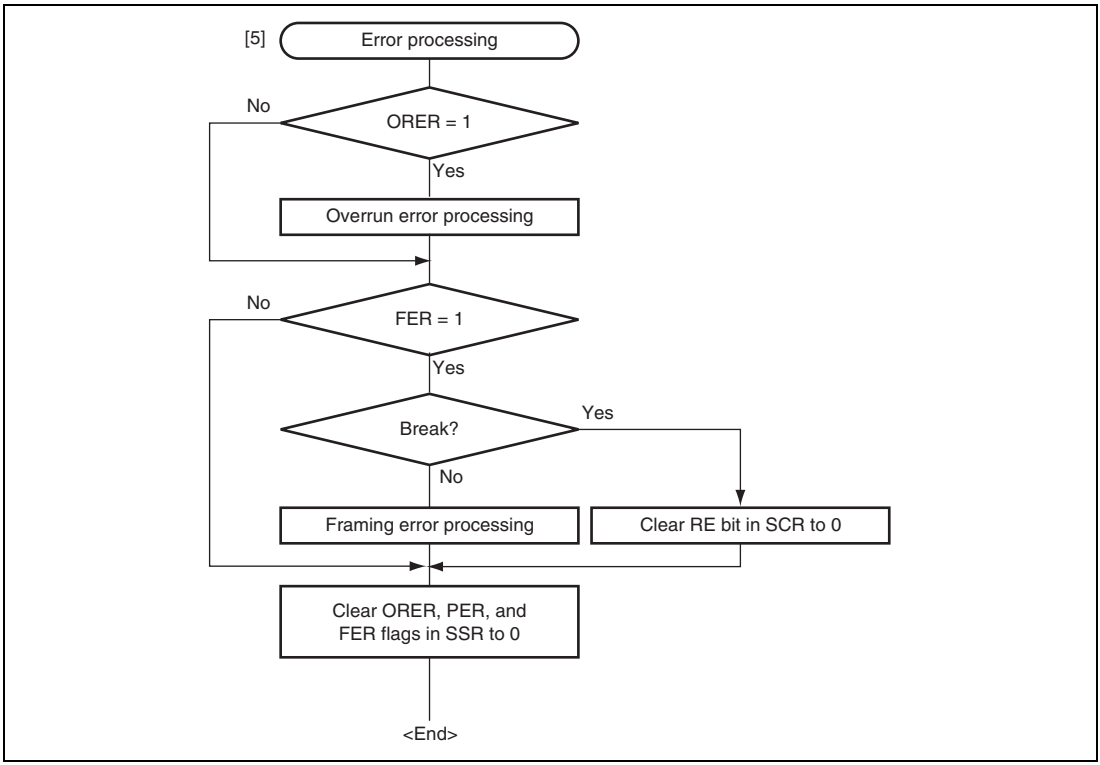


Figure 17.16 Sample Multiprocessor Serial Reception Flowchart (2)

18.4.2 Master Transmit Operation

In I²C bus format master transmit mode, the master device outputs the transmit clock and transmit data, and the slave device return an acknowledge signal. Figures 18.5 and 18.6 show the operating timings in master transmit mode. The transmission procedure and operations in master transmit mode are described below.

1. Set the ICR bit in the corresponding register to 1. Set the ICE bit in ICCRA to 1. Set the WAIT bit in ICMR and the CKS3 to CKS0 bits in ICCRA to 1. (initial setting)
2. Read the BSSY flag in ICCRB to confirm that the bus is free. Set the MST and TRS bits in ICCRA to select master transmit mode. Then, write 1 to BBSY and 0 to SCP using the MOV instruction. (The start condition is issued.) This generates the start condition.
3. After confirming that TDRE in ICSR has been set, write the transmit data (the first byte shows the slave address and R/W) to ICDRT. After this, when TDRE is automatically cleared to 0, data is transferred from ICDRT to ICDRS. TDRE is set again.
4. When transmission of one byte data is completed while TDRE is 1, TEND in ICSR is set to 1 at the rising of the ninth transmit clock pulse. Read the ACKBR bit in ICIER to confirm that the slave device has been selected. Then, write the second byte data to ICDRT. When ACKBR is 1, the slave device has not been acknowledged, so issue a stop condition. To issue the stop condition, write 0 to BBSY and SCP using the MOV instruction. SCL is fixed to a low level until the transmit data is prepared or the stop condition is issued.
5. The transmit data after the second byte is written to ICDRT every time TDRE is set.
6. Write the number of bytes to be transmitted to ICDRT. Wait until TEND is set (the end of last byte data transmission) while TDRE is 1, or wait for NACK (NACKF in ICSR is 1) from the receive device while ACKE in ICIER is 1. Then, issue the stop condition to clear TEND or NACKF.
7. When the STOP bit in ICSR is set to 1, the operation returns to the slave receive mode.

3. All peripheral modules enter the reset state.
4. "Functioning" or "Halted" is selectable through the setting of bits MSTPA9 and MSTPA8 in MSTPCRA.
5. "Retained" or "Undefined" of the contents of RAM is selected by the setting of the bits RAMCUT2 to RAMCUT0 in DPSBYCR.
6. Retention or high-impedance for the address bus and bus-control signals ($\overline{CS0}$ to $\overline{CS7}$, $\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$) is selected by the setting of the OPE bit in SBYCR.
7. Some peripheral modules enter a state where the register values are retained.
8. External interrupt, voltage monitoring interrupt*[9]
9. Supported only by the H8SX/1638L Group.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
SMR_1*[1]	C/$\overline{A}$ (GM)	CHR (BLK)	PE (PE)	O/$\overline{E}$ (O/$\overline{E}$)	STOP (BCP1)	MP (BCP0)	CKS1	CKS0	SCI_1
BRR_1									
SCR_1*[1]	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_1									
SSR_1*[1]	TDRE	RDRF	ORER	FER (ERS)	PER	TEND	MPB	MPBT	
RDR_1									
SCMR_1	—	—	—	—	SDIR	SINV	—	SMIF	
ADDRA_0									A/D_0
ADDRB_0									
ADDRC_0									
ADDRD_0									
ADDRE_0									
ADDRF_0									
ADDRG_0									
ADDRH_0									
ADCSR_0	ADF	ADIE	ADST	—	CH3	CH2	CH1	CH0	
ADCR_0	TRGS1	TRGS0	SCANE	SCANS	CKS1	CKS0	—	EXTRGS	
TCSR	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	WDT
TCNT									
RSTCSR	WOVF	RSTE	—	—	—	—	—	—	
TCR_0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_0
TCR_1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_1

27.4.2 Control Signal Timing

Table 27.7 Control Signal Timing

Conditions: V_{CC} = $PLLV_{CC}$ = 3.0 V to 3.6 V*, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, Iϕ = 8 MHz to 50 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	ns	Figure 27.6
$\overline{RES}$ pulse width	t_{RESW}	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	ns	Figure 27.7
NMI hold time	t_{NMIH}	10	—	ns	
NMI pulse width (after leaving software standby mode)	t_{NMIW}	200	—	ns	
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	ns	
$\overline{IRQ}$ pulse width (after leaving software standby mode)	t_{IRQW}	200	—	ns	

Note: * Vcc=PLLVcc=2.95 to 3.6V in the H8SX/1638L Group.

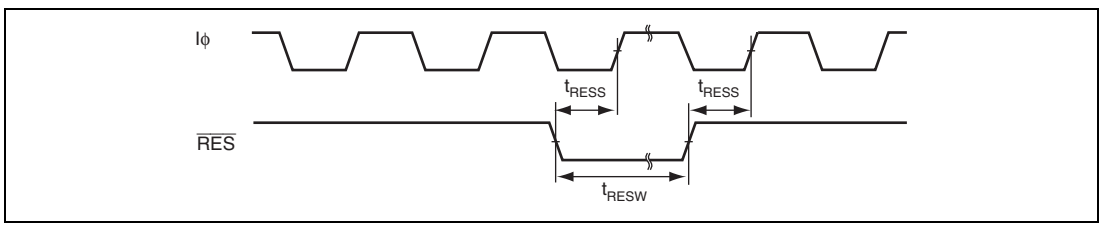


Figure 27.6 Reset Input Timing

Item	Page	Revision (See Manual for Details)
Section 26. List of Registers	992	Added

Deep standby backup register 0	DPSBKR0	8	H'FFBF0	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 1	DPSBKR1	8	H'FFBF1	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 2	DPSBKR2	8	H'FFBF2	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 3	DPSBKR3	8	H'FFBF3	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 4	DPSBKR4	8	H'FFBF4	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 5	DPSBKR5	8	H'FFBF5	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 6	DPSBKR6	8	H'FFBF6	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 7	DPSBKR7	8	H'FFBF7	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 8	DPSBKR8	8	H'FFBF8	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 9	DPSBKR9	8	H'FFBF9	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 10	DPSBKR 10	8	H'FFBFA	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 11	DPSBKR 11	8	H'FFBFB	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 12	DPSBKR 12	8	H'FFBFC	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 13	DPSBKR 13	8	H'FFBFD	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 14	DPSBKR 14	8	H'FFBFE	SYSTEM	8	2Iφ/3Iφ
Deep standby backup register 15	DPSBKR 15	8	H'FFBFF	SYSTEM	8	2Iφ/3Iφ