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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	250MHz
Non-Volatile Memory	External
On-Chip RAM	112kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56724ag

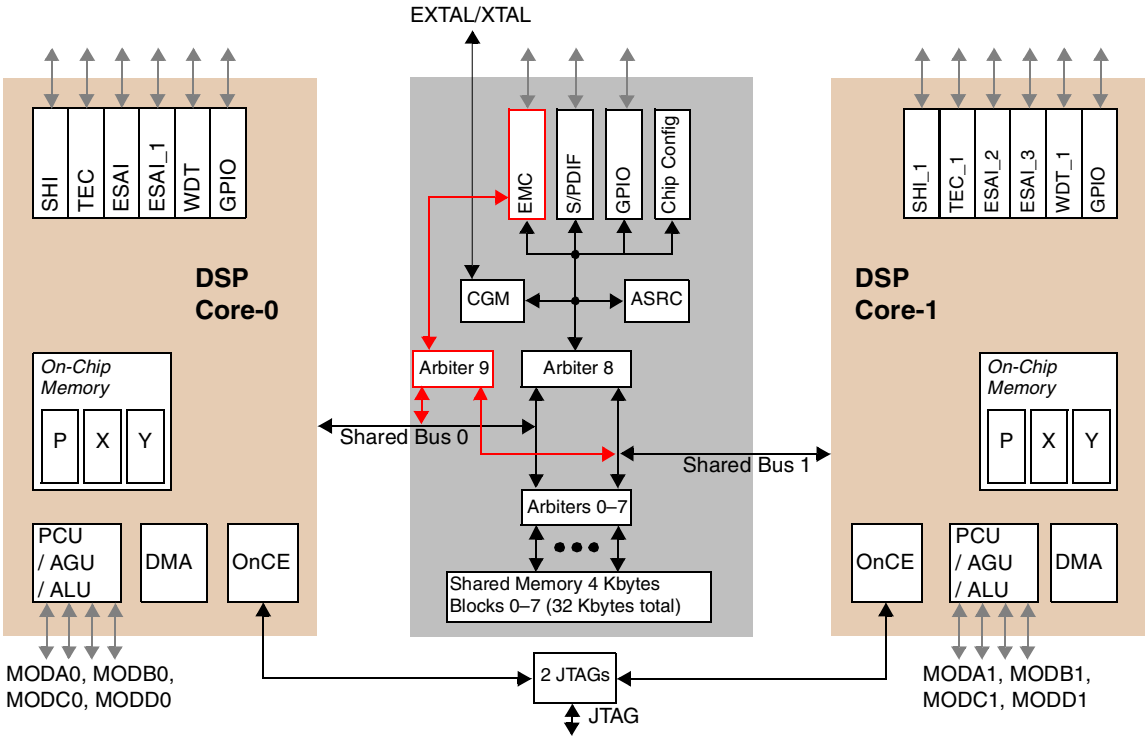


Figure 1. DSP56724 Block Diagram

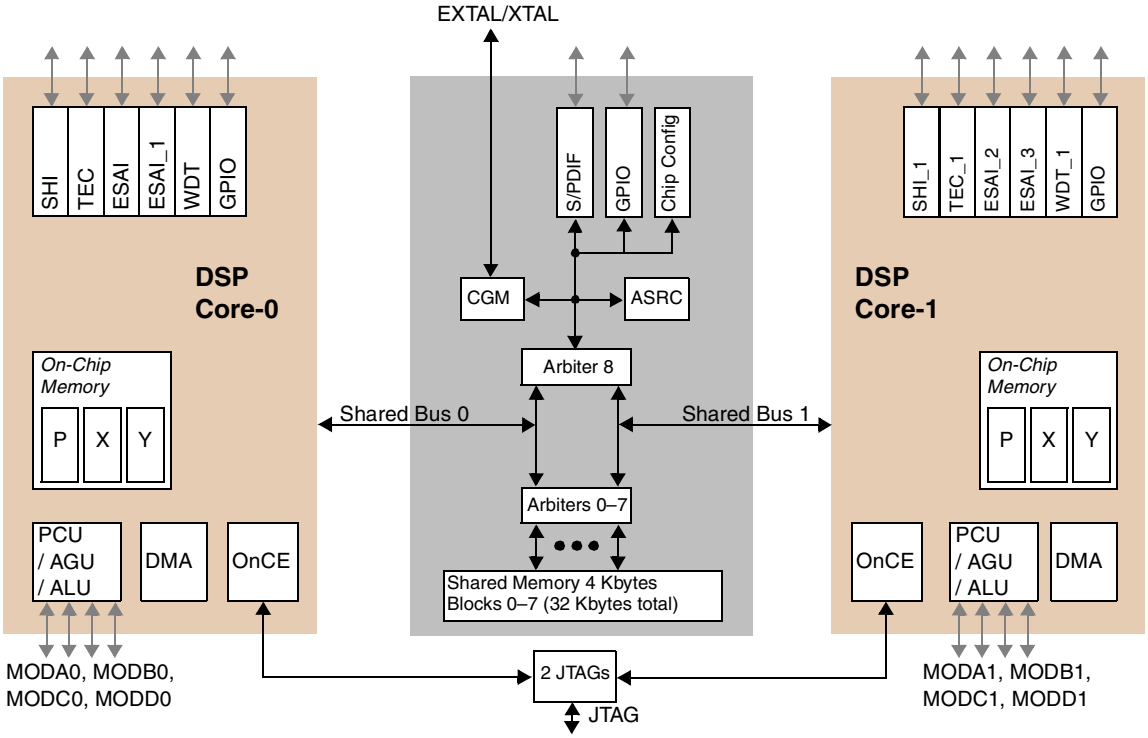


Figure 2. DSP56725 Block Diagram

1 Electrical Characteristics

1.1 Chip-Level Conditions

Table 1 provides a quick reference to the subsections in this section.

Table 1. Chip-Level Conditions

For	See
Section 1.1.1, “Maximum Ratings”	on page 4
Section 1.1.2, “Thermal Characteristics”	on page 6
Section 1.1.3, “Power Requirements”	on page 6
Section 1.1.5, “DC Electrical Characteristics”	on page 8
Section 1.1.6, “AC Electrical Characteristics”	on page 9
Section 1.1.7, “Internal Clocks”	on page 9
Section 1.1.8, “External Clock Operation”	on page 10
Section 1.1.9, “Reset, Stop, Mode Select, and Interrupt Timing”	on page 11

1.1.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{DD}). The suggested value for a pull-up or pull-down resistor is 4.7 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 4. DC Electrical Characteristics (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Internal supply current[1] (core only) operating at Fsys < 250 MHz					
• In Normal mode	I_{CCI}	—	140	340	mA
• In Wait mode	I_{CCW}	—	90	290	mA
• In Stop mode[2]	I_{CCS}	—	40	240	mA
Input capacitance	C_{IN}	—	—	10	pF

Note:

1. The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (for example, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current with Fsys < 200 MHz is measured with V_{CORE_VDD} = 1.0 V, V_{DD_IO} = 3.3 V at T_J = 25° C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.05 V, $V_{IO\_VDD)}$ = 3.6 V at T_J = 100° C. Typical internal supply current with Fsys < 250 MHz is measured with V_{CORE_VDD} = 1.2 V, V_{DD_IO} = 3.3 V at T_J = 25° C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.26 V, $V_{IO\_VDD)}$ = 3.6 V at T_J = 90° C.
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (that is, not allowed to float).

1.1.6 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. For all pins, output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

1.1.7 Internal Clocks

Table 5 lists the internal clocks.

Table 5. Internal Clocks

No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
1	Comparison Frequency	Fref	2	—	8	MHz	Fref = Fin/NR
2	Input Clock Frequency • with PLL enabled • with PLL disabled	Fin	 2 —	—	 248 200	MHz	—

Table 5. Internal Clocks (Continued)

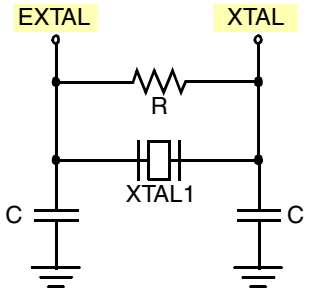
No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
3	PLL VCO Frequency	Fvco	200	—	500	MHz	Fvco = (Fin * NF)/NR
4	Output Clock Frequency [1] [2] • with PLL enabled • with PLL disabled	Fout	 25 —	—	 200 or 250 200 or 250	MHz	 Fout = Fvco/NO Fout = Fin
5	System Clock Frequency • with PLL enabled[2] • with PLL disabled	Fsys	 0.195 0	—	 200 or 250 200	MHz	 Fsys = Fout/2^{DF} Fsys = Fout

Note:

1. Fin = External frequency
   NF = Multiplication Factor
   NR = Predivision Factor
   NO = Output Divider
   DF = Division Factor
2. Maximum frequency of 200 MHz supported at 0.95 V < V_{VDD_CORE} < 1.05 V and –40 < Tj < 100° C
   Maximum frequency of 250 MHz supported at 1.14 V < V_{VDD_CORE} < 1.26 V and 0 < Tj < 90° C

1.1.8 External Clock Operation

The DSP56724/DSP56725 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; see Figure 6.



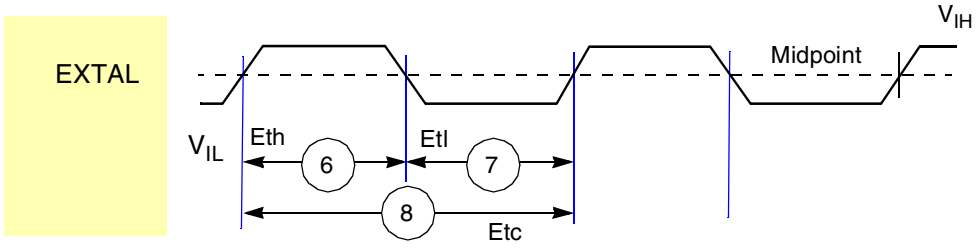
Suggested component values:

f_{osc} = 24.576 MHz
R = 1 M ±10%
C (EXTAL)= 18 pF
C (XTAL) = 18 pF

Calculations are for a 5–30 MHz crystal with the following parameters:
- shunt capacitance (C_0) of 10 pq–F12 pF
- series resistance 40 Ohm
- drive level of 10 µW

Figure 6. Using the On-Chip Oscillator

If the DSP56724/DSP56725 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 7). When the external square wave source is connected to EXTAL, the XTAL pin is not used.



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 7. External Clock Timing

Table 6 lists the clock operation.

Table 6. Clock Operation

No.	Characteristics	Symbol	Min	Max	Units
6	EXTAL input high [1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Eth	 16.67 2.5	 100 inf	ns
7	EXTAL input low[1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Etl	 16.67 2.5	 100 inf	ns
8	EXTAL cycle time • With PLL disabled • With PLL enabled	Etc	 5 33.3	 inf 500	ns
9	Instruction cycle time • With PLL disabled • With PLL enabled	Tc	 5 4[4]	 inf 5120	ns

Note:

1. Measured at 50% of the input transition.
2. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.
3. Maximum frequency of 200 MHz supported at 0.95 V < V_{VDD_CORE} < 1.05 V and –40 < Tj < 100° C
   Maximum frequency of 250 MHz supported at 1.14 V < V_{VDD_CORE} < 1.26 V and 0 < Tj < 90° C
4. PLL_{LOCK} = 200 µs.

1.1.9 Reset, Stop, Mode Select, and Interrupt Timing

Table 7 lists the reset, stop, mode select, and interrupt timing.

Table 7. Reset, Stop, Mode Select, and Interrupt Timing

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled	 $2 \times T_C$ $2 \times T_C$	 10 10	 — —	 ns ns
13	Syn reset deassert delay time • Minimum • Maximum (PLL enabled)	 $2 \times T_C$ $(2xT_C)+PLL_{LOCK}$	 10 200	 — —	 ns us
14	Mode select setup time	—	10	—	ns
15	Mode select hold time	—	12	—	ns
16	Minimum edge-triggered interrupt request assertion width	—	7	—	ns
17	Minimum edge-triggered interrupt request deassertion width	—	4	—	ns
18	Delay from interrupt trigger to interrupt code execution	$10 \times T_{C+4}$	54	—	ns

Table 9. Serial Host Interface SPI Protocol Timing (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	$2.0 \times T_C + 2$	35	—	ns
			Very Narrow	$2.0 \times T_C + 1$	25	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
	CPHA = 1	Slave	Bypassed	—	10	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	—	12	—	ns
			Very Narrow	—	22	—	ns
			Narrow	—	100	—	ns
			Wide	—	200	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	—	0	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
30	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	$2 \times T_C + 10$	20	—	ns
			Very Narrow	$2 \times T_C + 30$	40	—	ns
			Narrow	$2 \times T_C + 60$	70	—	ns
			Wide	—	100.0	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	—	—	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	—	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	—	—	45	ns
			Very Narrow	—	—	110	ns
			Narrow	—	—	135	ns
			Wide	—	—	225	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	—	10	—	ns
			Very Narrow	—	15	—	ns
			Narrow	—	55	—	ns
			Wide	—	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	14.0	ns

Figure 13 shows the SPI master timing (CPHA = 1).

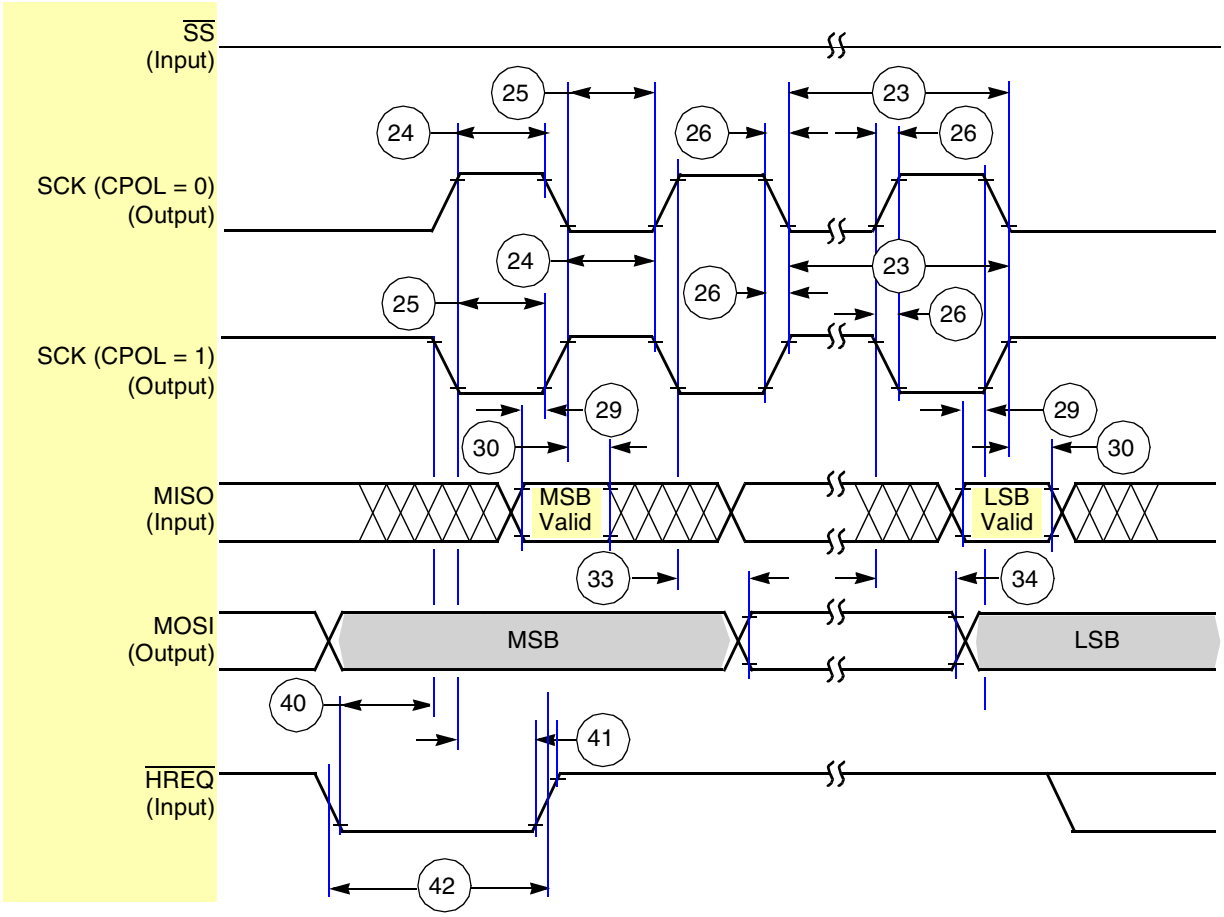


Figure 13. SPI Master Timing (CPHA = 1)

Figure 14 shows the SPI slave timing (CPHA = 0).

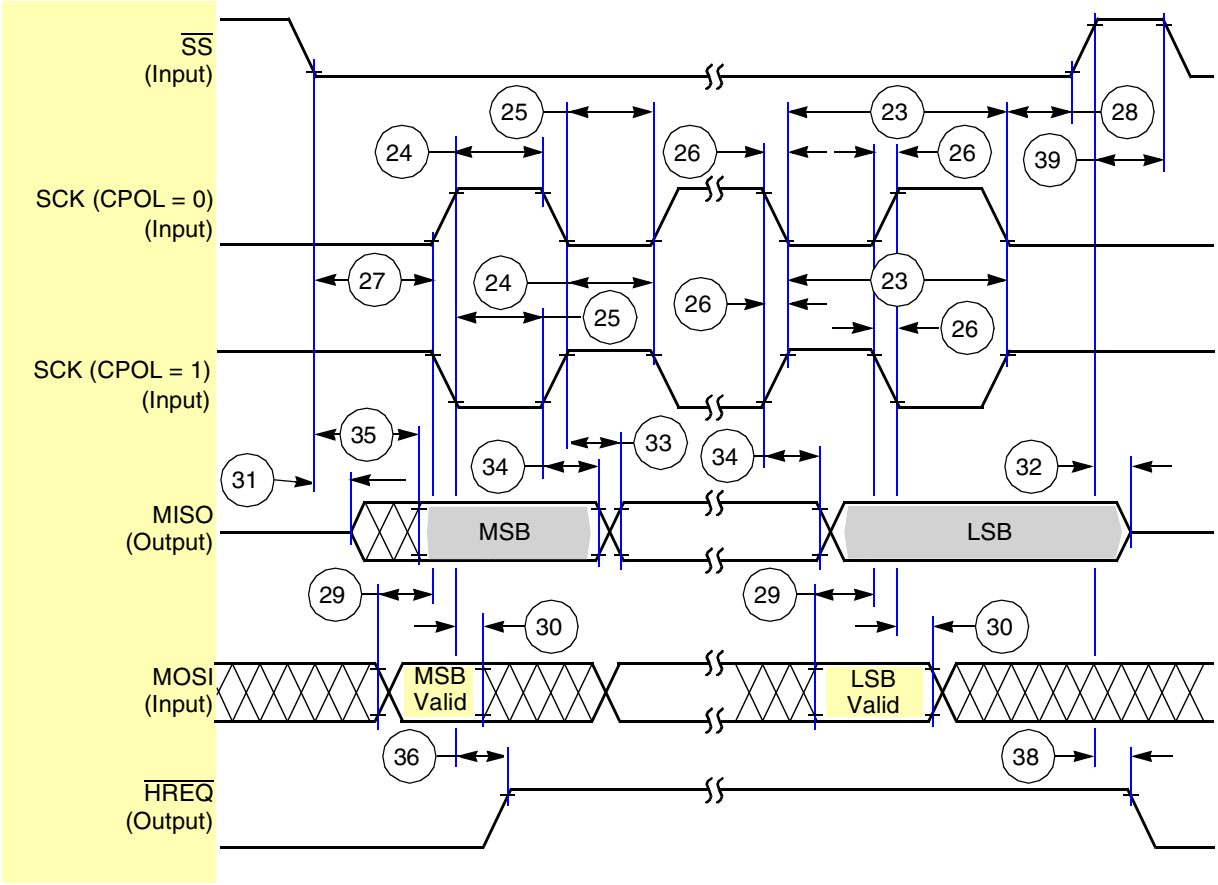


Figure 14. SPI Slave Timing (CPHA = 0)

Figure 15 shows the SPI slave timing (CPHA = 1).

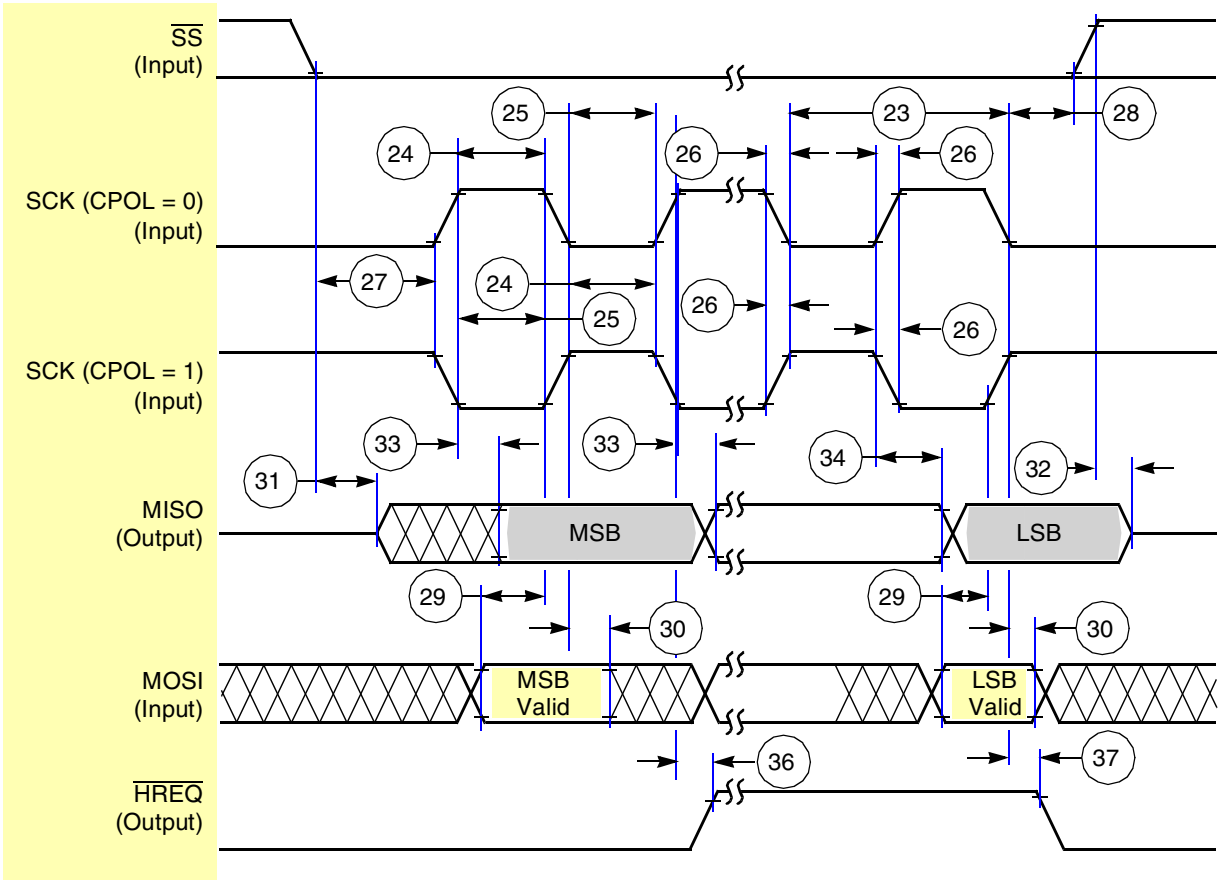


Figure 15. SPI Slave Timing (CPHA = 1)

1.2.2 Serial Host Interface (SHI) I²C Protocol Timing

Table 10 lists the SHI I²C protocol timing diagram.

Table 10. SHI I²C Protocol Timing

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
XX	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	—	 — — — —	 0 10 50 100	 — — — —	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs

Table 10. SHI I²C Protocol Timing (Continued)

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
60	$\overline{\text{HREQ}}$ in assertion to first SCL edge • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	$T_{AS;RQI}$	 4327 4317 4282 4227	 — — — —	 927 917 877 827	 — — — —	 ns ns ns ns
61	First SCL edge to $\overline{\text{HREQ}}$ is not asserted ($\overline{\text{HREQ}}$ in hold time.)	$t_{HO;RQI}$	0.0	—	0.0	—	ns

Note:

1. V_{CORE_VDD} = 1.00± 0.05 V; T_J = –40° C to 100° C, C_L = 50 pF
2. Pull-up resistor: R_P (min) = 1.5 kΩ
3. Capacitive load: C_b (max) = 50 pF
5. All times assume noise free inputs
5. All times assume internal clock frequency of 200 MHz
6. SHI_1 specs match those of SHI
7. The numbers listed are based on the module/pad design and its characteristics during output. The module is compliant with I²C standard, so the module should receive I²C bus compliant signal without any issue.

1.2.3 Programming the SHI I²C Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)] \quad \textit{Eqn. 4}$$

where

— HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.

— HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I²C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \quad \text{(if HDM[7:0] = \$02 and HRS = 1)} \quad \textit{Eqn. 5}$$

to

$$4096 \times T_C \quad \text{(if HDM[7:0] = \$FF and HRS = 0)} \quad \textit{Eqn. 6}$$

The programmed serial clock cycle (T_{I^2CCP}) should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in next.

$$T_{I^2CCP} + 3 \times T_C + 45ns + T_R \quad \text{(Nominal, SCL Serial Clock Cycle (TSCL) generated as master)} \quad \textit{Eqn. 7}$$

Table 11. Enhanced Serial Audio Interface Timing (Continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	0.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge [6]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT rising edge to FST out (bl) high	—	—	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[6]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	15.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	15.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	17.0 11.0	x ck i ck	ns
86	SCKT rising edge to data out valid	—	—	— —	25.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance[7]	—	—	— —	25.0 16.0	x ck i ck	ns
88	SCKT rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	14.0 9.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	—	—	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	—	—	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	—	—	4.0 5.0	— —	x ck i ck	ns

Figure 18 shows the ESAI receiver timing diagram.

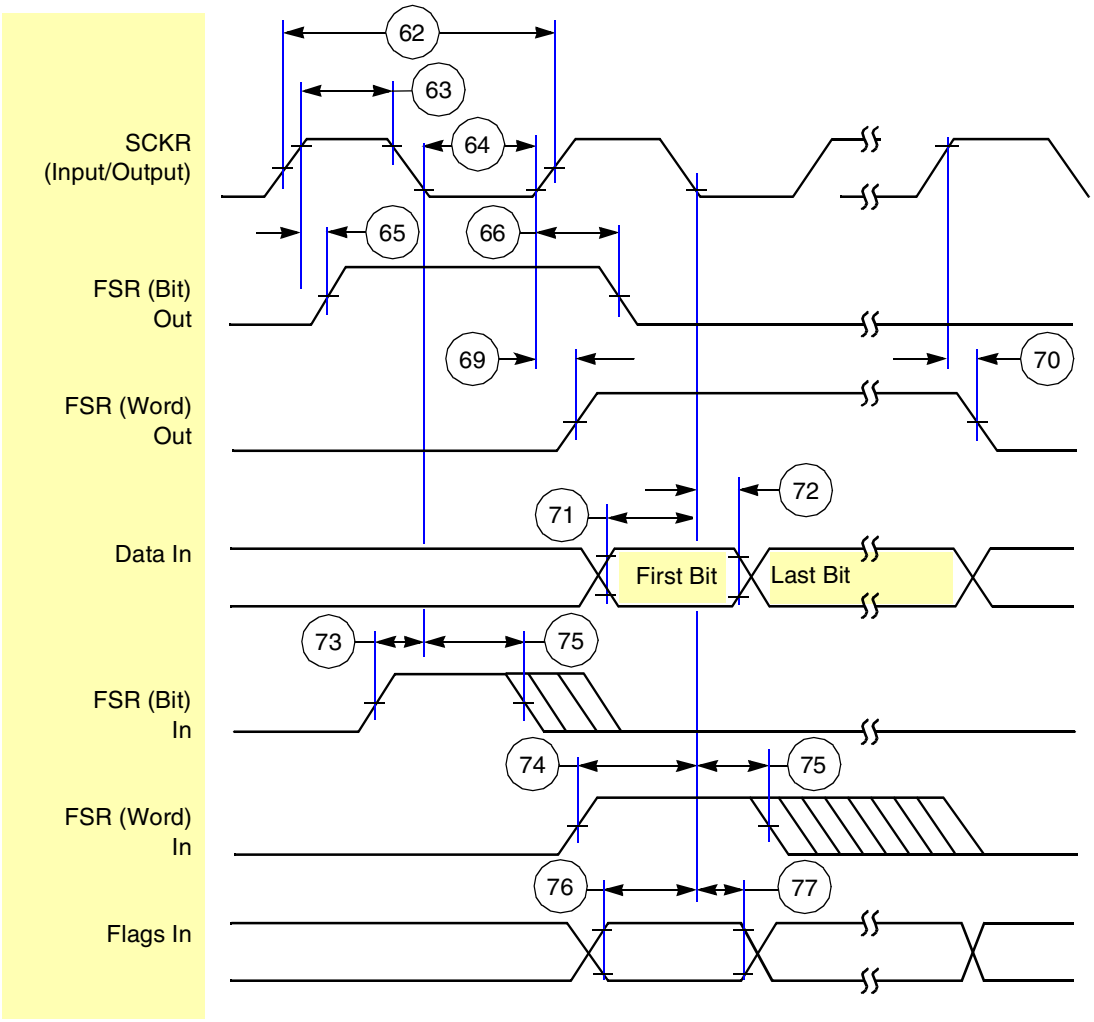


Figure 18. ESAI Receiver Timing

Figure 19 shows the ESAI HCKT timing diagram.

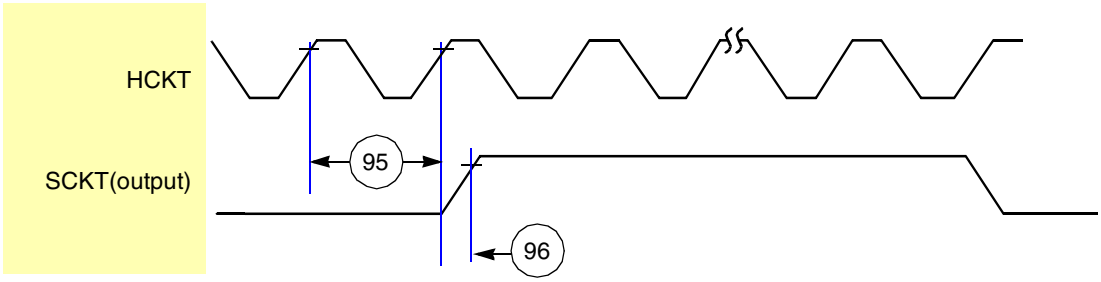


Figure 19. ESAI HCKT Timing

Figure 24 shows the test access port timing diagram.

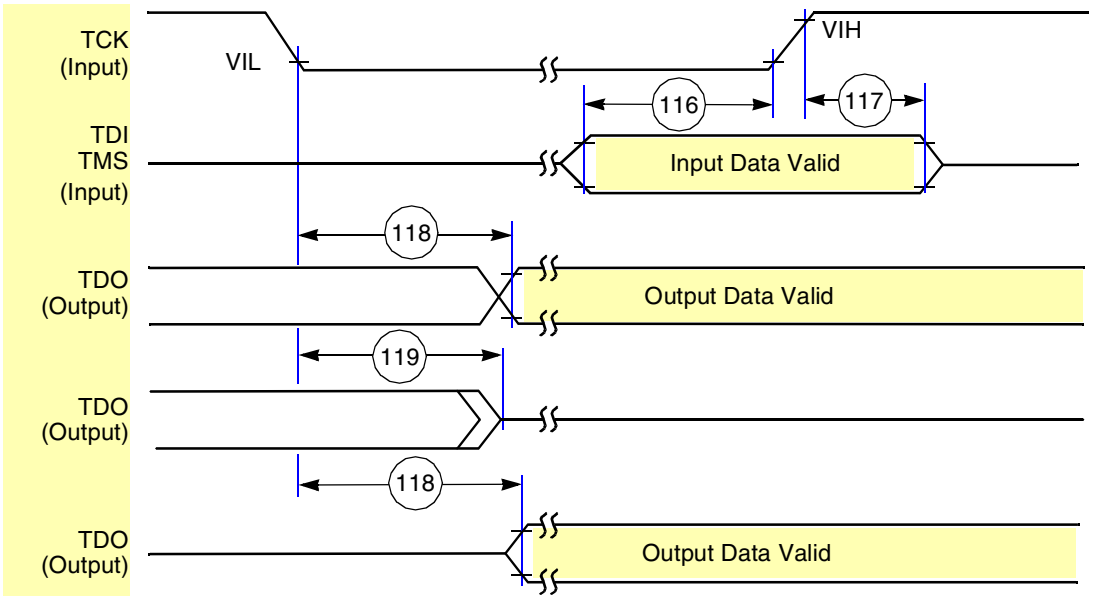


Figure 24. Test Access Port Timing Diagram

1.2.7 Watchdog Timer Timing

Table 14 lists the watchdog timer timings.

Table 14. Watchdog Timer Timing

No.	Characteristics	Expression	Min	Max	Unit
120	Delay from time-out to fall of $\overline{WDT}$, $\overline{WDT\_1}$	$2 \times T_C$	10.0	—	ns
121	Delay from timer clear to rise of $\overline{WDT}$, $\overline{WDT\_1}$	$2 \times Tc$	10.0	—	ns

Table 17 lists the EMC timing parameters with EMC PLL bypassed.

Table 17. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 4)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	$4 \times T_C$	—	ns
Input setup to LCLK (except $\overline{\text{LGTA}}$/LUPWAIT)	T_{in_s}	8	—	ns
Input hold from LCLK (except $\overline{\text{LGTA}}$/LUPWAIT)[1]	T_{in_h}	–1	—	ns
$\overline{\text{LGTA}}$ valid time	T_{gta}	22	—	ns
LUPWAIT valid time	T_{upwait}	22	—	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	4	—	ns
LALE valid time	T_{ale}	14	—	ns
Output setup from LCLK (except LAD[23:0] and LALE)	T_{out_s}	9	—	ns
Output hold from LCLK (except LAD[23:0] and LALE)	T_{out_h}	8	—	ns
LAD[23:0] output setup from LCLK	T_{ad_s}	8	—	ns
LAD[23:0] output hold from LCLK	T_{ad_h}	7	—	ns
LCLK to output high impedance for LAD[23:0]	T_{ad_z}	—	8.1	ns

Note: Negative hold time means the signal could be invalid before LCLK rising edge.

Figure 28 shows the EMC signals diagram, with EMC PLL bypassed.

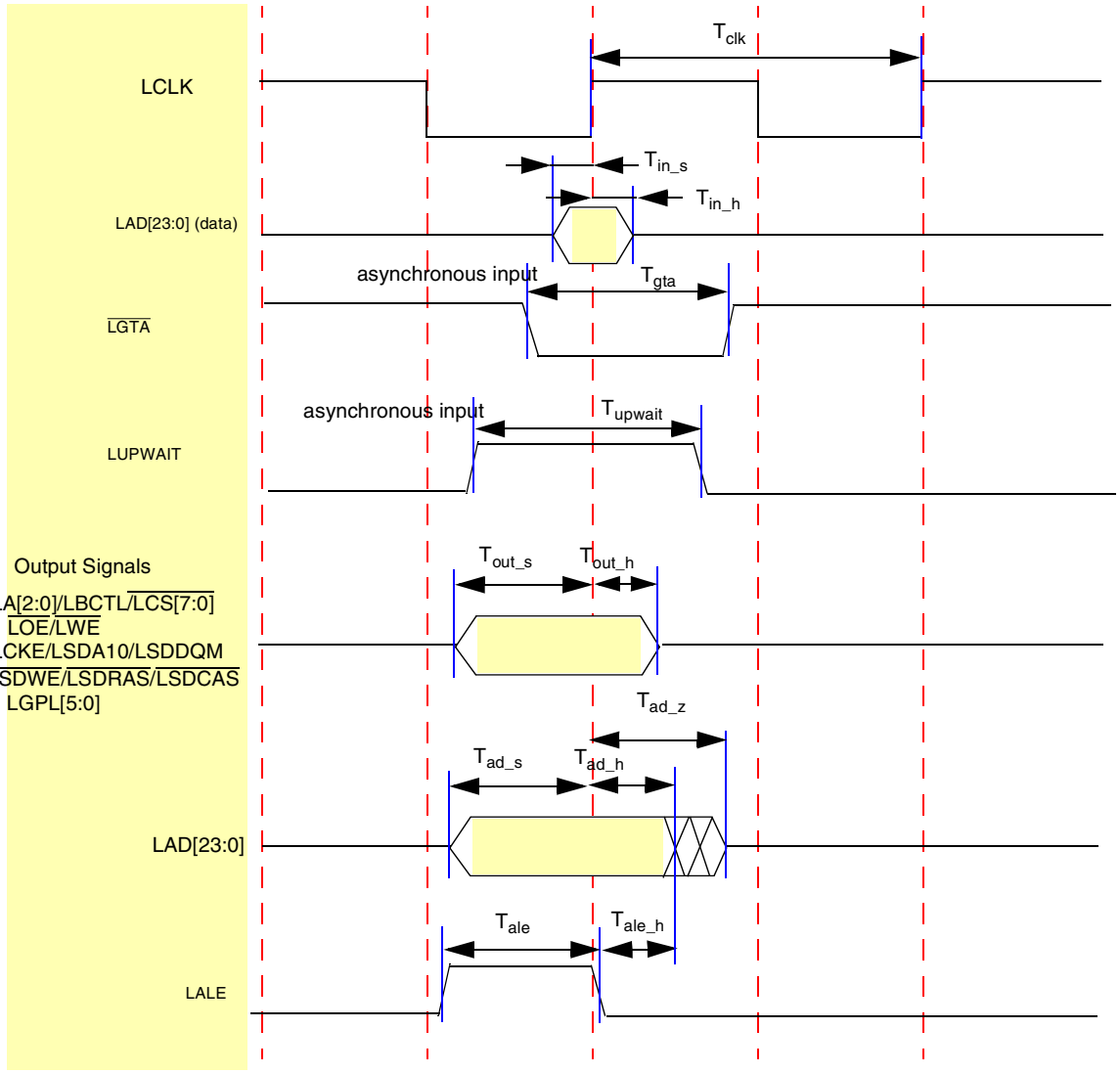


Figure 28. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 4

Table 18 lists the EMC timing parameters with EMC PLL bypassed.

Table 18. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	$8 \times T_C$	—	ns
Input setup to LCLK (except $\overline{\text{LGTA}}$/LUPWAIT)	T_{in_s}	8	—	ns
Input hold from LCLK (except $\overline{\text{LGTA}}$/LUPWAIT)[1]	T_{in_h}	–1	—	ns
$\overline{\text{LGTA}}$ valid time	T_{gta}	42	—	ns
LUPWAIT valid time	T_{upwait}	42	—	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	5	—	ns
LALE valid time	T_{ale}	34	—	ns

4.1.2 Pinout for DSP56725 80-Pin Plastic LQFP Package

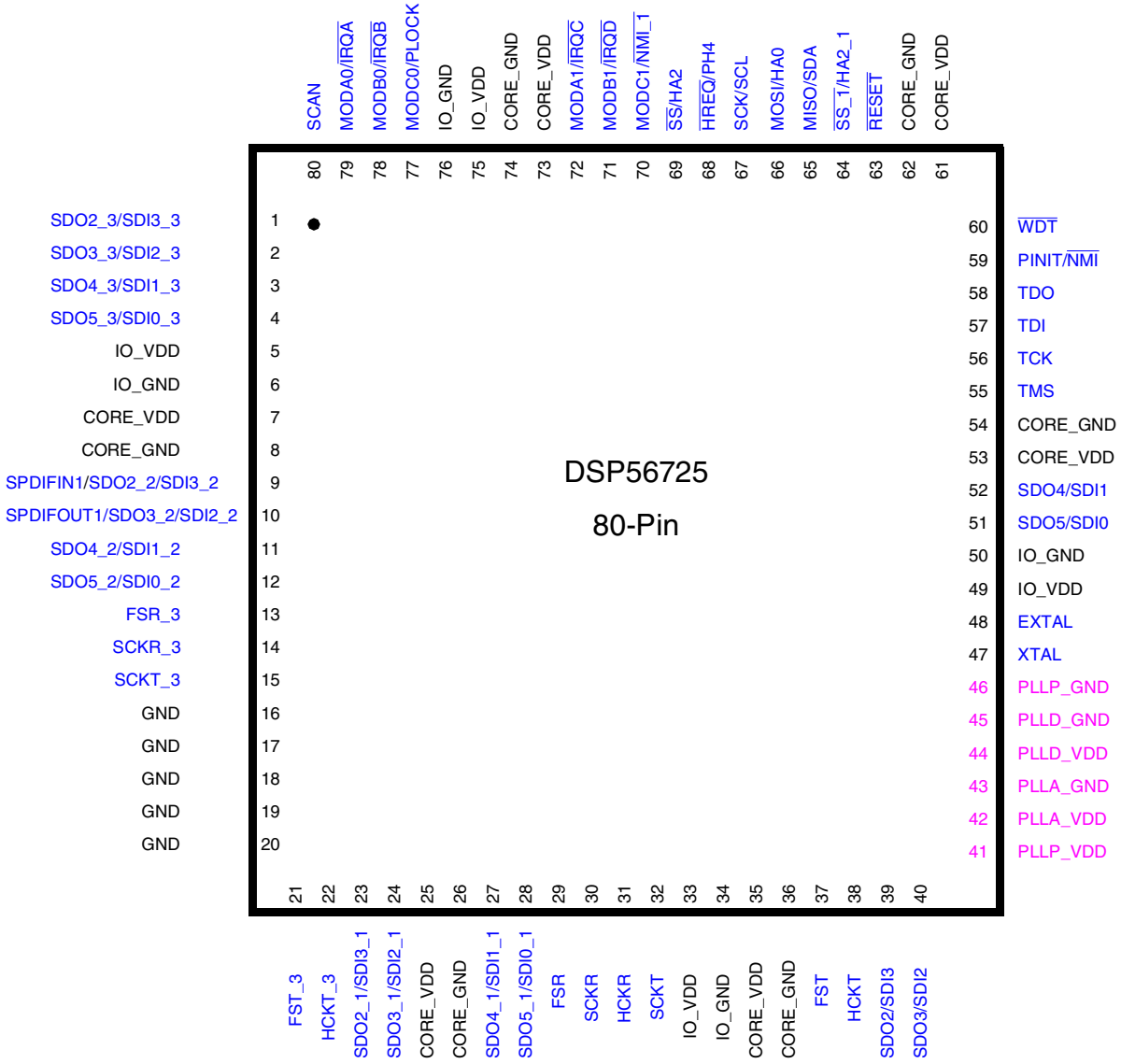


Figure 31. DSP56725 80-Pin Package

4.1.3 Pin Multiplexing

Many pins are multiplexed, and depending on the selected configuration, can be one of three possible signals. For more about pin multiplexing, refer to the *Symphony™ DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual* (DSP56724RM).

4.2 144-Pin Package Outline Drawing

The 144-pin package outline drawing is shown in Figure 32 and Figure 33.

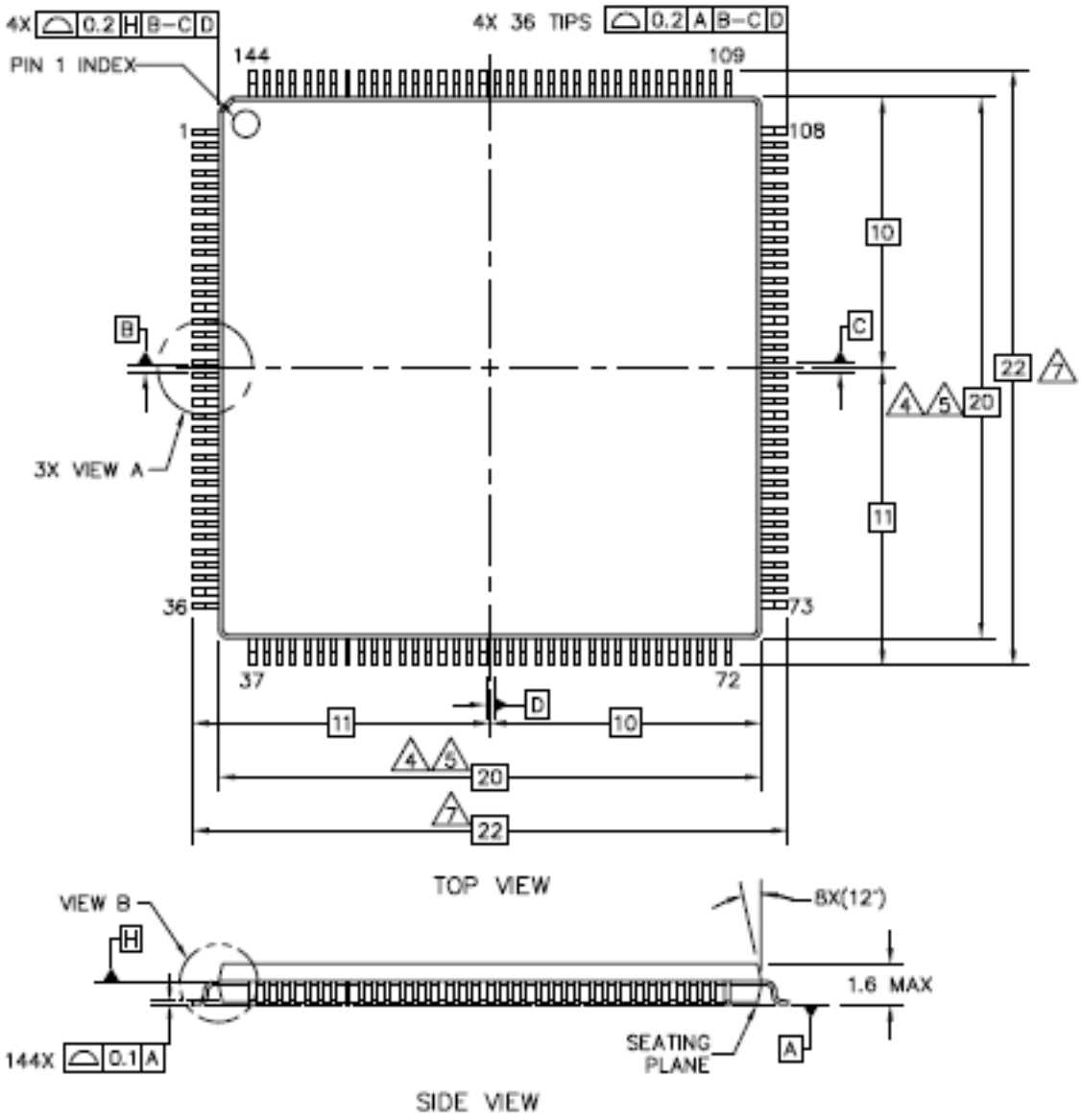


Figure 32. 144-Pin Package Outline Drawing

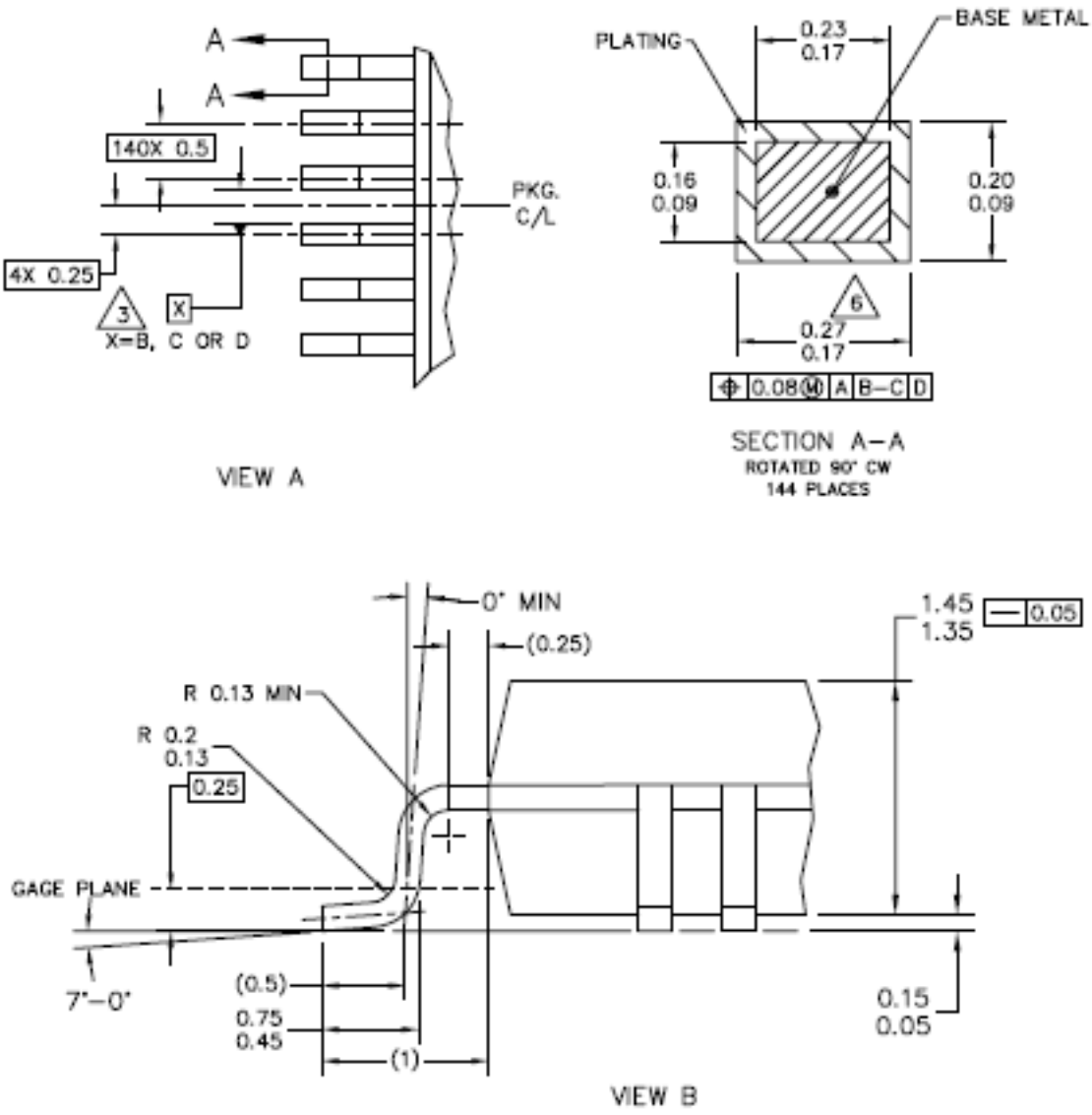


Figure 33. 144-Pin Package Outline Drawing (continued)

FIGURE NOTES:

1 All dimensions are in millimeters.

2 Interpret dimensions and tolerances per ASME Y.14.5M–1994

3 Datums B, C and D to be determined at datum plane H.

4 The top package body size may be smaller than the bottom package size by a maximum of 0.1 mm.

5 These dimensions do not include mold protrusions. The maximum allowable protrusion is 0.25 mm per side. These dimensions are maximum body size dimensions including mold mismatch.

6 This dimension does not include dam bar protrusion. Protrusions shall not cause the lead width to exceed 0.35 mm. Minimum space between protrusion and an adjacent lead shall be 0.07 mm.

7 These dimensions are determined at the seating plane, datum A.

5 Product Documentation

Table 21 lists the documents that provide a complete description of the DSP56724/DSP56725 devices and are required to design properly with the part. Documentation is available from a local Freescale Semiconductor, Inc. (formerly Motorola) distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 21. DSP56724 / DSP56725 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56724/DSP56725 Reference Manual	Detailed description of memory, peripherals, and interfaces	DSP56724RM
DSP56724 Product Brief	Brief description of the DSP56724 device	DSP56724PB
DSP56725 Product Brief	Brief description of the DSP56725 device	DSP56725PB
DSP56724/DSP56725 Data Sheet	Electrical and timing specifications; pin and package descriptions (this document)	DSP56724

6 Revision History

Table 22 summarizes revisions to this document.

Table 22. Revision History

Revision	Date	Description
2	3/2009	• Added Section 1.1.4, “Power Consumption Considerations.” • In Table 9, “Serial Host Interface SPI Protocol Timing,” updated values for Nos. 24, 25, 27, 33, 34, and 39. Removed 40 and renumbered subsequent items accordingly. Updated Figure 12 and Figure 13 to reflect renumbering. • In Table 11, “Enhanced Serial Audio Interface Timing,” for No. 71 changed 12.0 to 0.
1	12/2008	• Modified values and removed rows in Table 4, “DC Electrical Characteristics.” • Removed “IO_VDD_25” from Figure 4, “Prevent High Current Conditions by Applying IO_VDD Before Core_VDD.” • In Table 7, “Reset, Stop, Mode Select, and Interrupt Timing,” for No. 15, changed 10 to 12, and for No. 16, changed 4 to 7. • In Table 9, “Serial Host Interface SPI Protocol Timing,” updated values. • In Table 10, “SHI I2C Protocol Timing,” added note 7 and changed Max values for No. 50 to 1000 and 300; in addition, updated the values for note 1. • In Table 11, “Enhanced Serial Audio Interface Timing,” for No. 82, changed 19 to 15; for No. 83, changed 20 to 15; for No. 86, changed 18 to 25; for No. 87, changed 21 to 25. • Removed Section 1.2.5, “Timer Timing.” • In Table 16, “EMC Timing Parameters (EMC PLL Enabled; LCRR[CLKDIV] = 2),” for “LSYNC_IN (except $\overline{\text{LGTA}}$/LUPWAIT),” changed 2 to 3. • In Table 17, “EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 4),” for “LCLK to output high impedance for LAD [23:0],” changed 9 to 8.1. • In Table 18, “EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8),” for LCLK to output high impedance for LAD [23:0],” changed 19 to 17.1 • In Table 19, “Ordering Information,” added rows for DSPB56724CAG and DSPB56725CAF, and changed “DSPA56724AG” to “DSPB56724AG.”
0	6/2008	• Initial public release.

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