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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Type | Audio Processor |
| Interface | Host Interface, I²C, SAI, SPI |
| Clock Rate | 250MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 112kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-QFP |
| Supplier Device Package | 80-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56725af |

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Table 2 lists the maximum ratings.

**Table 2. Maximum Ratings**

| Rating[1] | Symbol | Value[1, 2] | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CORE\_VDD}$, $V_{PLLD\_VDD}$ | –0.3 to + 1.26 | V |
| | $V_{PLLP\_VDD}$, $V_{IO\_VDD}$, $V_{IO\_VDD\_25}$, $V_{PLLA\_VDD}$ | –0.3 to + 4.0 | V |
| Maximum CORE_VDD power supply ramp time | Tr | 10 | ms |
| Input Voltage per pin excluding VDD and GND | $V_{IN}$ | GND – 0.3 to 5.5 V | V |
| Current drain per pin excluding $V_{DD}$ and GND (Except for pads listed below) | I | 12 | mA |
| LSYNC_OUT | $I_{lsync\_out}$ | 5 | mA |
| LCLK | $I_{lclk}$ | 5 | mA |
| LALE | $I_{ale}$ | 5 | mA |
| TDO | $I_{JTAG}$ | 12 | mA |
| Operating temperature range<br>• Fsys < 200 MHz<br>• Fsys < 250 MHz | $T_J$ | <br>–40 to +100<br>0 to 90 | °C |
| Storage temperature | $T_{STG}$ | –65 to +150 | °C |
| ESD protected voltage (Human Body Model) | — | 2000 | V |
| ESD protected voltage (Charged Device Model)<br>• All pins<br>• Corner pins | — | <br>500<br>750 | V |

**Note:**

1. GND = 0 V, $T_J$ = –40° C to 100° C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

**Table 7. Reset, Stop, Mode Select, and Interrupt Timing (Continued)**

| No. | Characteristics | Expression | Min | Max | Unit |
|---|---|---|---|---|---|
| 19 | Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[1, 2, 3] | | | | |
| | • PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0) | (128 Kbytes × $T_{C)}$ | 655 | — | µs |
| | • PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1) | 25 × $T_C$ | 125 | — | ns |
| | • PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0) | (128K x $T_C$) + $PLL_{LOCK}$ | 855 | — | µs |
| | • PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1) | (25 × $T_C$) + $PLL_{LOCK}$ | 200 | — | µs |
| 20 | • Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution[1] | 10 × $T_C$ + 3.8 | — | 53.8 | ns |
| 21 | Interrupt Requests Rate[1] | | | | |
| | • ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1, Timer, Timer_1 | 12 × $T_C$ | — | 60.0 | ns |
| | • DMA | 8 × $T_C$ | — | 40.0 | ns |
| | • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger) | 8 × $T_C$ | — | 40.0 | ns |
| | • $\overline{\text{IRQ}}$ (level trigger) | 12 × $T_C$ | — | 60.0 | ns |
| 22 | DMA Requests Rate | | | | |
| | • Data read from ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1 | 6 × $T_C$ | — | 30.0 | ns |
| | • Data write to ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1 | 7 × $T_C$ | — | 35.0 | ns |
| | • Timer, Timer_1 | 2 × $T_C$ | — | 10.0 | ns |
| | • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger) | 3 × $T_C$ | — | 15.0 | ns |

**Note:**

1. When using fast interrupts and when $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, if using an external clock (PCTL Bit 13 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.
   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shut down during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 200 us.
3. Periodically sampled and not 100% tested.
4. $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, $V_{DD}$ is valid, and the EXTAL input is active and valid. When $V_{DD}$ is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

Figure 12 shows the SPI master timing (CPHA = 0).

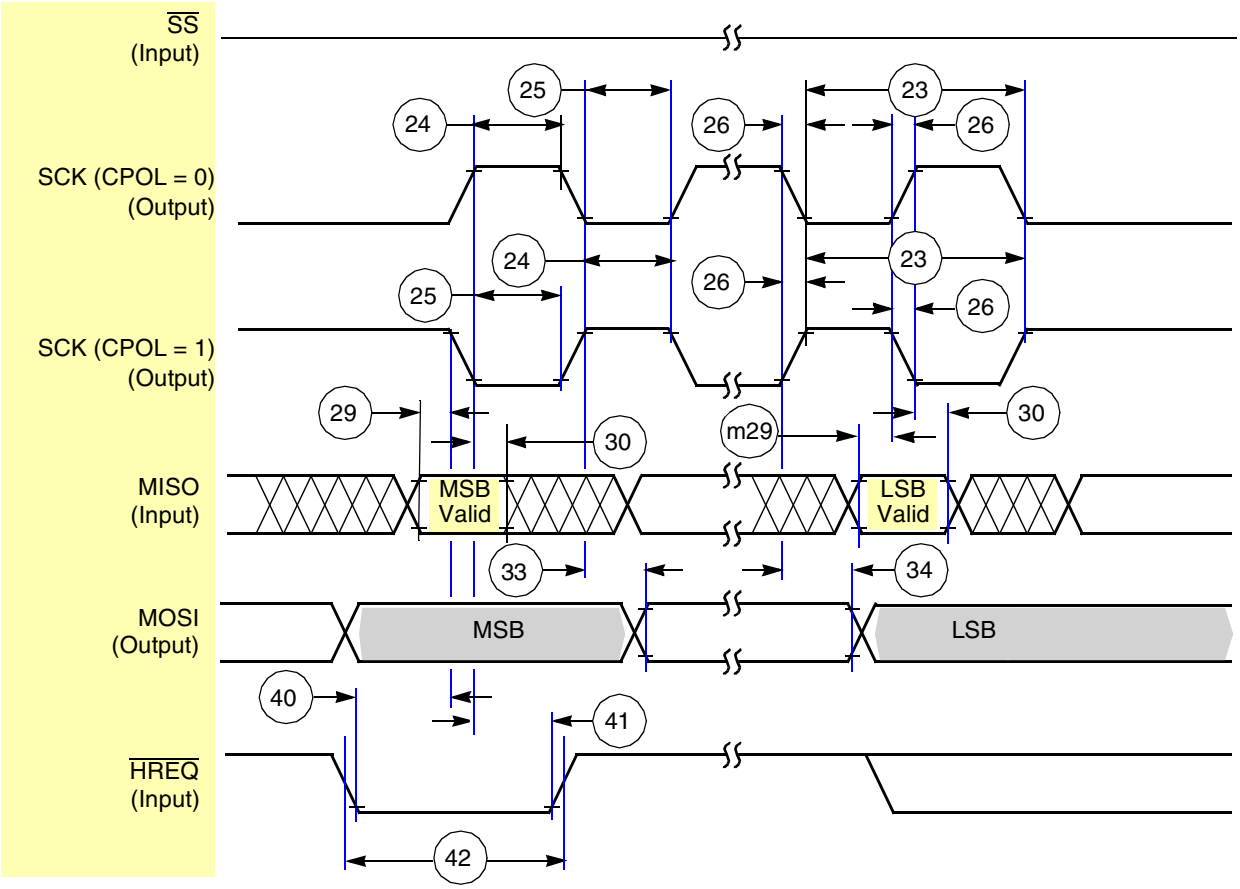


**Figure 12. SPI Master Timing (CPHA = 0)**