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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	112kB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56725caf

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1 Electrical Characteristics

1.1 Chip-Level Conditions

Table 1 provides a quick reference to the subsections in this section.

Table 1. Chip-Level Conditions

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Section 1.1.3, “Power Requirements”	on page 6
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1.1.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{DD}). The suggested value for a pull-up or pull-down resistor is 4.7 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 lists the maximum ratings.

Table 2. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	–0.3 to + 1.26	V
	V_{PLLP_VDD}, V_{IO_VDD}, $V_{IO\_VDD\_25}$, V_{PLLA_VDD}	–0.3 to + 4.0	V
Maximum CORE_VDD power supply ramp time	Tr	10	ms
Input Voltage per pin excluding VDD and GND	V_{IN}	GND – 0.3 to 5.5 V	V
Current drain per pin excluding V_{DD} and GND (Except for pads listed below)	I	12	mA
LSYNC_OUT	I_{lsync_out}	5	mA
LCLK	I_{lclk}	5	mA
LALE	I_{ale}	5	mA
TDO	I_{JTAG}	12	mA
Operating temperature range • Fsys < 200 MHz • Fsys < 250 MHz	T_J	 –40 to +100 0 to 90	°C
Storage temperature	T_{STG}	–65 to +150	°C
ESD protected voltage (Human Body Model)	—	2000	V
ESD protected voltage (Charged Device Model) • All pins • Corner pins	—	 500 750	V

Note:

1. GND = 0 V, T_J = –40° C to 100° C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

Table 5. Internal Clocks (Continued)

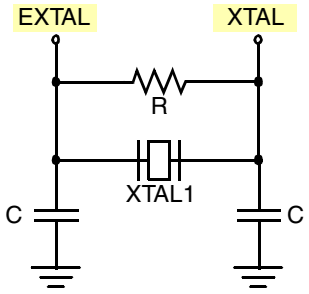
No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
3	PLL VCO Frequency	Fvco	200	—	500	MHz	Fvco = (Fin * NF)/NR
4	Output Clock Frequency [1] [2] • with PLL enabled • with PLL disabled	Fout	 25 —	—	 200 or 250 200 or 250	MHz	 Fout = Fvco/NO Fout = Fin
5	System Clock Frequency • with PLL enabled[2] • with PLL disabled	Fsys	 0.195 0	—	 200 or 250 200	MHz	 Fsys = Fout/2^{DF} Fsys = Fout

Note:

1. Fin = External frequency
   NF = Multiplication Factor
   NR = Predivision Factor
   NO = Output Divider
   DF = Division Factor
2. Maximum frequency of 200 MHz supported at 0.95 V < V_{VDD_CORE} < 1.05 V and –40 < Tj < 100° C
   Maximum frequency of 250 MHz supported at 1.14 V < V_{VDD_CORE} < 1.26 V and 0 < Tj < 90° C

1.1.8 External Clock Operation

The DSP56724/DSP56725 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; see Figure 6.



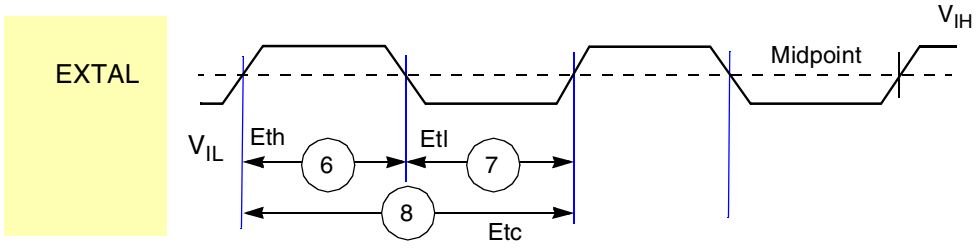
Suggested component values:

f_{osc} = 24.576 MHz
R = 1 M ±10%
C (EXTAL)= 18 pF
C (XTAL) = 18 pF

Calculations are for a 5–30 MHz crystal with the following parameters:
- shunt capacitance (C_0) of 10 pq–F12 pF
- series resistance 40 Ohm
- drive level of 10 µW

Figure 6. Using the On-Chip Oscillator

If the DSP56724/DSP56725 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 7). When the external square wave source is connected to EXTAL, the XTAL pin is not used.



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 7. External Clock Timing

Table 7. Reset, Stop, Mode Select, and Interrupt Timing (Continued)

No.	Characteristics	Expression	Min	Max	Unit
19	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[1, 2, 3]				
	• PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	(128 Kbytes × $T_{C)}$	655	—	µs
	• PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	25 × T_C	125	—	ns
	• PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	(128K x T_C) + PLL_{LOCK}	855	—	µs
	• PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	(25 × T_C) + PLL_{LOCK}	200	—	µs
20	• Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution[1]	10 × T_C + 3.8	—	53.8	ns
21	Interrupt Requests Rate[1]				
	• ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1, Timer, Timer_1	12 × T_C	—	60.0	ns
	• DMA	8 × T_C	—	40.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	8 × T_C	—	40.0	ns
	• $\overline{\text{IRQ}}$ (level trigger)	12 × T_C	—	60.0	ns
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	6 × T_C	—	30.0	ns
	• Data write to ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	7 × T_C	—	35.0	ns
	• Timer, Timer_1	2 × T_C	—	10.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	3 × T_C	—	15.0	ns

Note:

1. When using fast interrupts and when $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, if using an external clock (PCTL Bit 13 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.
   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shut down during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 200 us.
3. Periodically sampled and not 100% tested.
4. $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When V_{DD} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

Figure 8 shows the reset timing diagram.

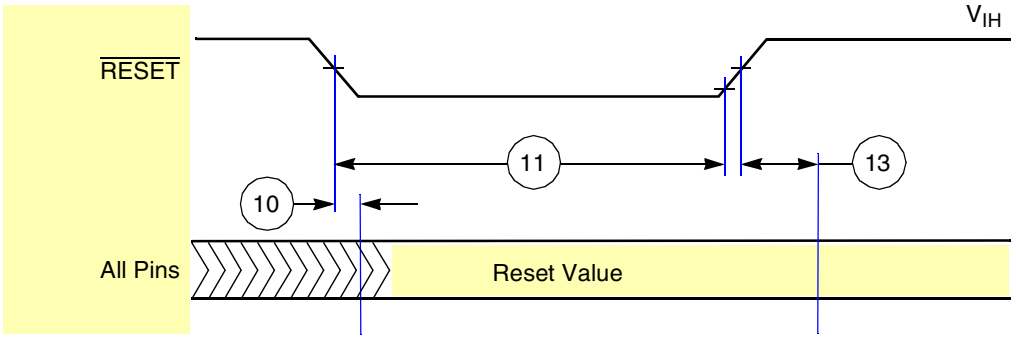


Figure 8. Reset Timing

Figure 9 shows external fast interrupt timing diagram.

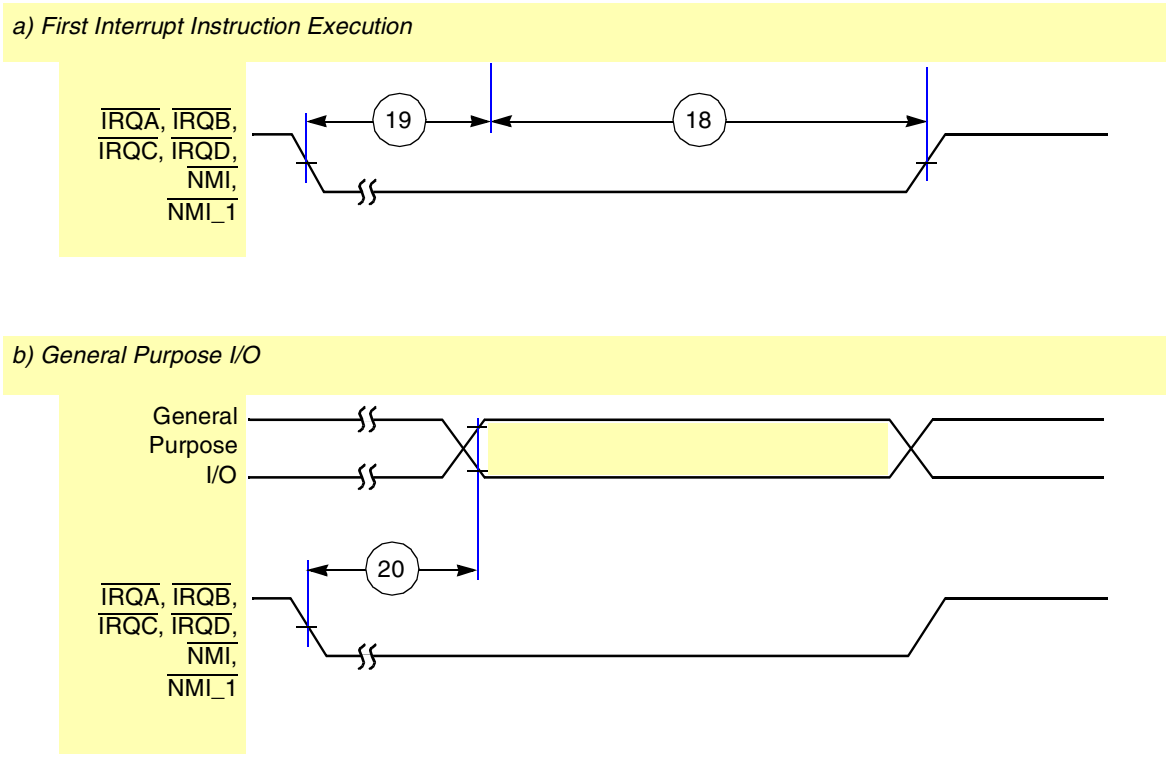


Figure 9. External Fast Interrupt Timing

Figure 10 shows external interrupt timing (negative edge-triggered).

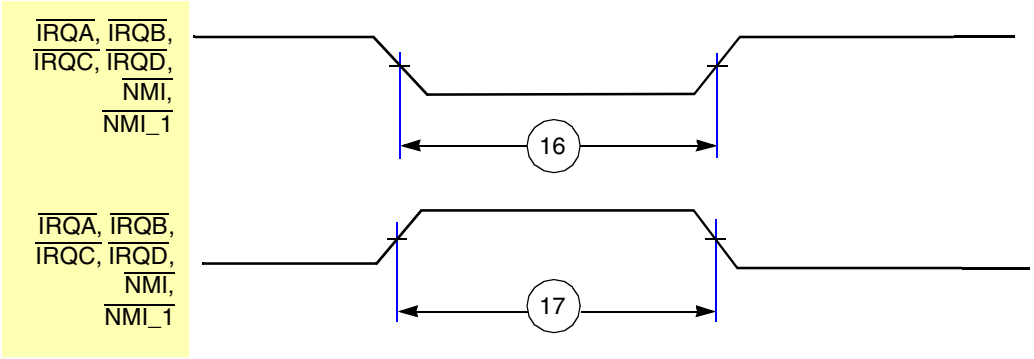


Figure 10. External Interrupt Timing (Negative Edge-Triggered)

Figure 11 shows MODE select set-up and hold time diagram.

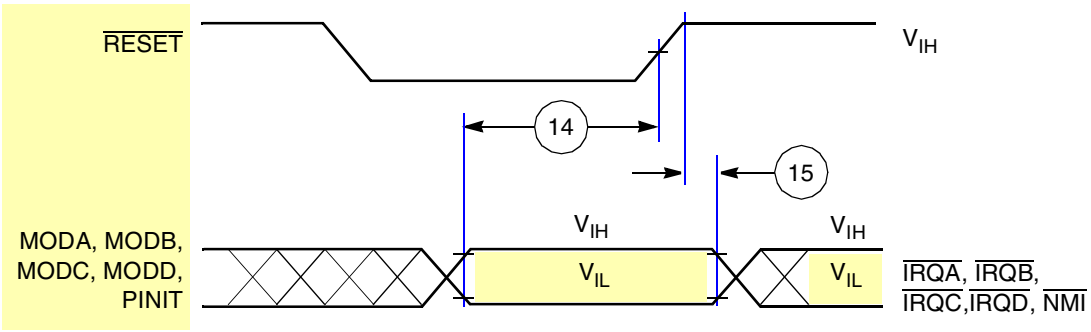


Figure 11. MODE Select Set-Up and Hold Time

1.2 Module-Level Specifications

Table 8 provides a quick reference to the subsections of this section.

Table 8. Module-Level Specifications

For	See
Section 1.2.1, “Serial Host Interface SPI Protocol Timing”	on page 4
Section 1.2.2, “Serial Host Interface (SHI) I2C Protocol Timing”	on page 6
Section 1.2.3, “Programming the SHI I2C Serial Clock”	on page 6
Section 1.2.4, “Enhanced Serial Audio Interface Timing”	on page 8
Section 1.2.5, “GPIO Timing”	on page 29
Section 1.2.6, “JTAG Timing”	on page 30
Section 1.2.7, “Watchdog Timer Timing”	on page 32
Section 1.2.8, “S/PDIF Timing”	on page 33
Section 1.2.9, “EMC Timing Specifications—DSP56724”	on page 34

Table 9. Serial Host Interface SPI Protocol Timing (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	$2.0 \times T_C + 2$	35	—	ns
			Very Narrow	$2.0 \times T_C + 1$	25	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
	CPHA = 1	Slave	Bypassed	—	10	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	—	12	—	ns
			Very Narrow	—	22	—	ns
			Narrow	—	100	—	ns
			Wide	—	200	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	—	0	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
30	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	$2 \times T_C + 10$	20	—	ns
			Very Narrow	$2 \times T_C + 30$	40	—	ns
			Narrow	$2 \times T_C + 60$	70	—	ns
			Wide	—	100.0	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	—	—	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	—	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	—	—	45	ns
			Very Narrow	—	—	110	ns
			Narrow	—	—	135	ns
			Wide	—	—	225	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	—	10	—	ns
			Very Narrow	—	15	—	ns
			Narrow	—	55	—	ns
			Wide	—	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	14.0	ns

Table 9. Serial Host Interface SPI Protocol Timing (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
36	First SCK sampling edge to $\overline{\text{HREQ}}$ output deassertion	Slave	Bypassed	—	45	—	ns
			Very Narrow	—	55	—	ns
			Narrow	—	95	—	ns
			Wide	—	145	—	ns
37	Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 1)	Slave	Bypassed	—	50.0	—	ns
			Very Narrow	—	60.0	—	ns
			Narrow	—	100.0	—	ns
			Wide	—	150.0	—	ns
38	$\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 0)	Slave	—	—	45.0	—	ns
39	$\overline{\text{SS}}$ deassertion pulse width (CPHA = 0)	Slave	—	$2 \times T_C$	0	—	ns
40	$\overline{\text{HREQ}}$ in deassertion to last SCK sampling edge ($\overline{\text{HREQ}}$ in set-up time) (CPHA = 1)	Master	—	—	0	—	ns
41	First SCK edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time)	Master	—	—	0	—	ns
42	$\overline{\text{HREQ}}$ assertion width	Master	—	$3.0 \times T_C$	15	—	ns

Note:

1. 0.95 V < V_{VDD_CORE} < 1.05 V and T_J < 100° C, C_L = 50 pF
2. Periodically sampled, not 100% tested
3. All times assume noise free inputs.
4. All times assume internal clock frequency of 200 MHz.
5. SHI_1 specs match those of SHI
6. Slave timings should equal the serial clock high period + the serial clock low period.

Figure 13 shows the SPI master timing (CPHA = 1).

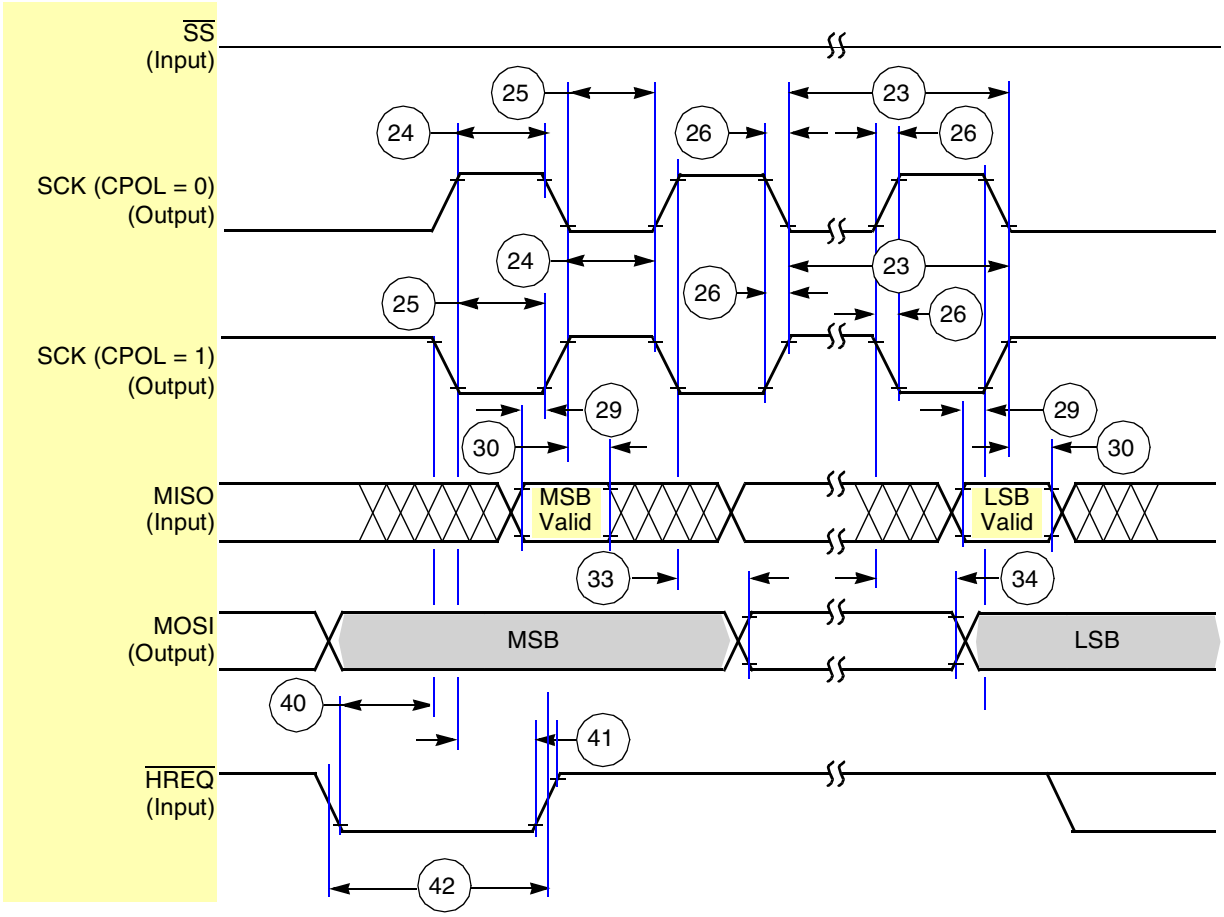


Figure 13. SPI Master Timing (CPHA = 1)

Figure 15 shows the SPI slave timing (CPHA = 1).

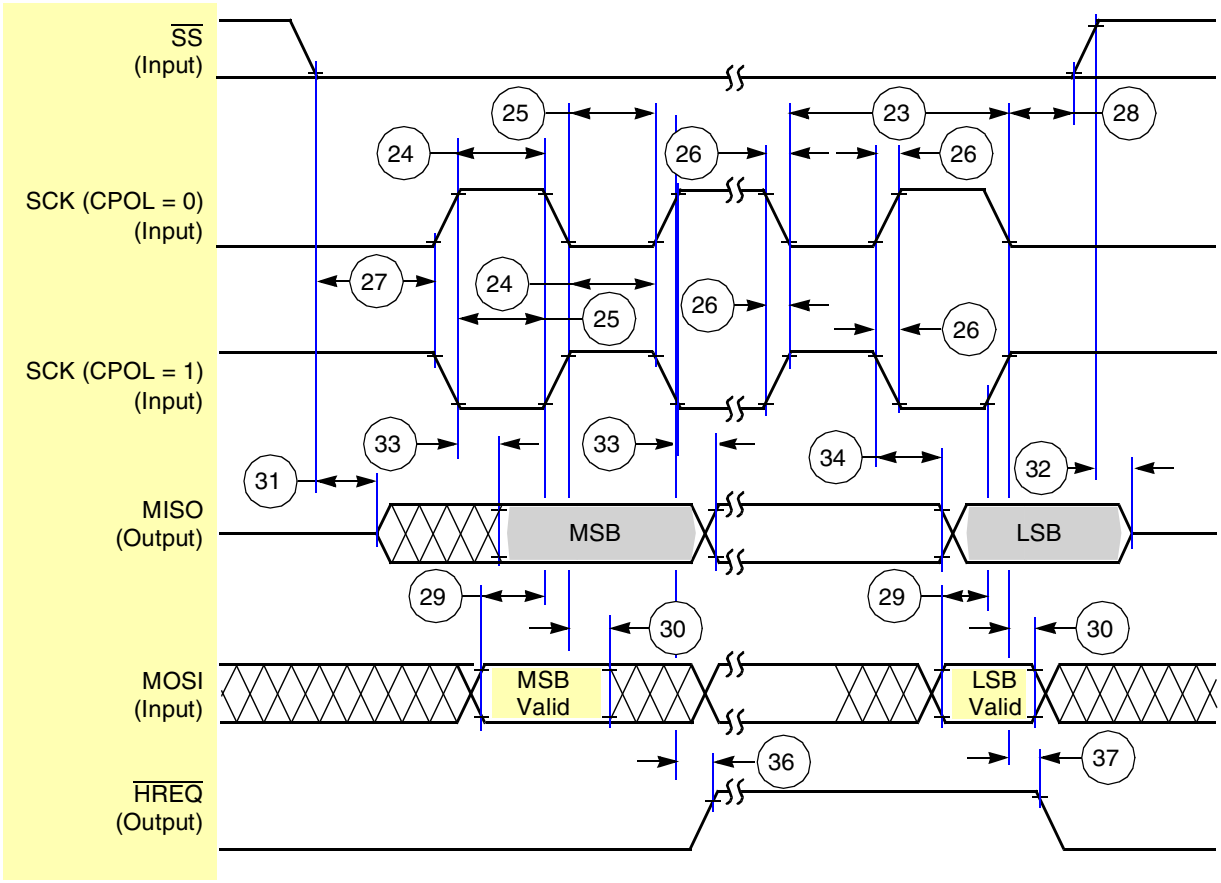


Figure 15. SPI Slave Timing (CPHA = 1)

1.2.2 Serial Host Interface (SHI) I²C Protocol Timing

Table 10 lists the SHI I²C protocol timing diagram.

Table 10. SHI I²C Protocol Timing

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
XX	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	—	 — — — —	 0 10 50 100	 — — — —	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs

Figure 16 shows the I²C timing diagram.

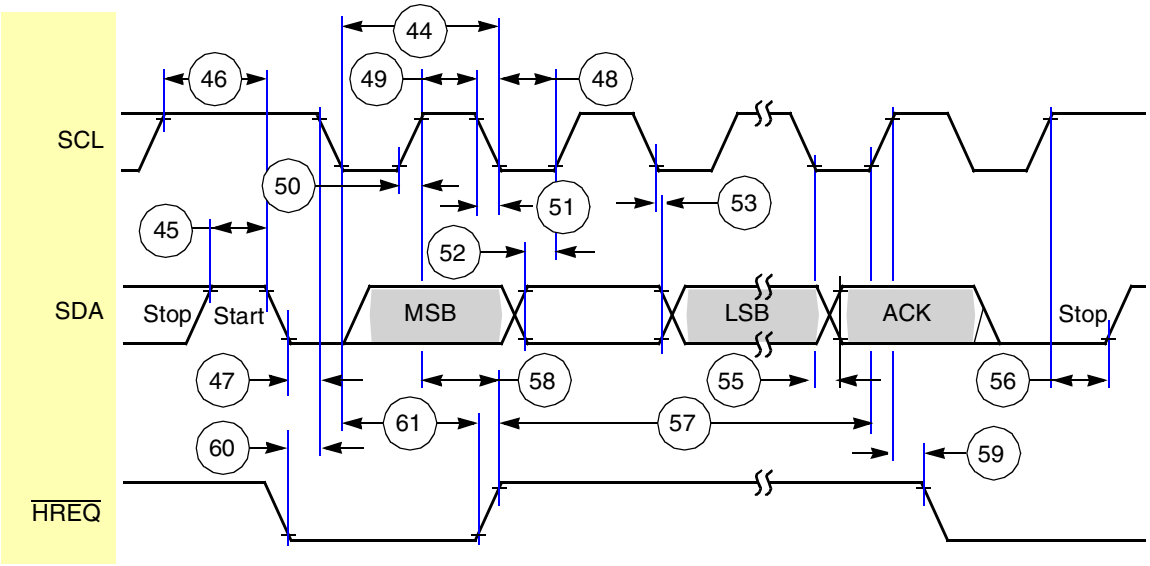


Figure 16. I²C Timing

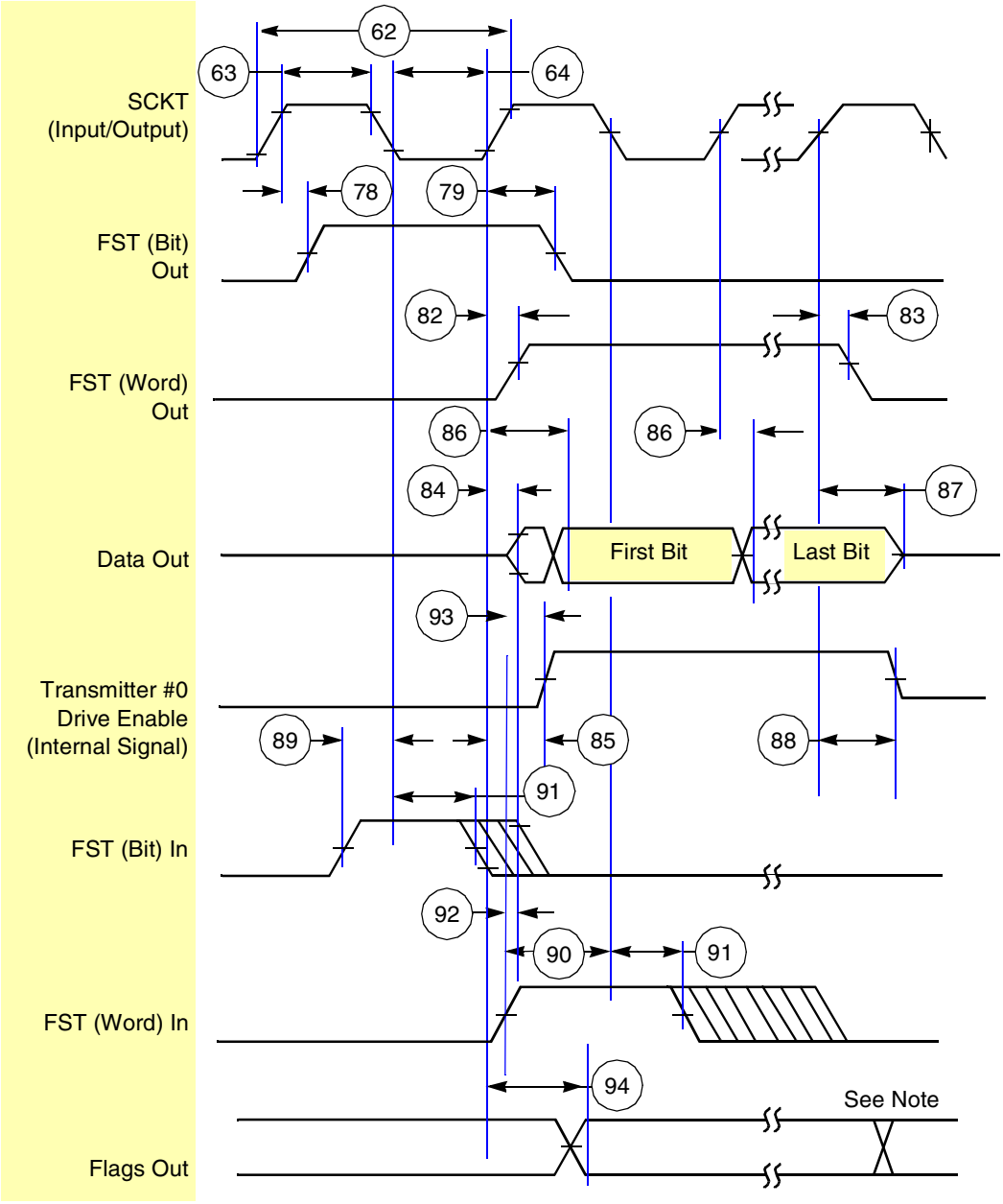
1.2.4 Enhanced Serial Audio Interface Timing

Table 11 lists the enhanced serial audio interface timing.

Table 11. Enhanced Serial Audio Interface Timing

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	20.0 20.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	— —	$2 \times T_C$ $2 \times T_C$	10 10	— —	— —	ns
64	Clock low period • For internal clock • For external clock	— —	$2 \times T_C$ $2 \times T_C$	10 10	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	—	—	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[6]	—	—	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[6]	—	—	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	—	—	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	—	—	— —	17.0 7.0	x ck i ck a	ns

Figure 17 shows the ESAI transmitter timing diagram.



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 17. ESAI Transmitter Timing

Figure 18 shows the ESAI receiver timing diagram.

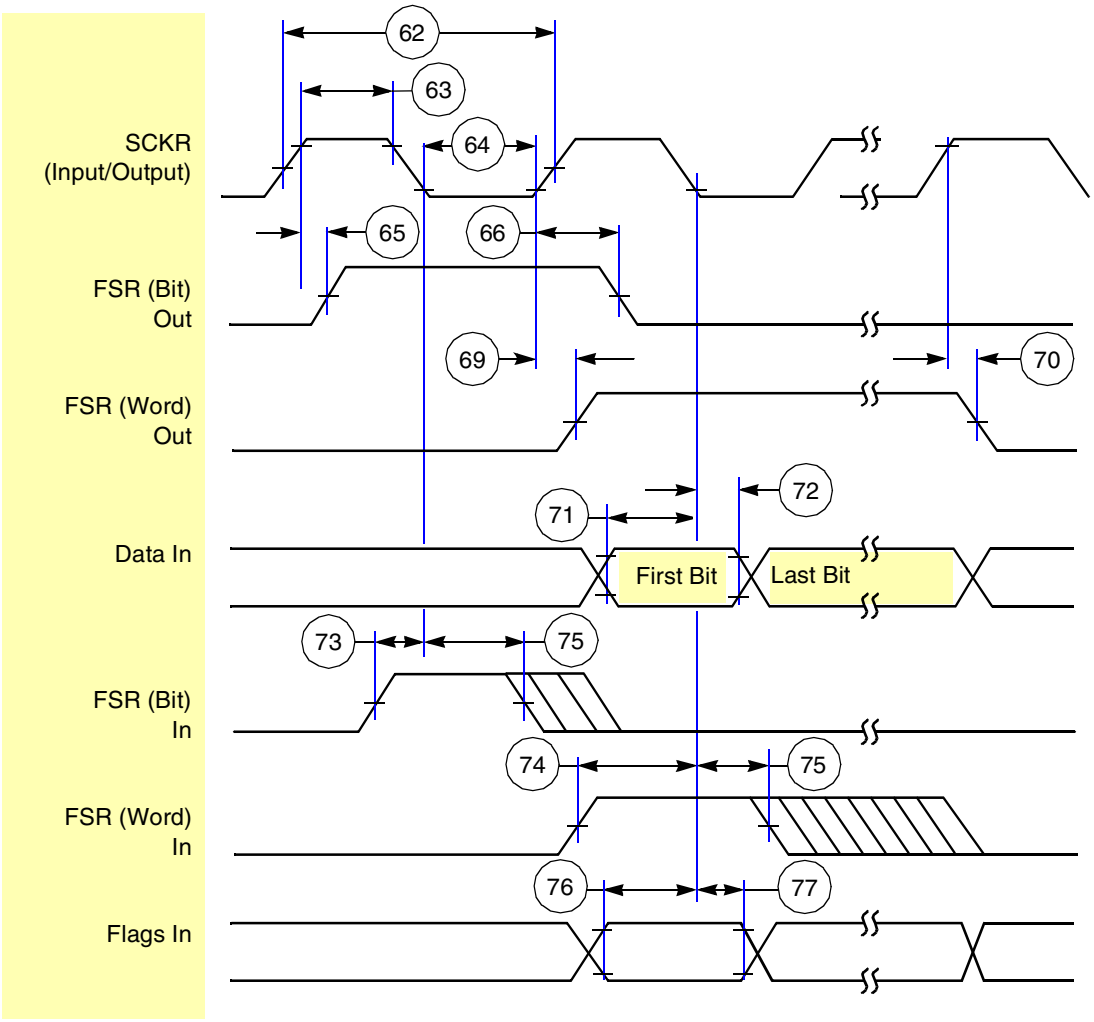


Figure 18. ESAI Receiver Timing

Figure 19 shows the ESAI HCKT timing diagram.

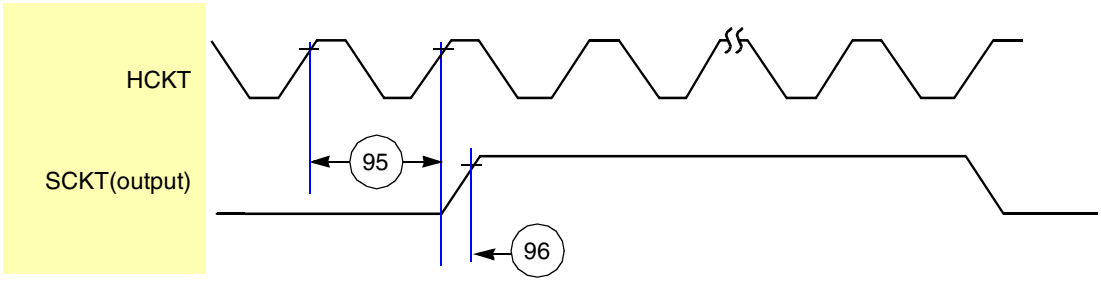


Figure 19. ESAI HCKT Timing

Figure 20 shows the ESAI HCKR timing diagram.

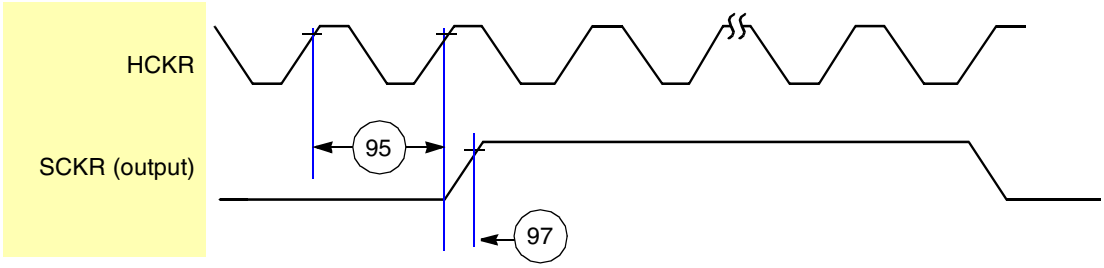


Figure 20. ESAI HCKR Timing

1.2.5 GPIO Timing

Table 12 lists the GPIO timing.

Table 12. GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
100	Fsys edge to GPIO out valid (GPIO out delay time)[2]	—	—	7	ns
101	Fsys edge to GPIO out not valid (GPIO out hold time)[2]	—	—	7	ns
102	Fsys In valid to EXTAL edge (GPIO in set-up time)[2]	—	2	—	ns
103	Fsys edge to GPIO in not valid (GPIO in hold time)[2]	—	0	—	ns
104	Minimum GPIO pulse high width	2 × TC	10	—	ns
105	Minimum GPIO pulse low width	2 × TC	10	—	ns
106	GPIO out rise time	—	—	13.0	ns
107	GPIO out fall time	—	—	13.0	ns

Note:
1. 0.95 V < V_{VDD_CORE} < 1.05 V and Tj < 100° C, C_L = 50 pF
2. Simulation numbers-subject to change.

Figure 22 shows the text clock input timing diagram.

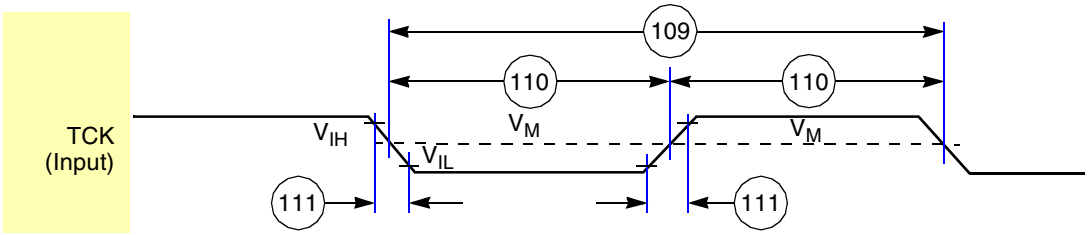


Figure 22. Test Clock Input Timing Diagram

Figure 23 shows the debugger port timing diagram.

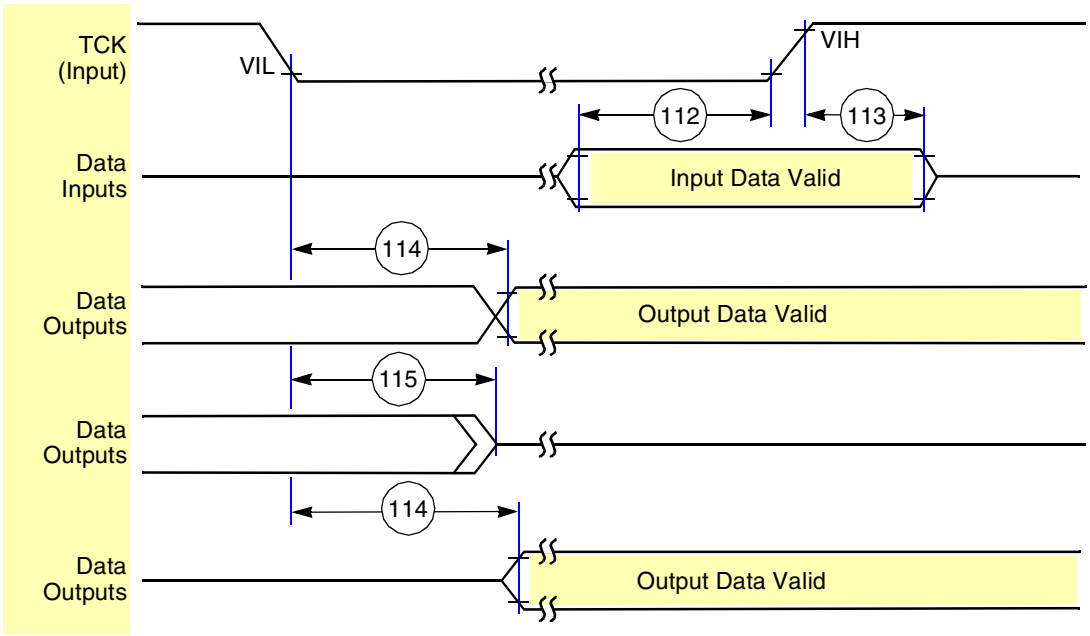


Figure 23. Debugger Port Timing Diagram

Figure 28 shows the EMC signals diagram, with EMC PLL bypassed.

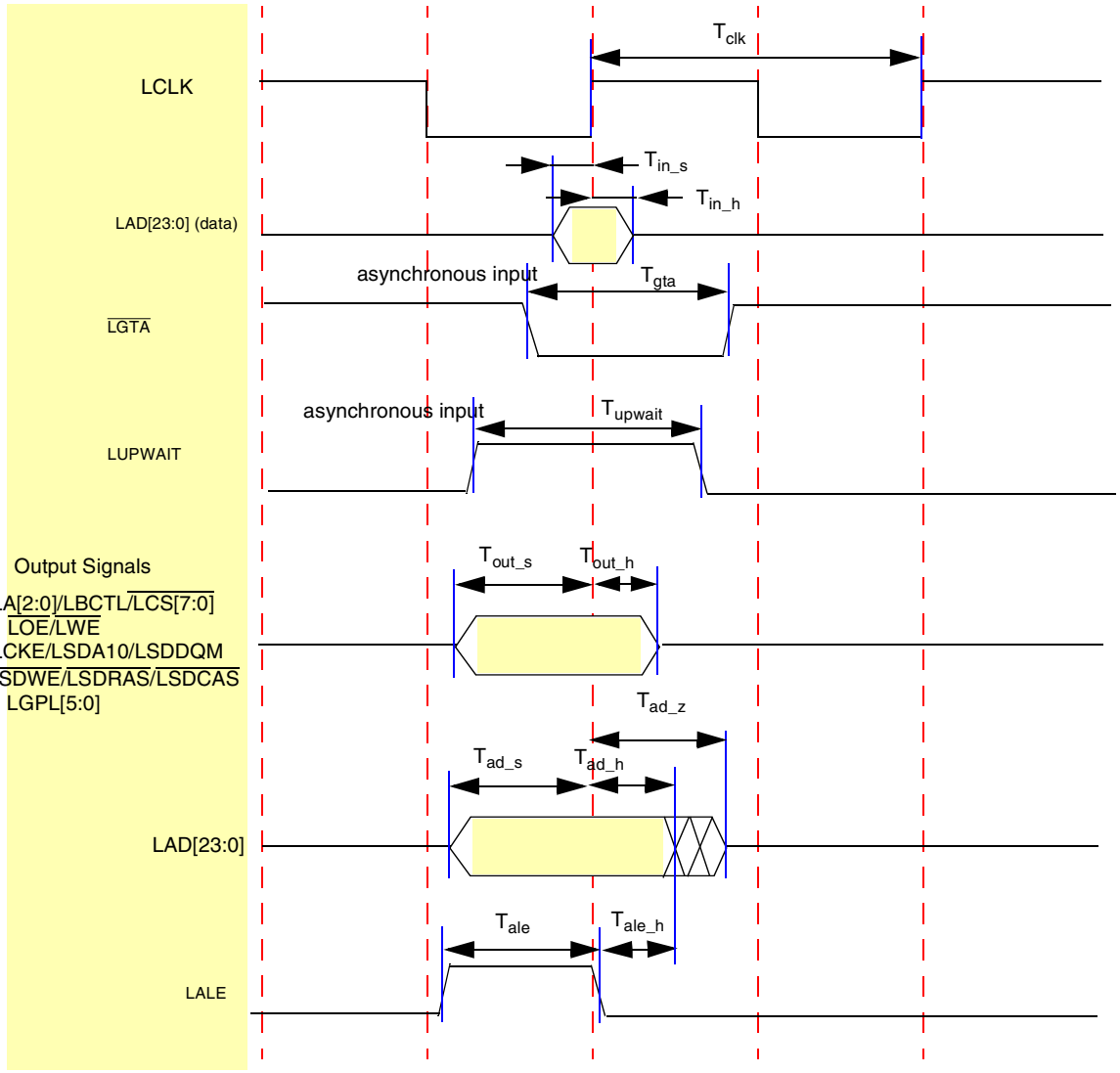


Figure 28. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 4

Table 18 lists the EMC timing parameters with EMC PLL bypassed.

Table 18. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	$8 \times T_C$	—	ns
Input setup to LCLK (except $\overline{\text{LGTA}}$/LUPWAIT)	T_{in_s}	8	—	ns
Input hold from LCLK (except $\overline{\text{LGTA}}$/LUPWAIT)[1]	T_{in_h}	–1	—	ns
$\overline{\text{LGTA}}$ valid time	T_{gta}	42	—	ns
LUPWAIT valid time	T_{upwait}	42	—	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	5	—	ns
LALE valid time	T_{ale}	34	—	ns

Table 18. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

Parameter	Symbol	Min	Max	Unit
Output setup from LCLK (except LAD[23:0] and LALE)	T_{out_s}	19	—	ns
Output hold from LCLK (except LAD[23:0] and LALE)	T_{out_h}	18	—	ns
LAD[23:0] output setup from LCLK	T_{ad_s}	18	—	ns
LAD[23:0] output hold from LCLK	T_{ad_h}	17	—	ns
LCLK to output high impedance for LAD[23:0]	T_{ad_z}	—	17.1	ns

Note:

1. Negative hold time means the signal could be invalid before LCLK raising edge.

Figure 29 shows the EMC signals diagram, with EMC PLL bypassed.

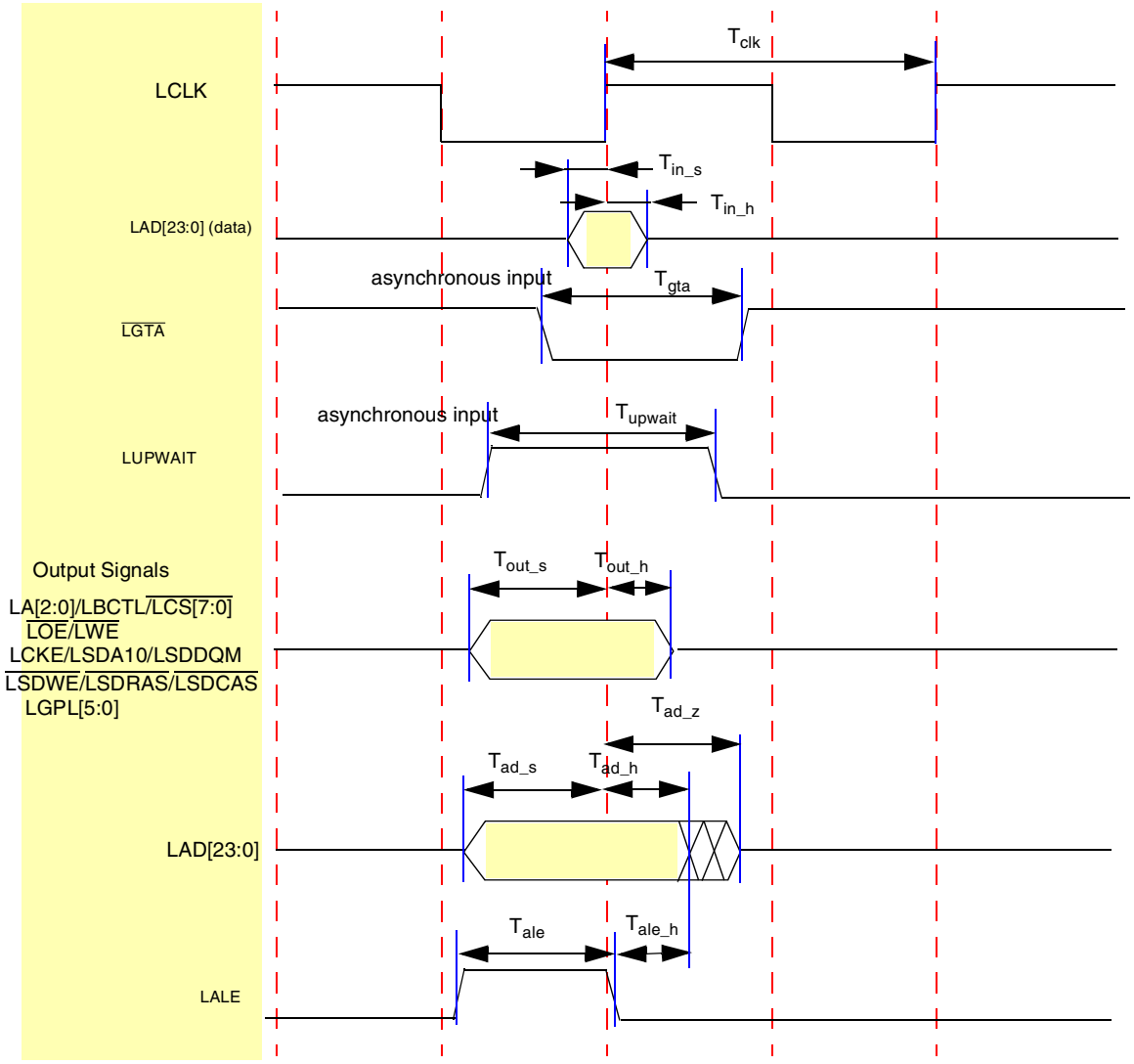


Figure 29. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

2 Functional Description and Application Information

Refer to the *Symphony™ DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual* (DSP56724RM) for detailed functional and applications information.

3 Ordering Information

Table 19 shows the ordering information for the DSP56724/DSP56725 devices.

Table 19. Ordering Information

Device	Device Marking	Ambient Temp.	Speed	Voltage	LQFP Package
DSP56724	DSPB56724AG	0° C–70° C	250 MHz	1.14–1.26 V	20 mm × 20 mm
DSP56724	DSPB56724CAG	–40° C–85° C	200 MHz	0.95–1.05 V	20 mm × 20 mm
DSP56725	DSPB56725AF	0° C–70° C	250 MHz	1.14–1.26 V	14 mm × 14 mm
DSP56725	DSPB56725CAF	–40° C–85° C	200 MHz	0.95–1.05 V	14 mm × 14 mm

Contact your local Freescale sales representative for ordering information.

4 Package Information

This section provides package and pinout information.

Table 20 is a quick reference to the package outline drawings.

Table 20. Package Outline Drawings

Device	Package	See
DSP56724	144-pin plastic LQFP	See Section 4.2, “144-Pin Package Outline Drawing,” on page 42.
DSP56725	80-pin plastic LQFP	See Section 4.3, “80-Pin Package Outline Drawing,” on page 44.

4.1.2 Pinout for DSP56725 80-Pin Plastic LQFP Package

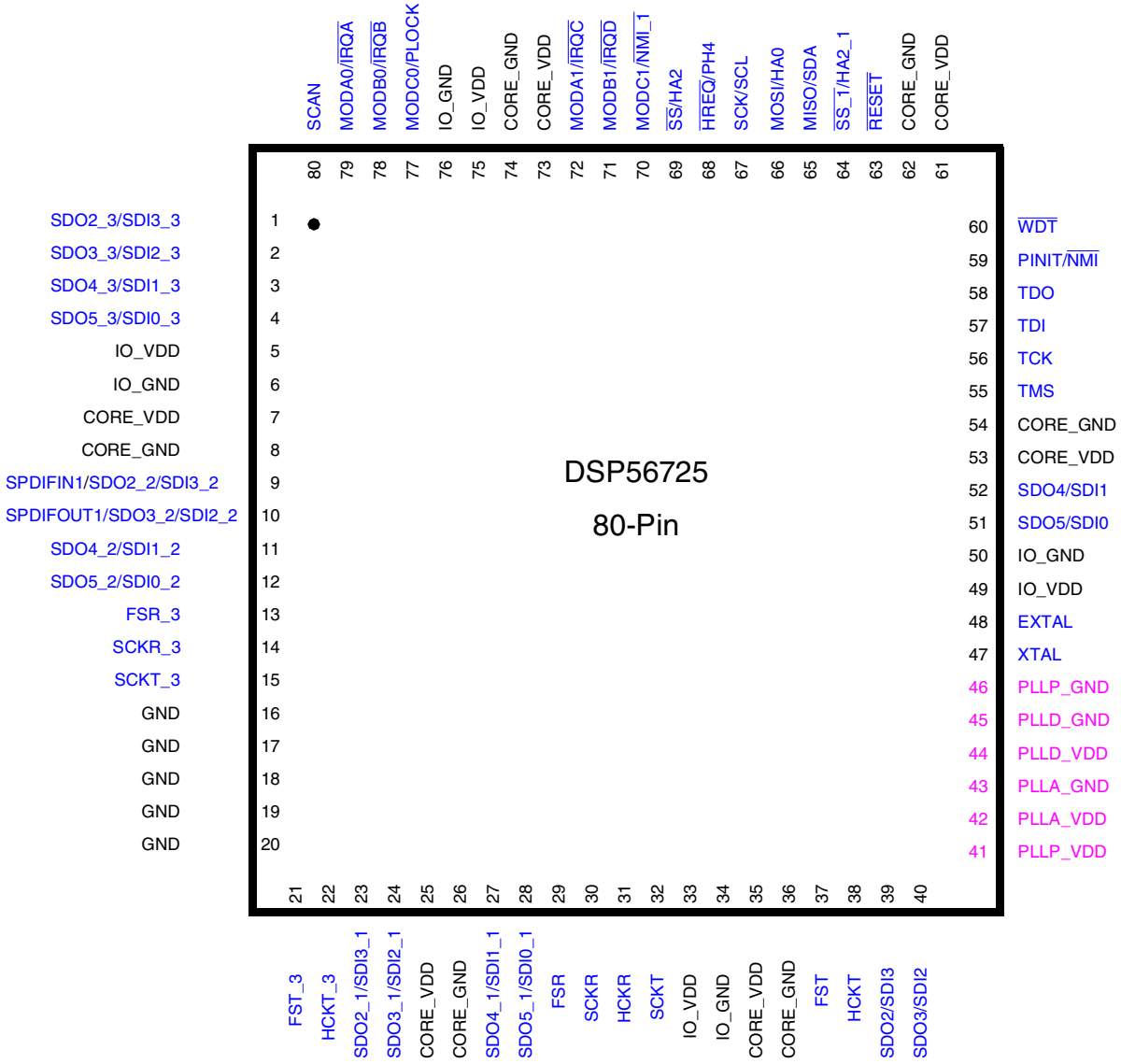


Figure 31. DSP56725 80-Pin Package

4.1.3 Pin Multiplexing

Many pins are multiplexed, and depending on the selected configuration, can be one of three possible signals. For more about pin multiplexing, refer to the *Symphony™ DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual* (DSP56724RM).