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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe167h-72f66l-ac

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Summary of Features

The XE167 types are offered with several Flash memory sizes. [Table 2](#) describes the location of the available memory areas for each Flash memory size.

Table 2 Flash Memory Allocation

Total Flash Size	Flash Area A ¹⁾	Flash Area B	Flash Area C
768 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... CB'FFFF _H	n.a.
576 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C8'FFFF _H	n.a.
384 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C5'FFFF _H	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XE167 types are offered with different interface options. [Table 3](#) lists the available channels for each option.

Table 3 Interface Channel Association

Total Number	Available Channels
16 ADC0 channels	CH0 ... CH15
8 ADC0 channels	CH0 ... CH7
8 ADC1 channels	CH0 ... CH7
5 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4
2 CAN nodes	CAN0, CAN1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1
4 serial channels	U0C0, U0C1, U1C0, U1C1

2.1 Pin Configuration and Definition

The pins of the XE167 are described in detail in [Table 4](#), which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. [Figure 2](#) summarizes all pins, showing their locations on the four sides of the package.

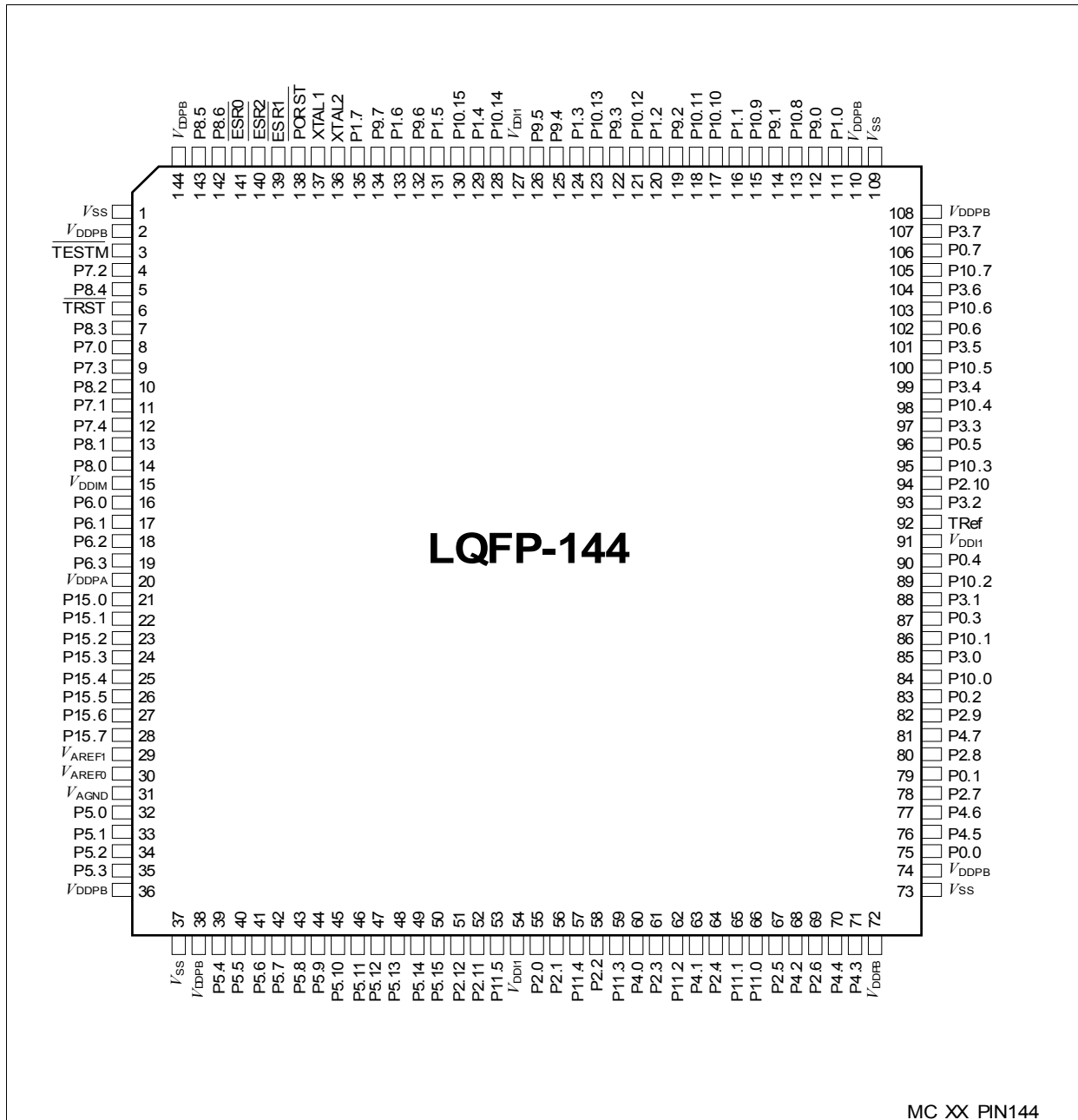


Figure 2 Pin Configuration (top view)

Notes to Pin Definitions

1. **Ctrl.:** The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bitfield PC to 1x00_B, output O1 is selected by 1x01_B, etc.
Output signal OH is controlled by hardware.
2. **Type:** Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	CCU62_ CCPOS0A	I	St/B	CCU62 Position Input 0
	TDI_C	I	St/B	JTAG Test Data Input
5	P8.4	O0 / I	St/B	Bit 4 of Port 8, General Purpose Input/Output
	CCU60_ COUT61	O1	St/B	CCU60 Channel 1 Output
	TMS_D	I	St/B	JTAG Test Mode Selection Input
6	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE167's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	Bit 3 of Port 8, General Purpose Input/Output
	CCU60_ COUT60	O1	St/B	CCU60 Channel 0 Output
	TDI_D	I	St/B	JTAG Test Data Input

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
18	P6.2	O0 / I	St/A	Bit 2 of Port 6, General Purpose Input/Output
	EMUX2	O1	St/A	External Analog MUX Control Output 2 (ADC0)
	T6OUT	O2	St/A	GPT2 Timer T6 Toggle Latch Output
	U1C1_SCLKOUT	O3	St/A	USIC1 Channel 1 Shift Clock Output
	U1C1_DX1C	I	St/A	USIC1 Channel 1 Shift Clock Input
19	P6.3	O0 / I	St/A	Bit 3 of Port 6, General Purpose Input/Output
	T3OUT	O2	St/A	GPT1 Timer T3 Toggle Latch Output
	U1C1_SELO0	O3	St/A	USIC1 Channel 1 Select/Control 0 Output
	U1C1_DX2D	I	St/A	USIC1 Channel 1 Shift Control Input
	ADCx_REQTRYD	I	St/A	External Request Trigger Input for ADC0/1
21	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
22	P15.1	I	In/A	Bit 1 of Port 15, General Purpose Input
	ADC1_CH1	I	In/A	Analog Input Channel 1 for ADC1
23	P15.2	I	In/A	Bit 2 of Port 15, General Purpose Input
	ADC1_CH2	I	In/A	Analog Input Channel 2 for ADC1
	T5IN	I	In/A	GPT2 Timer T5 Count/Gate Input
24	P15.3	I	In/A	Bit 3 of Port 15, General Purpose Input
	ADC1_CH3	I	In/A	Analog Input Channel 3 for ADC1
	T5EUD	I	In/A	GPT2 Timer T5 External Up/Down Control Input
25	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6IN	I	In/A	GPT2 Timer T6 Count/Gate Input
26	P15.5	I	In/A	Bit 5 of Port 15, General Purpose Input
	ADC1_CH5	I	In/A	Analog Input Channel 5 for ADC1
	T6EUD	I	In/A	GPT2 Timer T6 External Up/Down Control Input
27	P15.6	I	In/A	Bit 6 of Port 15, General Purpose Input
	ADC1_CH6	I	In/A	Analog Input Channel 6 for ADC1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
28	P15.7	I	In/A	Bit 7 of Port 15, General Purpose Input
	ADC1_CH7	I	In/A	Analog Input Channel 7 for ADC1
29	V_{AREF1}	-	PS/A	Reference Voltage for A/D Converter ADC1
30	V_{AREF0}	-	PS/A	Reference Voltage for A/D Converter ADC0
31	V_{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
32	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
33	P5.1	I	In/A	Bit 1 of Port 5, General Purpose Input
	ADC0_CH1	I	In/A	Analog Input Channel 1 for ADC0
34	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input
35	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3IN	I	In/A	GPT1 Timer T3 Count/Gate Input
39	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	CCU63_T12HRB	I	In/A	External Run Control Input for T12 of CCU63
	T3EUD	I	In/A	GPT1 Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
40	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12HRB	I	In/A	External Run Control Input for T12 of CCU60
41	P5.6	I	In/A	Bit 6 of Port 5, General Purpose Input
	ADC0_CH6	I	In/A	Analog Input Channel 6 for ADC0
42	P5.7	I	In/A	Bit 7 of Port 5, General Purpose Input
	ADC0_CH7	I	In/A	Analog Input Channel 7 for ADC0

Functional Description

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see [Table 5](#)) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Up to 768 Kbytes of on-chip Flash memory store code, constant data, and control data. The on-chip Flash memory consists of up to three modules with a maximum capacity of 256 Kbytes each. Each module is organized in 4-Kbyte sectors.

The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen derivative (see [Table 1](#)).

Each sector can be separately write protected¹⁾, erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.

For Flash parameters, please see [Section 4.5](#).

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.4 Interrupt System

With a minimum interrupt response time of $7/11^{1)}$ CPU clocks (in the case of internal program execution), the XE167 can react quickly to the occurrence of non-deterministic events.

The architecture of the XE167 supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE167 has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

Each of the possible interrupt nodes has a separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield. Each node can be programmed by its related register to one of sixteen interrupt priority levels. Once accepted by the CPU, an interrupt service can only be interrupted by a higher-priority service request. For standard interrupt processing, each possible interrupt node has a dedicated vector location.

Fast external interrupt inputs can service external interrupts with high-precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 6 shows all of the possible XE167 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes) may be used to generate software-controlled interrupt requests by setting the respective interrupt request bit (xIR).

1) Depending if the jump cache is used or not.

Functional Description

Table 6 XE167 Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location¹⁾	Trap Number
CAPCOM Register 16, or ERU Request 0	CC2_CC16IC	xx'0040 _H	10 _H / 16 _D
CAPCOM Register 17, or ERU Request 1	CC2_CC17IC	xx'0044 _H	11 _H / 17 _D
CAPCOM Register 18, or ERU Request 2	CC2_CC18IC	xx'0048 _H	12 _H / 18 _D
CAPCOM Register 19, or ERU Request 3	CC2_CC19IC	xx'004C _H	13 _H / 19 _D
CAPCOM Register 20, or USIC0 Request 6	CC2_CC20IC	xx'0050 _H	14 _H / 20 _D
CAPCOM Register 21, or USIC0 Request 7	CC2_CC21IC	xx'0054 _H	15 _H / 21 _D
CAPCOM Register 22, or USIC1 Request 6	CC2_CC22IC	xx'0058 _H	16 _H / 22 _D
CAPCOM Register 23, or USIC1 Request 7	CC2_CC23IC	xx'005C _H	17 _H / 23 _D
CAPCOM Register 24, or ERU Request 0	CC2_CC24IC	xx'0060 _H	18 _H / 24 _D
CAPCOM Register 25, or ERU Request 1	CC2_CC25IC	xx'0064 _H	19 _H / 25 _D
CAPCOM Register 26, or ERU Request 2	CC2_CC26IC	xx'0068 _H	1A _H / 26 _D
CAPCOM Register 27, or ERU Request 3	CC2_CC27IC	xx'006C _H	1B _H / 27 _D
CAPCOM Register 28, or USIC2 Request 6	CC2_CC28IC	xx'0070 _H	1C _H / 28 _D
CAPCOM Register 29, or USIC2 Request 7	CC2_CC29IC	xx'0074 _H	1D _H / 29 _D
CAPCOM Register 30	CC2_CC30IC	xx'0078 _H	1E _H / 30 _D
CAPCOM Register 31	CC2_CC31IC	xx'007C _H	1F _H / 31 _D
GPT1 Timer 2	GPT12E_T2IC	xx'0080 _H	20 _H / 32 _D
GPT1 Timer 3	GPT12E_T3IC	xx'0084 _H	21 _H / 33 _D
GPT1 Timer 4	GPT12E_T4IC	xx'0088 _H	22 _H / 34 _D

Functional Description

Table 6 XE167 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location¹⁾	Trap Number
CAN Request 1	CAN_1IC	xx'0104 _H	41 _H / 65 _D
CAN Request 2	CAN_2IC	xx'0108 _H	42 _H / 66 _D
CAN Request 3	CAN_3IC	xx'010C _H	43 _H / 67 _D
CAN Request 4	CAN_4IC	xx'0110 _H	44 _H / 68 _D
CAN Request 5	CAN_5IC	xx'0114 _H	45 _H / 69 _D
CAN Request 6	CAN_6IC	xx'0118 _H	46 _H / 70 _D
CAN Request 7	CAN_7IC	xx'011C _H	47 _H / 71 _D
CAN Request 8	CAN_8IC	xx'0120 _H	48 _H / 72 _D
CAN Request 9	CAN_9IC	xx'0124 _H	49 _H / 73 _D
CAN Request 10	CAN_10IC	xx'0128 _H	4A _H / 74 _D
CAN Request 11	CAN_11IC	xx'012C _H	4B _H / 75 _D
CAN Request 12	CAN_12IC	xx'0130 _H	4C _H / 76 _D
CAN Request 13	CAN_13IC	xx'0134 _H	4D _H / 77 _D
CAN Request 14	CAN_14IC	xx'0138 _H	4E _H / 78 _D
CAN Request 15	CAN_15IC	xx'013C _H	4F _H / 79 _D
USIC0 Cannel 0, Request 0	U0C0_0IC	xx'0140 _H	50 _H / 80 _D
USIC0 Cannel 0, Request 1	U0C0_1IC	xx'0144 _H	51 _H / 81 _D
USIC0 Cannel 0, Request 2	U0C0_2IC	xx'0148 _H	52 _H / 82 _D
USIC0 Cannel 1, Request 0	U0C1_0IC	xx'014C _H	53 _H / 83 _D
USIC0 Cannel 1, Request 1	U0C1_1IC	xx'0150 _H	54 _H / 84 _D
USIC0 Cannel 1, Request 2	U0C1_2IC	xx'0154 _H	55 _H / 85 _D
USIC1 Cannel 0, Request 0	U1C0_0IC	xx'0158 _H	56 _H / 86 _D
USIC1 Cannel 0, Request 1	U1C0_1IC	xx'015C _H	57 _H / 87 _D
USIC1 Cannel 0, Request 2	U1C0_2IC	xx'0160 _H	58 _H / 88 _D
USIC1 Cannel 1, Request 0	U1C1_0IC	xx'0164 _H	59 _H / 89 _D
USIC1 Cannel 1, Request 1	U1C1_1IC	xx'0168 _H	5A _H / 90 _D
USIC1 Cannel 1, Request 2	U1C1_2IC	xx'016C _H	5B _H / 91 _D
USIC2 Cannel 0, Request 0	U2C0_0IC	xx'0170 _H	5C _H / 92 _D
USIC2 Cannel 0, Request 1	U2C0_1IC	xx'0174 _H	5D _H / 93 _D
USIC2 Cannel 0, Request 2	U2C0_2IC	xx'0178 _H	5E _H / 94 _D

Functional Description

The XE167 includes an excellent mechanism to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 7 shows all possible exceptions or error conditions that can arise during runtime:

Table 7 Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location ¹⁾	Trap Number	Trap Priority
Reset Functions	—	RESET	xx'0000 _H	00 _H	III
Class A Hardware Traps:					
• System Request 0	SR0	SR0TRAP	xx'0008 _H	02 _H	II
• Stack Overflow	STKOF	STOTRAP	xx'0010 _H	04 _H	II
• Stack Underflow	STKUF	STUTRAP	xx'0018 _H	06 _H	II
• Software Break	SOFTBRK	SBRKTRAP	xx'0020 _H	08 _H	II
Class B Hardware Traps:					
• System Request 1	SR1	BTRAP	xx'0028 _H	0A _H	I
• Undefined Opcode	UNDOPC	BTRAP	xx'0028 _H	0A _H	I
• Memory Access Error	ACER	BTRAP	xx'0028 _H	0A _H	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx'0028 _H	0A _H	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx'0028 _H	0A _H	I
Reserved	—	—	[2C _H - 3C _H]	[0B _H - 0F _H]	—
Software Traps:	—	—	Any	Any	Current
• TRAP Instruction			[xx'0000 _H - xx'01FC _H] in steps of 4 _H	[00 _H - 7F _H]	CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
 - maximum baud rate: $f_{\text{SYS}} / 4$
 - data frame length programmable from 1 to 63 bits
 - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
 - maximum baud rate: $f_{\text{SYS}} / 16$
 - checksum generation under software control
 - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
 - maximum baud rate in slave mode: f_{SYS}
 - maximum baud rate in master mode: $f_{\text{SYS}} / 2$, limited by loop delay
 - number of data bits programmable from 1 to 63, more with explicit stop condition
 - MSB or LSB first
 - optional control of slave select signals
- **IIC** (Inter-IC Bus)
 - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
 - maximum baud rate: $f_{\text{SYS}} / 2$ for transmitter, f_{SYS} for receiver

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XE167 into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 20 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply watchdog (SWD) supervision level (see Table 21)	V_{SWD} CC	$V_{\text{LV}} - 0.150$	V_{LV}	$V_{\text{LV}} + 0.100$	V	V_{LV} = selected voltage in upper voltage area
		$V_{\text{LV}} - 0.125$	V_{LV}	$V_{\text{LV}} + 0.050$	V	V_{LV} = selected voltage in lower voltage area
Core voltage (PVC) supervision level (see Table 22)	V_{PVC} CC	$V_{\text{LV}} - 0.070$	V_{LV}	$V_{\text{LV}} + 0.030$	V	V_{LV} = selected voltage
Current control limit	I_{CC} CC	13	–	30	mA	Power domain DMP_M
		90	–	150	mA	Power domain DMP_1
Wakeup clock source frequency	f_{WU} CC	400	500	600	kHz	FREQSEL = 00 _B
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Startup time from stopover mode	t_{SSO} CC	200	260	320	μs	User instruction from PSRAM

4.6.2 Definition of Internal Timing

The internal operation of the XE167 is controlled by the internal system clock f_{SYS} .

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS} . This must be considered when calculating the timing for the XE167.

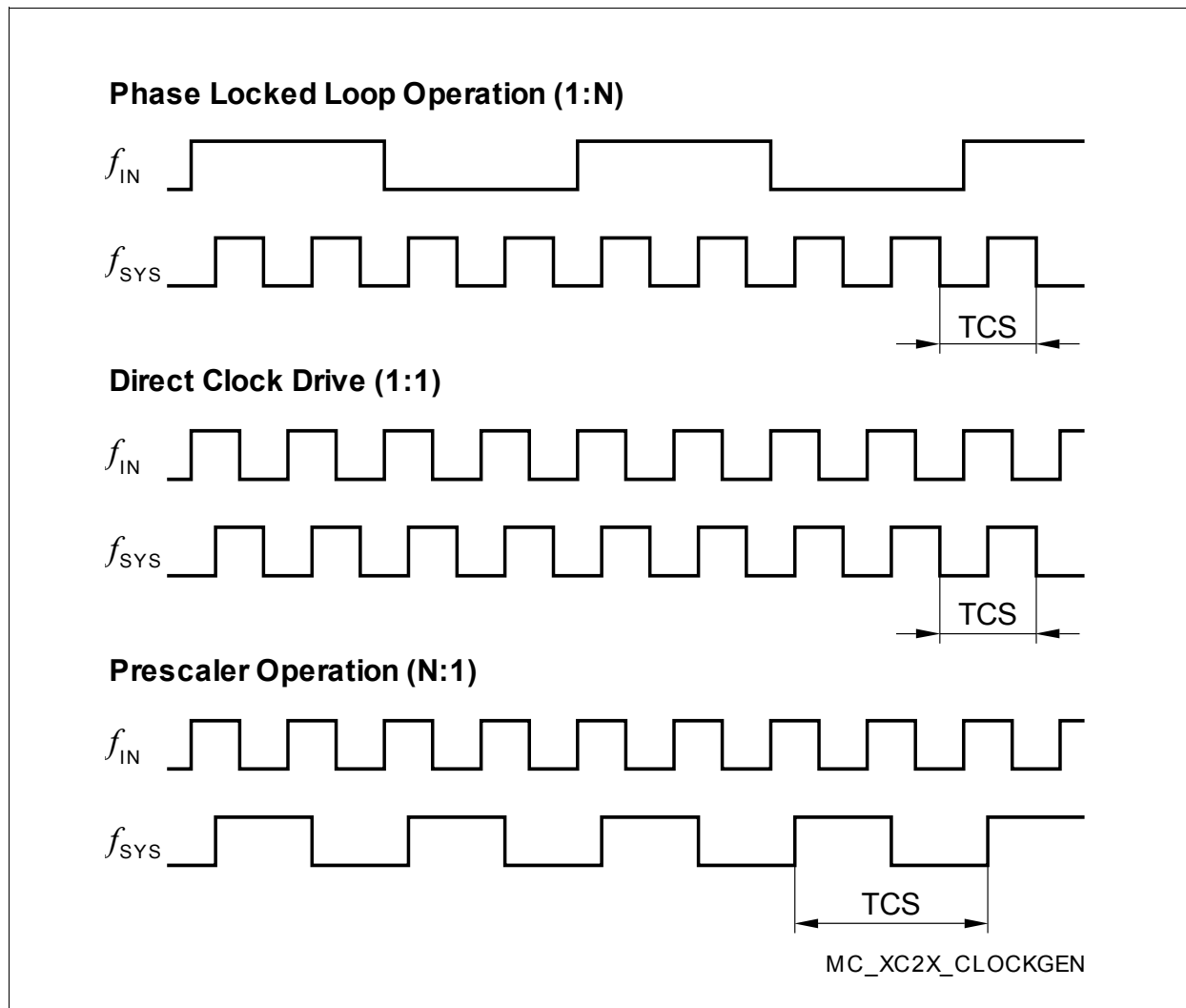


Figure 18 Generation Mechanisms for the System Clock

Note: The example of PLL operation shown in [Figure 18](#) uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

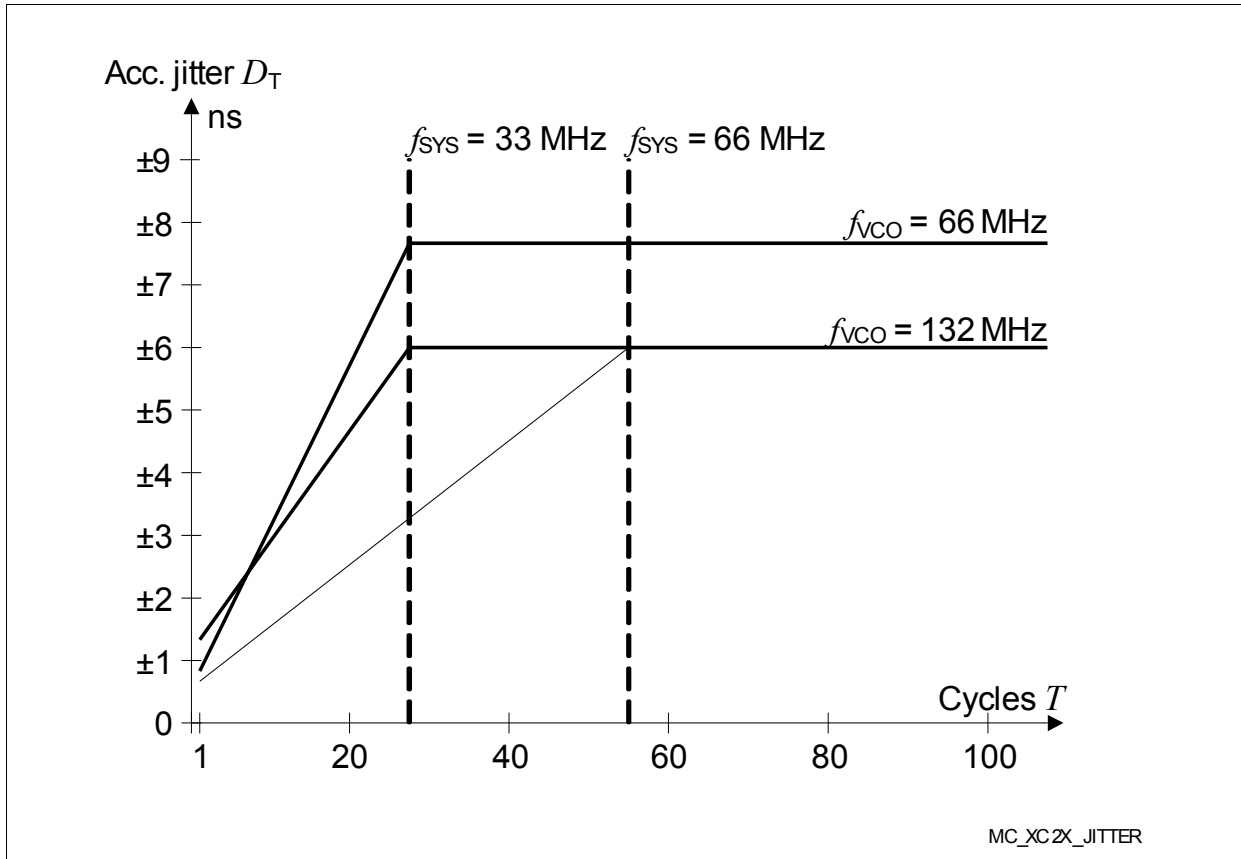


Figure 19 **Approximated Accumulated PLL Jitter**

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20$ pF (see [Table 12](#)).

The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100/144 and V_{SS} pin 1) is limited to a peak-to-peak voltage of $V_{PP} = 50$ mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 25 **VCO Bands for PLL Operation¹⁾**

PLLCON0.VCOSEL	VCO Frequency Range	Base Frequency Range
00	50 ... 110 MHz	10 ... 40 MHz
01	100 ... 160 MHz	20 ... 80 MHz
1X	Reserved	

¹⁾ Not subject to production test - verified by design/characterization.

**Table 29 External Bus Cycle Timing for Upper Voltage Range
(Operating Conditions apply)**

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: $\overline{\text{RD}}$, $\overline{\text{WR}}(\text{L}/\text{H})$	t_{10} CC	–		13	ns	
Output valid delay for: $\overline{\text{BHE}}$, ALE	t_{11} CC	–		13	ns	
Output valid delay for: A23 ... A16, A15 ... A0 (on P0/P1)	t_{12} CC	–		14	ns	
Output valid delay for: A15 ... A0 (on P2/P10)	t_{13} CC	–		14	ns	
Output valid delay for: $\overline{\text{CS}}$	t_{14} CC	–		13	ns	
Output valid delay for: D15 ... D0 (write data, MUX-mode)	t_{15} CC	–		14	ns	
Output valid delay for: D15 ... D0 (write data, DEMUX-mode)	t_{16} CC	–		14	ns	
Output hold time for: $\overline{\text{RD}}$, $\overline{\text{WR}}(\text{L}/\text{H})$	t_{20} CC	0		8	ns	
Output hold time for: $\overline{\text{BHE}}$, ALE	t_{21} CC	0		8	ns	
Output hold time for: A23 ... A16, A15 ... A0 (on P2/P10)	t_{23} CC	0		8	ns	
Output hold time for: $\overline{\text{CS}}$	t_{24} CC	0		8	ns	
Output hold time for: D15 ... D0 (write data)	t_{25} CC	0		8	ns	
Input setup time for: READY, D15 ... D0 (read data)	t_{30} SR	18		–	ns	
Input hold time for: READY, D15 ... D0 (read data) ¹⁾	t_{31} SR	-4		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of $\overline{\text{RD}}$. Address changes before the end of $\overline{\text{RD}}$ have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of $\overline{\text{RD}}$.

External Bus Arbitration

If the arbitration signals are enabled, the XE167 makes its external resources available in response to an arbitration request.

**Table 31 Bus Arbitration Timing for Upper Voltage Range
(Operating Conditions apply)**

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Input setup time for: HOLD input	t_{40} SR	18		–	ns	
Output delay rising edge for: HLDA, BREQ	t_{41} CC	0		13	ns	
Output delay falling edge for: HLDA	t_{42} CC	1		14	ns	

**Table 32 Bus Arbitration Timing for Lower Voltage Range
(Operating Conditions apply)**

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Input setup time for: HOLD input	t_{40} SR	28		–	ns	
Output delay rising edge for: HLDA, BREQ	t_{41} CC	0		19	ns	
Output delay falling edge for: HLDA	t_{42} CC	1		21	ns	

4.6.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

**Table 33 SSC Master/Slave Mode Timing for Upper Voltage Range
(Operating Conditions apply), $C_L = 50$ pF**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	—	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$0.5 \times t_{\text{BIT}}$	—	3)	ns	
Transmit data output valid time	t_3 CC	-6	—	13	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-7	—	—	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	7	—	—	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	5	—	—	ns	7)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	7	—	—	ns	7)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	5	—	—	ns	7)
Data output DOUT valid time	t_{14} CC	8	—	29	ns	7)

1) The maximum value further depends on the settings for the slave select output leading delay.

2) $t_{SYS} = 1/f_{SYS}$ (= 12.5 ns @ 80 MHz)

3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

5.2 Thermal Considerations

When operating the XE167 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$ ” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 125 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$$P_{INT} = V_{DDP} \times I_{DDP} \text{ (see Section 4.2.3).}$$

The static external power consumption caused by the output drivers is defined as

$$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers