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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 66MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 118 |
| Program Memory Size | 576KB (576K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 50K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-144-4 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xe167f72f66lacfxqma1 |

**Table 1 XE167 Derivative Synopsis**

| Derivative[1] | Temp. Range | Program Memory[2] | PSRAM[3] | CCU6 Mod. | ADC[4] Chan. | Interfaces[4] |
|---|---|---|---|---|---|---|
| SAF-XE167F-48F66L | -40 °C to 85 °C | 384 Kbytes Flash | 16 Kbytes | 0, 1, 2, 3 | 16 + 8 | 5 CAN Nodes, 6 Serial Chan. |
| SAF-XE167F-72F66L | -40 °C to 85 °C | 576 Kbytes Flash | 32 Kbytes | 0, 1, 2, 3 | 16 + 8 | 5 CAN Nodes, 6 Serial Chan. |
| SAF-XE167F-96FxxL | -40 °C to 85 °C | 768 Kbytes Flash | 64 Kbytes | 0, 1, 2, 3 | 16 + 8 | 5 CAN Nodes, 6 Serial Chan. |
| SAF-XE167G-48F66L | -40 °C to 85 °C | 384 Kbytes Flash | 16 Kbytes | 0, 1 | 8 + 8 | 2 CAN Nodes, 4 Serial Chan. |
| SAF-XE167G-72F66L | -40 °C to 85 °C | 576 Kbytes Flash | 32 Kbytes | 0, 1 | 8 + 8 | 2 CAN Nodes, 4 Serial Chan. |
| SAF-XE167G-96F66L | -40 °C to 85 °C | 768 Kbytes Flash | 64 Kbytes | 0, 1 | 8 + 8 | 2 CAN Nodes, 4 Serial Chan. |
| SAF-XE167H-48F66L | -40 °C to 85 °C | 384 Kbytes Flash | 16 Kbytes | 0, 1, 2, 3 | 16 + 8 | No CAN Node, 6 Serial Chan. |
| SAF-XE167H-72F66L | -40 °C to 85 °C | 576 Kbytes Flash | 32 Kbytes | 0, 1, 2, 3 | 16 + 8 | No CAN Node, 6 Serial Chan. |
| SAF-XE167H-96F66L | -40 °C to 85 °C | 768 Kbytes Flash | 64 Kbytes | 0, 1, 2, 3 | 16 + 8 | No CAN Node, 6 Serial Chan. |
| SAF-XE167K-48F66L | -40 °C to 85 °C | 384 Kbytes Flash | 16 Kbytes | 0, 1 | 8 + 8 | No CAN Node, 4 Serial Chan. |
| SAF-XE167K-72F66L | -40 °C to 85 °C | 576 Kbytes Flash | 32 Kbytes | 0, 1 | 8 + 8 | No CAN Node, 4 Serial Chan. |
| SAF-XE167K-96F66L | -40 °C to 85 °C | 768 Kbytes Flash | 64 Kbytes | 0, 1 | 8 + 8 | No CAN Node, 4 Serial Chan. |

1) This Data Sheet is valid for devices starting with and including design step AC.

2) Specific inormation about the on-chip Flash memory in **Table 2**.

3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM.

4) Specific information about the available channels in **Table 3**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

### Notes to Pin Definitions

1. ***Ctrl.**: The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bitfield PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.*
   *Output signal OH is controlled by hardware.*
2. ***Type**: Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).*

**Table 4 Pin Definitions and Functions**

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 3 | $\overline{\text{TESTM}}$ | I | In/B | **Testmode Enable**<br>Enables factory test modes, must be held HIGH for normal operation (connect to $V_{DDPB}$).<br>An internal pullup device will hold this pin high when nothing is driving it. |
| 4 | P7.2 | O0 / I | St/B | **Bit 2 of Port 7, General Purpose Input/Output** |
| | EMUX0 | O1 | St/B | **External Analog MUX Control Output 0 (ADC1)** |
| | TxDC4 | O2 | St/B | **CAN Node 4 Transmit Data Output** |
| | CCU62_ CCPOS0A | I | St/B | **CCU62 Position Input 0** |
| | TDI_C | I | St/B | **JTAG Test Data Input** |
| 5 | P8.4 | O0 / I | St/B | **Bit 4 of Port 8, General Purpose Input/Output** |
| | CCU60_ COUT61 | O1 | St/B | **CCU60 Channel 1 Output** |
| | TMS_D | I | St/B | **JTAG Test Mode Selection Input** |
| 6 | $\overline{\text{TRST}}$ | I | In/B | **Test-System Reset Input**<br>For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE167's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.<br>An internal pulldown device will hold this pin low when nothing is driving it. |
| 7 | P8.3 | O0 / I | St/B | **Bit 3 of Port 8, General Purpose Input/Output** |
| | CCU60_ COUT60 | O1 | St/B | **CCU60 Channel 0 Output** |
| | TDI_D | I | St/B | **JTAG Test Data Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 79 | P0.1 | O0 / I | St/B | **Bit 1 of Port 0, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CCU61_ CC61 | O3 / I | St/B | **CCU61 Channel 1 Input/Output** |
| | A1 | OH | St/B | **External Bus Interface Address Line 1** |
| | U1C0_DX0B | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX1A | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| 80 | P2.8 | O0 / I | DP/B | **Bit 8 of Port 2, General Purpose Input/Output** |
| | U0C1_ SCLKOUT | O1 | DP/B | **USIC0 Channel 1 Shift Clock Output** |
| | EXTCLK | O2 | DP/B | **Programmable Clock Signal Output** 1) |
| | CC2_21 | O3 / I | DP/B | **CAPCOM2 CC21IO Capture Inp./ Compare Out.** |
| | A21 | OH | DP/B | **External Bus Interface Address Line 21** |
| | U0C1_DX1D | I | DP/B | **USIC0 Channel 1 Shift Clock Input** |
| 81 | P4.7 | O0 / I | St/B | **Bit 7 of Port 4, General Purpose Input/Output** |
| | CC2_31 | O3 / I | St/B | **CAPCOM2 CC31IO Capture Inp./ Compare Out.** |
| | T4EUD | I | St/B | **GPT1 Timer T4 External Up/Down Control Input** |
| 82 | P2.9 | O0 / I | St/B | **Bit 9 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | CC2_22 | O3 / I | St/B | **CAPCOM2 CC22IO Capture Inp./ Compare Out.** |
| | A22 | OH | St/B | **External Bus Interface Address Line 22** |
| | CLKIN1 | I | St/B | **Clock Signal Input** |
| | TCK_A | I | St/B | **JTAG Clock Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 92 | TRef | IO | Sp/1 | **Control Pin for Core Voltage Generation** 2) |
| 93 | P3.2 | O0 / I | St/B | **Bit 2 of Port 3, General Purpose Input/Output** |
| | U2C0_ SCLKOUT | O1 | St/B | **USIC2 Channel 0 Shift Clock Output** |
| | TxDC3 | O2 | St/B | **CAN Node 3 Transmit Data Output** |
| | U2C0_DX1B | I | St/B | **USIC2 Channel 0 Shift Clock Input** |
| | HOLD | I | St/B | **External Bus Master Hold Request Input** |
| 94 | P2.10 | O0 / I | St/B | **Bit 10 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_ SELO3 | O2 | St/B | **USIC0 Channel 0 Select/Control 3 Output** |
| | CC2_23 | O3 / I | St/B | **CAPCOM2 CC23IO Capture Inp./ Compare Out.** |
| | A23 | OH | St/B | **External Bus Interface Address Line 23** |
| | U0C1_DX0E | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | CAPIN | I | St/B | **GPT2 Register CAPREL Capture Input** |
| 95 | P10.3 | O0 / I | St/B | **Bit 3 of Port 10, General Purpose Input/Output** |
| | CCU60_ COUT60 | O2 | St/B | **CCU60 Channel 0 Output** |
| | AD3 | OH / I | St/B | **External Bus Interface Address/Data Line 3** |
| | U0C0_DX2A | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX2A | I | St/B | **USIC0 Channel 1 Shift Control Input** |
| 96 | P0.5 | O0 / I | St/B | **Bit 5 of Port 0, General Purpose Input/Output** |
| | U1C1_ SCLKOUT | O1 | St/B | **USIC1 Channel 1 Shift Clock Output** |
| | U1C0_ SELO2 | O2 | St/B | **USIC1 Channel 0 Select/Control 2 Output** |
| | CCU61_ COUT62 | O3 | St/B | **CCU61 Channel 2 Output** |
| | A5 | OH | St/B | **External Bus Interface Address Line 5** |
| | U1C1_DX1A | I | St/B | **USIC1 Channel 1 Shift Clock Input** |
| | U1C0_DX1C | I | St/B | **USIC1 Channel 0 Shift Clock Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 115 | P10.9 | O0 / I | St/B | **Bit 9 of Port 10, General Purpose Input/Output** |
| | U0C0_ SELO4 | O1 | St/B | **USIC0 Channel 0 Select/Control 4 Output** |
| | U0C1_ MCLKOUT | O2 | St/B | **USIC0 Channel 1 Master Clock Output** |
| | AD9 | OH / I | St/B | **External Bus Interface Address/Data Line 9** |
| | CCU60_ CCPOS2A | I | St/B | **CCU60 Position Input 2** |
| | TCK_B | I | St/B | **JTAG Clock Input** |
| 116 | P1.1 | O0 / I | St/B | **Bit 1 of Port 1, General Purpose Input/Output** |
| | CCU62_ COUT62 | O1 | St/B | **CCU62 Channel 2 Output** |
| | U1C0_ SELO5 | O2 | St/B | **USIC1 Channel 0 Select/Control 5 Output** |
| | U2C1_DOUT | O3 | St/B | **USIC2 Channel 1 Shift Data Output** |
| | A9 | OH | St/B | **External Bus Interface Address Line 9** |
| | ESR2_3 | I | St/B | **ESR2 Trigger Input 3** |
| | EX1BINA | I | St/B | **External Interrupt Trigger Input** |
| | U2C1_DX0C | I | St/B | **USIC2 Channel 1 Shift Data Input** |
| 117 | P10.10 | O0 / I | St/B | **Bit 10 of Port 10, General Purpose Input/Output** |
| | U0C0_ SELO0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | CCU60_ COUT63 | O2 | St/B | **CCU60 Channel 3 Output** |
| | AD10 | OH / I | St/B | **External Bus Interface Address/Data Line 10** |
| | U0C0_DX2C | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | TDI_B | I | St/B | **JTAG Test Data Input** |
| | U0C1_DX1A | I | St/B | **USIC0 Channel 1 Shift Clock Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 118 | P10.11 | O0 / I | St/B | **Bit 11 of Port 10, General Purpose Input/Output** |
| | U1C0_ SCLKOUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | $\overline{\text{BRKOUT}}$ | O2 | St/B | **OCDS Break Signal Output** |
| | AD11 | OH / I | St/B | **External Bus Interface Address/Data Line 11** |
| | U1C0_DX1D | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | RxDC2B | I | St/B | **CAN Node 2 Receive Data Input** |
| | TMS_B | I | St/B | **JTAG Test Mode Selection Input** |
| 119 | P9.2 | O0 / I | St/B | **Bit 2 of Port 9, General Purpose Input/Output** |
| | CCU63_ CC62 | O1 / I | St/B | **CCU63 Channel 2 Input/Output** |
| 120 | P1.2 | O0 / I | St/B | **Bit 2 of Port 1, General Purpose Input/Output** |
| | CCU62_ CC62 | O1 / I | St/B | **CCU62 Channel 2 Input/Output** |
| | U1C0_ SELO6 | O2 | St/B | **USIC1 Channel 0 Select/Control 6 Output** |
| | U2C1_ SCLKOUT | O3 | St/B | **USIC2 Channel 1 Shift Clock Output** |
| | A10 | OH | St/B | **External Bus Interface Address Line 10** |
| | ESR1_4 | I | St/B | **ESR1 Trigger Input 4** |
| | CCU61_ T12HRB | I | St/B | **External Run Control Input for T12 of CCU61** |
| | EX2AINA | I | St/B | **External Interrupt Trigger Input** |
| | U2C1_DX0D | I | St/B | **USIC2 Channel 1 Shift Data Input** |
| | U2C1_DX1C | I | St/B | **USIC2 Channel 1 Shift Clock Input** |
| 121 | P10.12 | O0 / I | St/B | **Bit 12 of Port 10, General Purpose Input/Output** |
| | U1C0_DOUT | O1 | St/B | **USIC1 Channel 0 Shift Data Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | TDO_B | O3 | St/B | **JTAG Test Data Output** |
| | AD12 | OH / I | St/B | **External Bus Interface Address/Data Line 12** |
| | U1C0_DX0C | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX1E | I | St/B | **USIC1 Channel 0 Shift Clock Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 131 | P1.5 | O0 / I | St/B | **Bit 5 of Port 1, General Purpose Input/Output** |
| | CCU62_ COUT60 | O1 | St/B | **CCU62 Channel 0 Output** |
| | U1C1_ SELO3 | O2 | St/B | **USIC1 Channel 1 Select/Control 3 Output** |
| | $\overline{\text{BRKOUT}}$ | O3 | St/B | **OCDS Break Signal Output** |
| | A13 | OH | St/B | **External Bus Interface Address Line 13** |
| | U2C0_DX0C | I | St/B | **USIC2 Channel 0 Shift Data Input** |
| 132 | P9.6 | O0 / I | St/B | **Bit 6 of Port 9, General Purpose Input/Output** |
| | CCU63_ COUT63 | O1 | St/B | **CCU63 Channel 3 Output** |
| | CCU63_ COUT62 | O2 | St/B | **CCU63 Channel 2 Output** |
| | CCU63 _ CTRAPA | I | St/B | **CCU63 Emergency Trap Input** |
| | CCU60_ CCPOS1B | I | St/B | **CCU60 Position Input 1** |
| 133 | P1.6 | O0 / I | St/B | **Bit 6 of Port 1, General Purpose Input/Output** |
| | CCU62_ CC61 | O1 / I | St/B | **CCU62 Channel 1 Input/Output** |
| | U1C1_ SELO2 | O2 | St/B | **USIC1 Channel 1 Select/Control 2 Output** |
| | U2C0_DOUT | O3 | St/B | **USIC2 Channel 0 Shift Data Output** |
| | A14 | OH | St/B | **External Bus Interface Address Line 14** |
| | U2C0_DX0D | I | St/B | **USIC2 Channel 0 Shift Data Input** |
| 134 | P9.7 | O0 / I | St/B | **Bit 7 of Port 9, General Purpose Input/Output** |
| | CCU63_ CTRAPB | I | St/B | **CCU63 Emergency Trap Input** |
| | U2C0_DX1D | I | St/B | **USIC2 Channel 0 Shift Clock Input** |
| | CCU60_ CCPOS0B | I | St/B | **CCU60 Position Input 0** |

The XE167 includes an excellent mechanism to identify and process exceptions or error conditions that arise during run-time, the so-called ‘Hardware Traps’. A hardware trap causes an immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

**Table 7** shows all possible exceptions or error conditions that can arise during runtime:

**Table 7 Trap Summary**

| Exception Condition | Trap Flag | Trap Vector | Vector Location[1)] | Trap Number | Trap Priority |
|---|---|---|---|---|---|
| Reset Functions | – | RESET | xx’0000$_H$ | 00$_H$ | III |
| Class A Hardware Traps: | | | | | |
| • System Request 0 | SR0 | SR0TRAP | xx’0008$_H$ | 02$_H$ | II |
| • Stack Overflow | STKOF | STOTRAP | xx’0010$_H$ | 04$_H$ | II |
| • Stack Underflow | STKUF | STUTRAP | xx’0018$_H$ | 06$_H$ | II |
| • Software Break | SOFTBRK | SBRKTRAP | xx’0020$_H$ | 08$_H$ | II |
| Class B Hardware Traps: | | | | | |
| • System Request 1 | SR1 | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| • Undefined Opcode | UNDOPC | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| • Memory Access Error | ACER | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| • Protected Instruction Fault | PRTFLT | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| • Illegal Word Operand Access | ILLOPA | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| Reserved | – | – | [2C$_H$ - 3C$_H$] | [0B$_H$ - 0F$_H$] | – |
| Software Traps: • TRAP Instruction | – | – | Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$ | Any [00$_H$ - 7F$_H$] | Current CPU Priority |

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

## 3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XE167 provides a broad range of debug and emulation features. User software running on the XE167 can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This consists of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the debug interface, or via the external bus interface for increased performance.

The JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

## 3.6 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to a number of prescaled values of the internal system clock. It may also be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range for the timer period and resolution while allowing precise adjustments for application-specific requirements. An external count input for CAPCOM2 timer T7 allows event scheduling for the capture/compare registers with respect to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers. Each may be individually allocated to either CAPCOM2 timer T7 or T8 and programmed for a capture or compare function.
Each register of the CAPCOM2 module has one port pin associated with it. This serves as an input pin to trigger the capture function or as an output pin to indicate the occurrence of a compare event.

**Table 8 Compare Modes (CAPCOM2)**

| Compare Modes | Function |
|---|---|
| Mode 0 | Interrupt-only compare mode;<br>Several compare interrupts per timer period are possible |
| Mode 1 | Pin toggles on each compare match;<br>Several compare events per timer period are possible |
| Mode 2 | Interrupt-only compare mode;<br>Only one compare interrupt per timer period is generated |
| Mode 3 | Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow;<br>Only one compare event per timer period is generated |
| Double Register Mode | Two registers operate on one pin;<br>Pin toggles on each compare match;<br>Several compare events per timer period are possible |
| Single Event Mode | Generates single edges or pulses;<br>Can be used with any compare mode |

## 3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE167 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

## 4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE167 can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE167 are designed to operate in various driver modes. The DC parameter specifications refer to the current limits in **Table 13**.

**Table 13 Current Limits for Port Output Drivers**

| Port Output Driver Mode | Maximum Output Current ($I_{OLmax}$, $-I_{OHmax}$)[1] | | Nominal Output Current ($I_{OLnom}$, $-I_{OHnom}$) | |
|---|---|---|---|---|
| | $V_{DDP} \geq$ 4.5 V | $V_{DDP} <$ 4.5 V | $V_{DDP} \geq$ 4.5 V | $V_{DDP} <$ 4.5 V |
| **Strong driver** | 10 mA | 10 mA | 2.5 mA | 2.5 mA |
| **Medium driver** | 4.0 mA | 2.5 mA | 1.0 mA | 1.0 mA |
| **Weak driver** | 0.5 mA | 0.5 mA | 0.1 mA | 0.1 mA |

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring output pins, the total output current in each direction ($\Sigma I_{OL}$ and $\Sigma -I_{OH}$) must remain below 50 mA.

### 4.2.2 DC Parameters for Lower Voltage Area

These parameters apply to the lower IO voltage range, 3.0 V ≤ $V_{DDP}$ ≤ 4.5 V.

**Table 15 DC Characteristics for Lower Voltage Range (Operating Conditions apply)[1)]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input low voltage (all except XTAL1) | $V_{IL}$ SR | -0.3 | – | 0.3 × $V_{DDP}$ | V | – |
| Input high voltage (all except XTAL1) | $V_{IH}$ SR | 0.7 × $V_{DDP}$ | – | $V_{DDP}$ + 0.3 | V | – |
| Input Hysteresis[2)] | HYS CC | 0.07 × $V_{DDP}$ | – | – | V | $V_{DDP}$ in [V], Series resistance = 0 Ω |
| Output low voltage | $V_{OL}$ CC | – | – | 1.0 | V | $I_{OL} \le I_{OLmax}$[3)] |
| Output low voltage | $V_{OL}$ CC | – | – | 0.4 | V | $I_{OL} \le I_{OLnom}$[3)4)] |
| Output high voltage[5)] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \ge I_{OHmax}$[3)] |
| Output high voltage[5)] | $V_{OH}$ CC | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \ge I_{OHnom}$[3)4)] |
| Input leakage current (Port 5, Port 15)[6)] | $I_{OZ1}$ CC | – | ±10 | ±200 | nA | 0 V < $V_{IN}$ < $V_{DDP}$ |
| Input leakage current (all other)[6)7)] | $I_{OZ2}$ CC | – | ±0.2 | ±2.5 | µA | $T_J \le$ 110°C, 0.45 V < $V_{IN}$ < $V_{DDP}$ |
| Pull level keep current | $I_{PLK}$ | – | – | ±10 | µA | $V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn) |
| Pull level force current | $I_{PLF}$ | ±150 | – | – | µA | $V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn) |
| Pin capacitance[9)] (digital inputs/outputs) | $C_{IO}$ CC | – | – | 10 | pF | |

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{OV}$.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

Sample time and conversion time of the XE167's A/D converters are programmable. The timing above can be calculated using **Table 19**.
The limit values for $f_{ADCI}$ must not be exceeded when selecting the prescaler value.

**Table 19 A/D Converter Computation Table**

| GLOBCTR.5-0 (DIVA) | A/D Converter Analog Clock $f_{ADCI}$ | INPCRx.7-0 (STC) | Sample Time $t_S$ |
|---|---|---|---|
| $000000_B$ | $f_{SYS}$ | $00_H$ | $t_{ADCI} \times 2$ |
| $000001_B$ | $f_{SYS}$ / 2 | $01_H$ | $t_{ADCI} \times 3$ |
| $000010_B$ | $f_{SYS}$ / 3 | $02_H$ | $t_{ADCI} \times 4$ |
| : | $f_{SYS}$ / (DIVA+1) | : | $t_{ADCI} \times$ (STC+2) |
| $111110_B$ | $f_{SYS}$ / 63 | $FE_H$ | $t_{ADCI} \times 256$ |
| $111111_B$ | $f_{SYS}$ / 64 | $FF_H$ | $t_{ADCI} \times 257$ |

**Converter Timing Example A:**

Assumptions: $f_{SYS}$ = 80 MHz (i.e. $t_{SYS}$ = 12.5 ns), DIVA = $03_H$, STC = $00_H$
Analog clock $f_{ADCI}$ = $f_{SYS}$ / 4 = 20 MHz, i.e. $t_{ADCI}$ = 50 ns
Sample time $t_S$ = $t_{ADCI} \times 2$ = 100 ns

**Conversion 10-bit:**

$t_{C10} = 13 \times t_{ADCI} + 2 \times t_{SYS} = 13 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.675\ \mu s$

**Conversion 8-bit:**

$t_{C8} = 11 \times t_{ADCI} + 2 \times t_{SYS} = 11 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.575\ \mu s$

**Converter Timing Example B:**

Assumptions: $f_{SYS}$ = 40 MHz (i.e. $t_{SYS}$ = 25 ns), DIVA = $02_H$, STC = $03_H$
Analog clock $f_{ADCI}$ = $f_{SYS}$ / 3 = 13.3 MHz, i.e. $t_{ADCI}$ = 75 ns
Sample time $t_S$ = $t_{ADCI} \times 5$ = 375 ns

**Conversion 10-bit:**

$t_{C10} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.25\ \mu s$

**Conversion 8-bit:**

$t_{C8} = 14 \times t_{ADCI} + 2 \times t_{SYS} = 14 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.10\ \mu s$

**Table 21 Coding of Bitfields LEVxV in Register SWDCON0**

| Code | Default Voltage Level | Notes[1)] |
|---|---|---|
| $0000_B$ | 2.9 V | |
| $0001_B$ | 3.0 V | LEV1V: reset request |
| $0010_B$ | 3.1 V | |
| $0011_B$ | 3.2 V | |
| $0100_B$ | 3.3 V | |
| $0101_B$ | 3.4 V | |
| $0110_B$ | 3.6 V | |
| $0111_B$ | 4.0 V | |
| $1000_B$ | 4.2 V | |
| $1001_B$ | 4.5 V | LEV2V: no request |
| $1010_B$ | 4.6 V | |
| $1011_B$ | 4.7 V | |
| $1100_B$ | 4.8 V | |
| $1101_B$ | 4.9 V | |
| $1110_B$ | 5.0 V | |
| $1111_B$ | 5.5 V | |

1) The indicated default levels are selected automatically after a power reset.

**Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz**

| Code | Default Voltage Level | Notes[1)] |
|---|---|---|
| $000_B$ | 0.9 V | |
| $001_B$ | 1.0 V | |
| $010_B$ | 1.1 V | |
| $011_B$ | 1.2 V | |
| $100_B$ | 1.3 V | LEV1V: reset request |
| $101_B$ | 1.4 V | LEV2V: interrupt request |
| $110_B$ | 1.5 V | |
| $111_B$ | 1.6 V | |

1) The indicated default levels are selected automatically after a power reset.

### Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = $00_B$), the system clock is derived from the low-frequency wakeup clock source:

$f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

### Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bitfields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock ($f_{SYS}$) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.
Please refer to the Programmer's Guide.

### 4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE167. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels $V_{IL}$ and $V_{IH}$. In connected to XTAL1, a minimum amplitude $V_{AX1}$ (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

*Note: The given clock timing parameters ($t_1$ … $t_4$) are only valid for an external clock input signal.*

**Table 26 External Clock Input Characteristics (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input voltage range limits for signal on XTAL1 | $V_{IX1}$ SR | -1.7 + $V_{DDI}$ | – | 1.7 | V | 1) |
| Input voltage (amplitude) on XTAL1 | $V_{AX1}$ SR | 0.3 × $V_{DDI}$ | – | – | V | Peak-to-peak voltage2) |
| XTAL1 input current | $I_{IL}$ CC | – | – | ±20 | µA | 0 V < $V_{IN}$ < $V_{DDI}$ |
| Oscillator frequency | $f_{OSC}$ CC | 4 | – | 40 | MHz | Clock signal |
| | | 4 | – | 16 | MHz | Crystal or Resonator |
| High time | $t_1$ SR | 6 | – | – | ns | |
| Low time | $t_2$ SR | 6 | – | – | ns | |
| Rise time | $t_3$ SR | – | 8 | 8 | ns | |
| Fall time | $t_4$ SR | – | 8 | 8 | ns | |

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage $V_{AX1}$ refers to the offset voltage $V_{OFF}$. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by $V_{IX1}$.

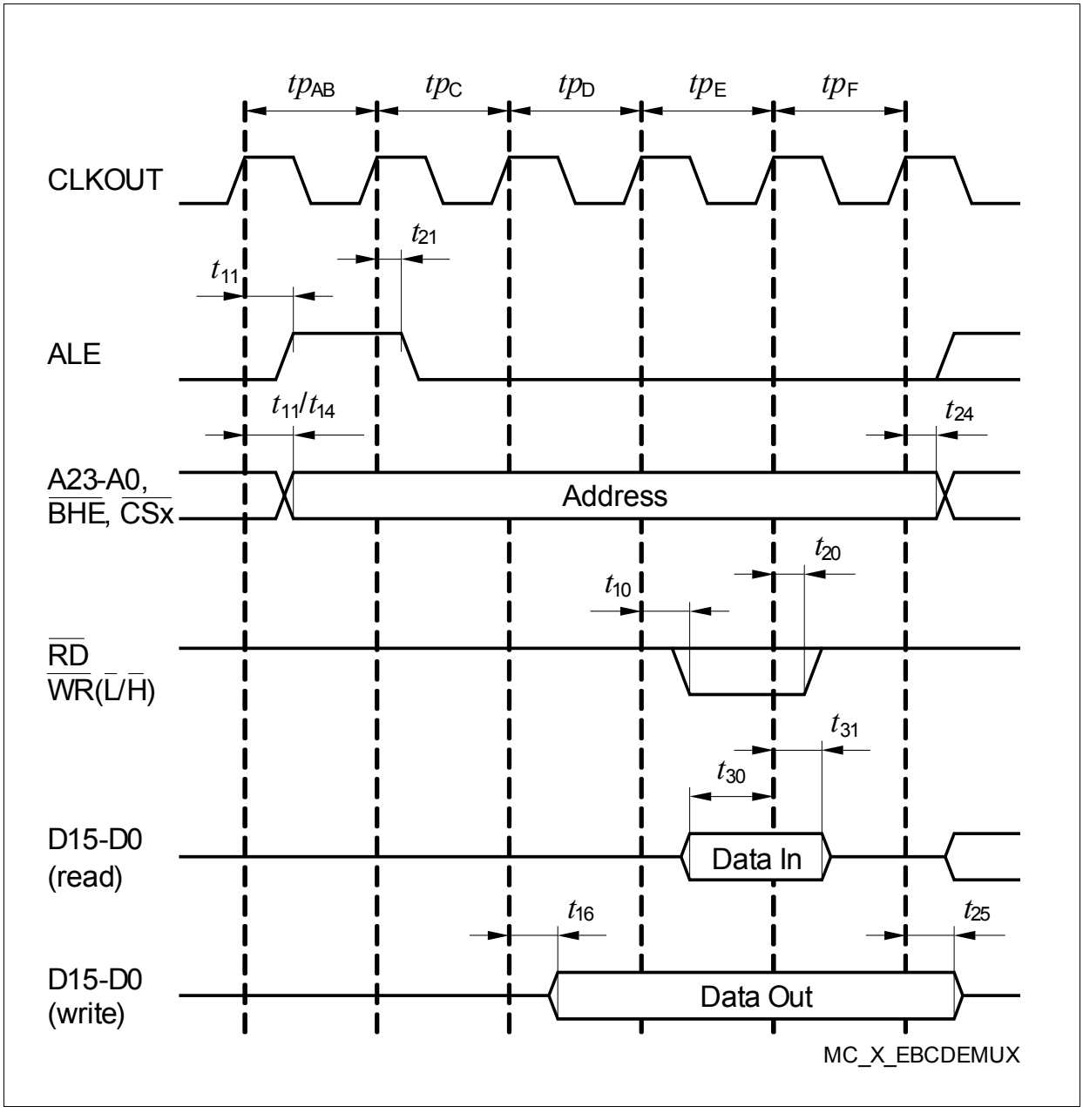


**Figure 23 Demultiplexed Bus Cycle**

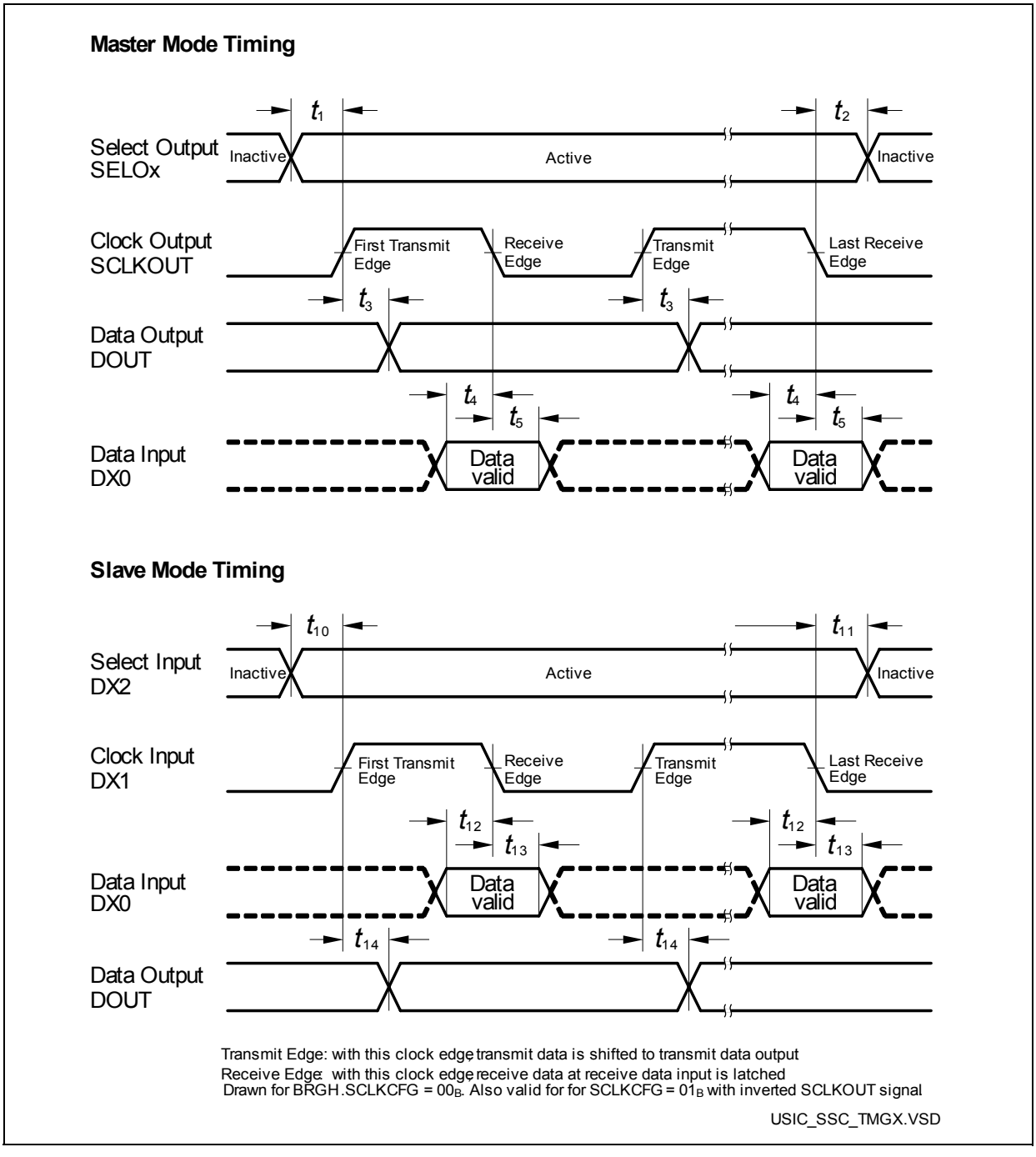


**Figure 27 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.*