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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/xe167f96f66lacfxqma1">https://www.e-xfl.com/product-detail/infineon-technologies/xe167f96f66lacfxqma1</a>

**Summary of Features**

- Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
- On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 5 CAN nodes and gateway functionality
- On-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Five programmable chip-select signals
  - Hold- and hold-acknowledge bus arbitration support
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 118 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via JTAG interface
- 144-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

**Ordering Information**

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

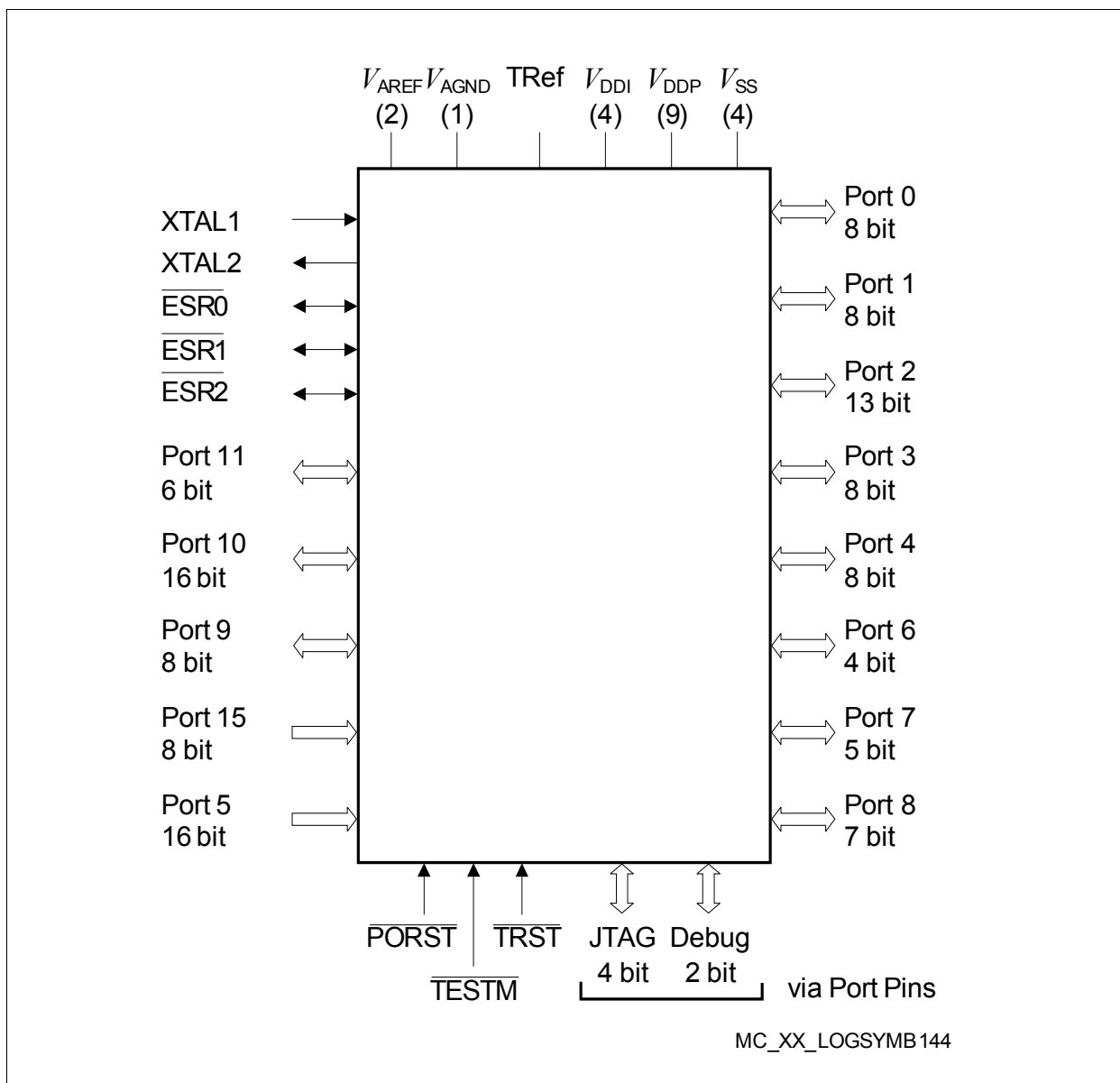
For ordering codes for the XE167 please contact your sales representative or local distributor.

This document describes several derivatives of the XE167 group. **Table 1** lists these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity the term **XE167** is used for all derivatives throughout this document.

## 2 General Device Information

The XE167 series of real time signal controllers is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.



**Figure 1** **Logic Symbol**

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
87	P0.3	O0 / I	St/B	<b>Bit 3 of Port 0, General Purpose Input/Output</b>
	U1C0_SELO0	O1	St/B	<b>USIC1 Channel 0 Select/Control 0 Output</b>
	U1C1_SELO1	O2	St/B	<b>USIC1 Channel 1 Select/Control 1 Output</b>
	CCU61_COUT60	O3	St/B	<b>CCU61 Channel 0 Output</b>
	A3	OH	St/B	<b>External Bus Interface Address Line 3</b>
	U1C0_DX2A	I	St/B	<b>USIC1 Channel 0 Shift Control Input</b>
	RxDC0B	I	St/B	<b>CAN Node 0 Receive Data Input</b>
88	P3.1	O0 / I	St/B	<b>Bit 1 of Port 3, General Purpose Input/Output</b>
	U2C0_DOUT	O1	St/B	<b>USIC2 Channel 0 Shift Data Output</b>
	TxDC3	O2	St/B	<b>CAN Node 3 Transmit Data Output</b>
	HLDA	OH / I	St/B	<b>External Bus Hold Acknowledge Output/Input</b> Output in master mode, input in slave mode.
	U2C0_DX0B	I	St/B	<b>USIC2 Channel 0 Shift Data Input</b>
89	P10.2	O0 / I	St/B	<b>Bit 2 of Port 10, General Purpose Input/Output</b>
	U0C0_SCLKOUT	O1	St/B	<b>USIC0 Channel 0 Shift Clock Output</b>
	CCU60_CC62	O2 / I	St/B	<b>CCU60 Channel 2 Input/Output</b>
	AD2	OH / I	St/B	<b>External Bus Interface Address/Data Line 2</b>
	U0C0_DX1B	I	St/B	<b>USIC0 Channel 0 Shift Clock Input</b>
90	P0.4	O0 / I	St/B	<b>Bit 4 of Port 0, General Purpose Input/Output</b>
	U1C1_SELO0	O1	St/B	<b>USIC1 Channel 1 Select/Control 0 Output</b>
	U1C0_SELO1	O2	St/B	<b>USIC1 Channel 0 Select/Control 1 Output</b>
	CCU61_COUT61	O3	St/B	<b>CCU61 Channel 1 Output</b>
	A4	OH	St/B	<b>External Bus Interface Address Line 4</b>
	U1C1_DX2A	I	St/B	<b>USIC1 Channel 1 Shift Control Input</b>
	RxDC1B	I	St/B	<b>CAN Node 1 Receive Data Input</b>

**Table 4 Pin Definitions and Functions (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
140	$\overline{\text{ESR2}}$	O0 / I	St/B	<b>External Service Request 2</b>
	U1C1_DX0D	I	St/B	<b>USIC1 Channel 1 Shift Data Input</b>
	U1C1_DX2C	I	St/B	<b>USIC1 Channel 1 Shift Control Input</b>
	U2C1_DX0E	I	St/B	<b>USIC1 Channel 1 Shift Data Input</b>
	U2C1_DX2B	I	St/B	<b>USIC2 Channel 1 Shift Control Input</b>
	EX1AINB	I	St/B	<b>External Interrupt Trigger Input</b>
141	$\overline{\text{ESR0}}$	O0 / I	St/B	<b>External Service Request 0</b> <i>Note: After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.</i>
	U1C0_DX0E	I	St/B	<b>USIC1 Channel 0 Shift Data Input</b>
	U1C0_DX2B	I	St/B	<b>USIC1 Channel 0 Shift Control Input</b>
142	P8.6	O0 / I	St/B	<b>Bit 6 of Port 8, General Purpose Input/Output</b>
	CCU60_COUT63	O1	St/B	<b>CCU60 Channel 3 Output</b>
	CCU60_CTRAPB	I	St/B	<b>CCU60 Emergency Trap Input</b>
	$\overline{\text{BRKIN\_D}}$	I	St/B	<b>OCDS Break Signal Input</b>
143	P8.5	O0 / I	St/B	<b>Bit 5 of Port 8, General Purpose Input/Output</b>
	CCU60_COUT62	O1	St/B	<b>CCU60 Channel 2 Output</b>
	TCK_D	I	St/B	<b>JTAG Clock Input</b>
15	$V_{\text{DDIM}}$	-	PS/M	<b>Digital Core Supply Voltage for Domain M</b> Decouple with a ceramic capacitor, see <a href="#">Table 12</a> for details.
54, 91, 127	$V_{\text{DDI1}}$	-	PS/1	<b>Digital Core Supply Voltage for Domain 1</b> Decouple with a ceramic capacitor, see <a href="#">Table 12</a> for details. All $V_{\text{DDI1}}$ pins must be connected to each other.
20	$V_{\text{DDPA}}$	-	PS/A	<b>Digital Pad Supply Voltage for Domain A</b> Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins. <i>Note: The A/D_Converters and ports P5, P6, and P15 are fed from supply voltage <math>V_{\text{DDPA}}</math>.</i>

**Functional Description**

**1024 bytes (2 × 512 bytes)** of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see [Table 5](#)) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

**Up to 768 Kbytes of on-chip Flash memory** store code, constant data, and control data. The on-chip Flash memory consists of up to three modules with a maximum capacity of 256 Kbytes each. Each module is organized in 4-Kbyte sectors.

The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

*Note: The actual size of the Flash memory depends on the chosen derivative (see [Table 1](#)).*

Each sector can be separately write protected<sup>1)</sup>, erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.

For Flash parameters, please see [Section 4.5](#).

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1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

### **3.2 External Bus Controller**

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections<sup>1)</sup>:

- Address Bus Width with a range of 0 ... 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes ... 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to five external  $\overline{\text{CS}}$  signals (four windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

A  $\overline{\text{HOLD}}/\overline{\text{HLDA}}$  protocol is available for bus arbitration; this allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software, after which pins P3.0 ... P3.2 ( $\overline{\text{BREQ}}$ ,  $\overline{\text{HLDA}}$ ,  $\overline{\text{HOLD}}$ ) are automatically controlled by the EBC. In Master Mode (default after reset) the  $\overline{\text{HLDA}}$  pin is an output. In Slave Mode pin  $\overline{\text{HLDA}}$  is switched to be an input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.

Access to very slow memories or modules with varying access times is supported by a special 'Ready' function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

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1) Bus modes are switched dynamically if several address windows with different mode settings are used.

### **3.6 Capture/Compare Unit (CAPCOM2)**

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to a number of prescaled values of the internal system clock. It may also be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range for the timer period and resolution while allowing precise adjustments for application-specific requirements. An external count input for CAPCOM2 timer T7 allows event scheduling for the capture/compare registers with respect to external events.

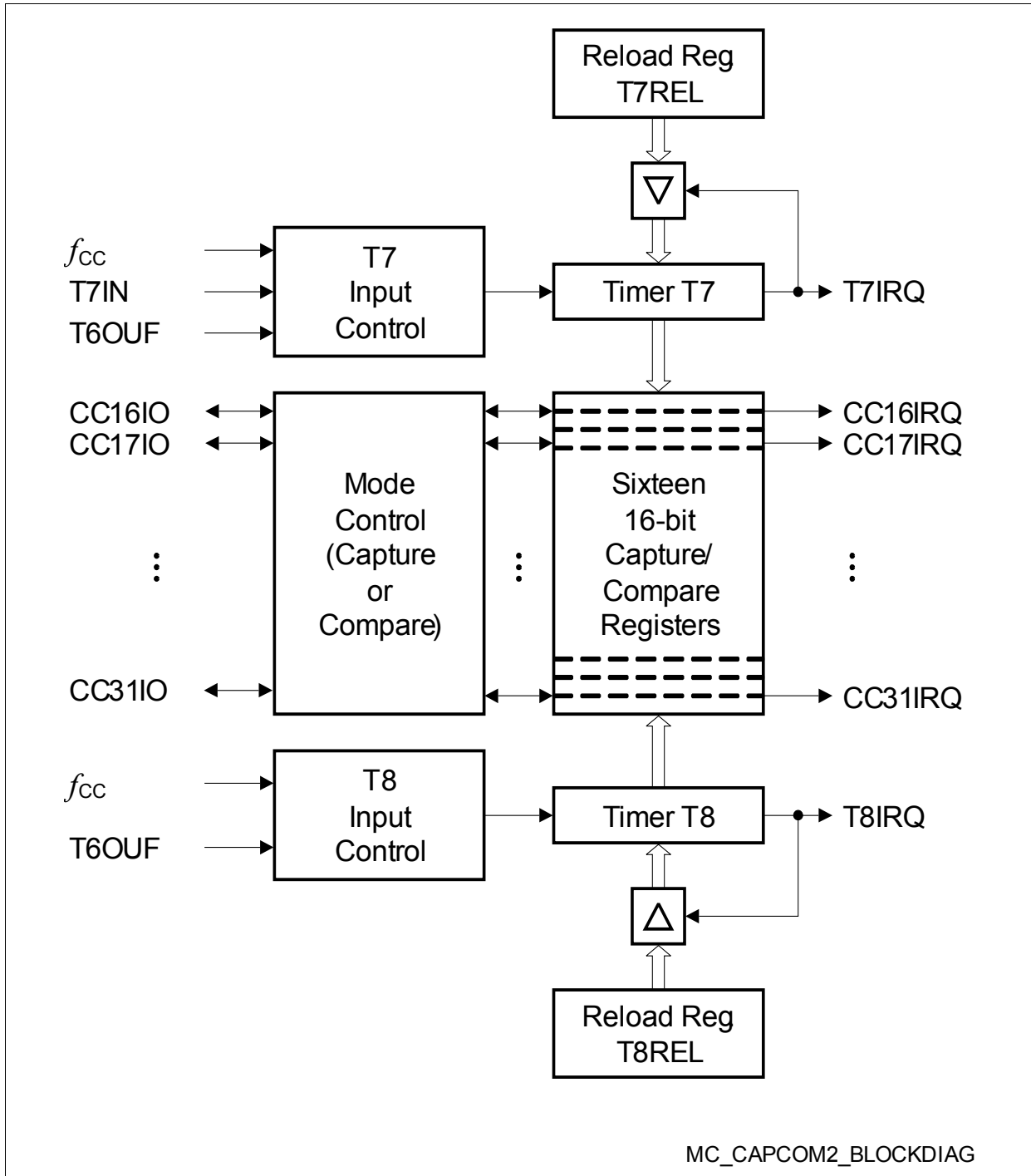
The capture/compare register array contains 16 dual purpose capture/compare registers. Each may be individually allocated to either CAPCOM2 timer T7 or T8 and programmed for a capture or compare function.

Each register of the CAPCOM2 module has one port pin associated with it. This serves as an input pin to trigger the capture function or as an output pin to indicate the occurrence of a compare event.

**Table 8 Compare Modes (CAPCOM2)**

<b>Compare Modes</b>	<b>Function</b>
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode





**Figure 5 CAPCOM2 Unit Block Diagram**

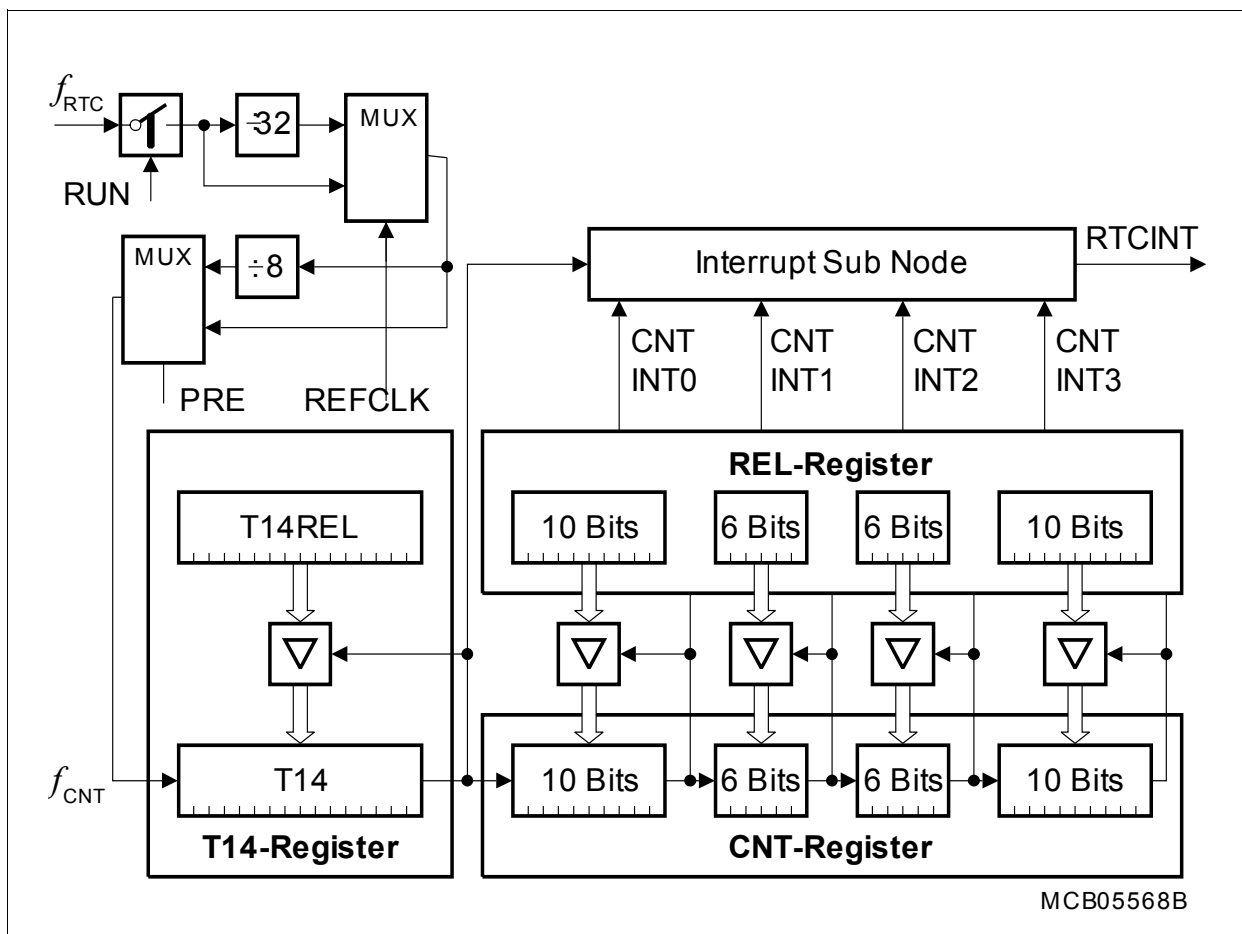
### 3.9 Real Time Clock

The Real Time Clock (RTC) module of the XE167 can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.



**Figure 9 RTC Block Diagram**

*Note: The registers associated with the RTC are only affected by a power reset.*

### **3.13 Watchdog Timer**

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2  $\mu$ s and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

### **3.14 Clock Generation**

The Clock Generation Unit can generate the system clock signal  $f_{\text{SYS}}$  for the XE167 from a number of external or internal clock sources:

- External clock signals with pad or core voltage levels
- External crystal using the on-chip oscillator
- On-chip clock source for operation without crystal
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals or from the on-chip clock source. See also [Section 4.6.2](#).

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

### 3.15 Parallel Ports

The XE167 provides up to 118 I/O lines which are organized into 11 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in [Table 9](#).

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

**Table 9 Summary of the XE167's Parallel Ports**

Port	Width	Alternate Functions
Port 0	8	Address lines, Serial interface lines of USIC1, CAN0, and CAN1, Input/Output lines for CCU61
Port 1	8	Address lines, Serial interface lines of USIC1 and USIC2, Input/Output lines for CCU62, OCDS control, interrupts
Port 2	13	Address and/or data lines, bus control, Serial interface lines of USIC0, CAN0, and CAN1, Input/Output lines for CCU60, CCU63, and CAPCOM2, Timer control signals, JTAG, interrupts, system clock output
Port 3	8	Bus arbitration signals, Serial interface lines of USIC0, USIC2, CAN3, and CAN4
Port 4	8	Chip select signals, Serial interface lines of CAN2, Input/Output lines for CAPCOM2, Timer control signals

**Functional Description**

**Table 10      Instruction Set Summary (cont'd)**

<b>Mnemonic</b>	<b>Description</b>	<b>Bytes</b>
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

- 1) The Enter Power Down Mode instruction is not used in the XE167, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

**Table 16      Switching Power Consumption XE167**  
**(Operating Conditions apply)**

Parameter	Sym- bol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	$I_{\text{SACT}}$	–	10 + $0.6 \times f_{\text{SYS}}$	10 + $1.0 \times f_{\text{SYS}}$	mA	Active mode <sup>1)2)</sup> $f_{\text{SYS}}$ in [MHz]
Power supply current in stopover mode, EVVRs on	$I_{\text{SSO}}$	–	1.0	2.0	mA	Stopover Mode <sup>2)</sup>

1) The pad supply voltage pins ( $V_{\text{DDPB}}$ ) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers' input stages are switched.

2) The pad supply voltage has only a minor influence on this parameter.

**Table 21**      **Coding of Bitfields LEVxV in Register SWDCON0**

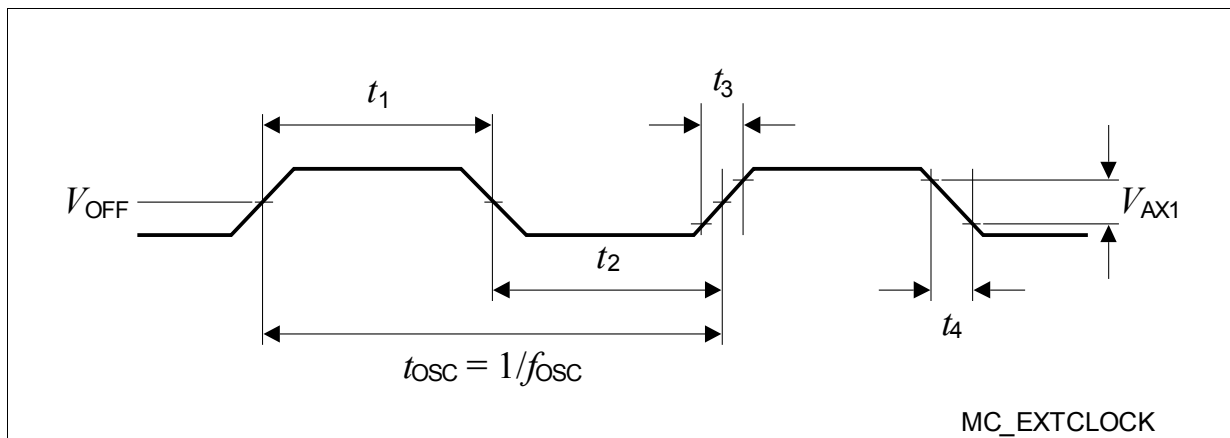
Code	Default Voltage Level	Notes <sup>1)</sup>
0000 <sub>B</sub>	2.9 V	
0001 <sub>B</sub>	3.0 V	LEV1V: reset request
0010 <sub>B</sub>	3.1 V	
0011 <sub>B</sub>	3.2 V	
0100 <sub>B</sub>	3.3 V	
0101 <sub>B</sub>	3.4 V	
0110 <sub>B</sub>	3.6 V	
0111 <sub>B</sub>	4.0 V	
1000 <sub>B</sub>	4.2 V	
1001 <sub>B</sub>	4.5 V	LEV2V: no request
1010 <sub>B</sub>	4.6 V	
1011 <sub>B</sub>	4.7 V	
1100 <sub>B</sub>	4.8 V	
1101 <sub>B</sub>	4.9 V	
1110 <sub>B</sub>	5.0 V	
1111 <sub>B</sub>	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

**Table 22**      **Coding of Bitfields LEVxV in Registers PVCyCONz**

Code	Default Voltage Level	Notes <sup>1)</sup>
000 <sub>B</sub>	0.9 V	
001 <sub>B</sub>	1.0 V	
010 <sub>B</sub>	1.1 V	
011 <sub>B</sub>	1.2 V	
100 <sub>B</sub>	1.3 V	LEV1V: reset request
101 <sub>B</sub>	1.4 V	LEV2V: interrupt request
110 <sub>B</sub>	1.5 V	
111 <sub>B</sub>	1.6 V	

1) The indicated default levels are selected automatically after a power reset.



**Figure 20 External Clock Drive XTAL1**

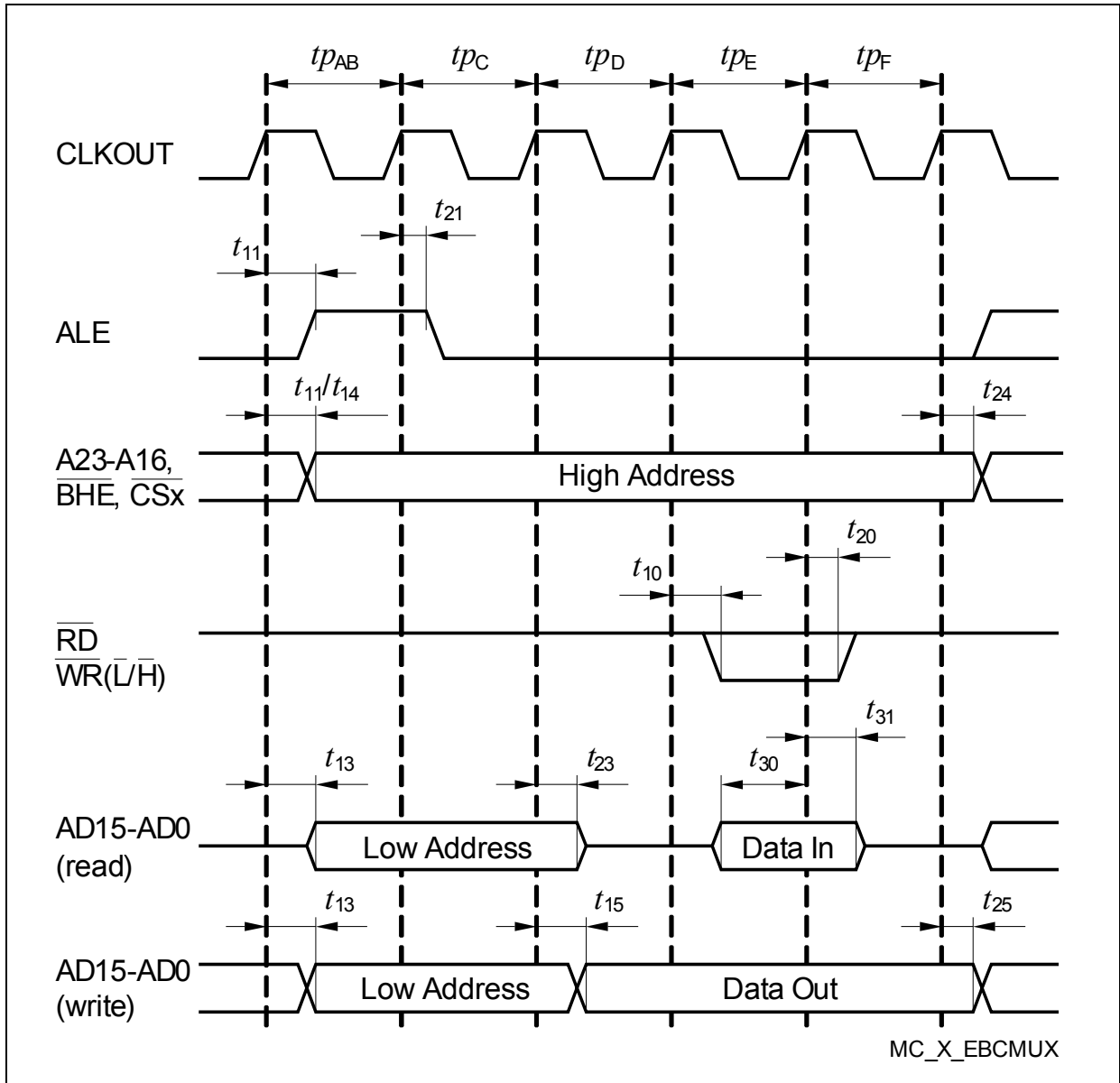
*Note: For crystal/resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation. Please refer to the limits specified by the crystal/resonator supplier.*



**Table 29 External Bus Cycle Timing for Upper Voltage Range  
(Operating Conditions apply)**

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: $\overline{\text{RD}}$ , $\overline{\text{WR}}(\text{L}/\text{H})$	$t_{10}$ CC	–		13	ns	
Output valid delay for: $\overline{\text{BHE}}$ , ALE	$t_{11}$ CC	–		13	ns	
Output valid delay for: A23 ... A16, A15 ... A0 (on P0/P1)	$t_{12}$ CC	–		14	ns	
Output valid delay for: A15 ... A0 (on P2/P10)	$t_{13}$ CC	–		14	ns	
Output valid delay for: $\overline{\text{CS}}$	$t_{14}$ CC	–		13	ns	
Output valid delay for: D15 ... D0 (write data, MUX-mode)	$t_{15}$ CC	–		14	ns	
Output valid delay for: D15 ... D0 (write data, DEMUX-mode)	$t_{16}$ CC	–		14	ns	
Output hold time for: $\overline{\text{RD}}$ , $\overline{\text{WR}}(\text{L}/\text{H})$	$t_{20}$ CC	0		8	ns	
Output hold time for: $\overline{\text{BHE}}$ , ALE	$t_{21}$ CC	0		8	ns	
Output hold time for: A23 ... A16, A15 ... A0 (on P2/P10)	$t_{23}$ CC	0		8	ns	
Output hold time for: $\overline{\text{CS}}$	$t_{24}$ CC	0		8	ns	
Output hold time for: D15 ... D0 (write data)	$t_{25}$ CC	0		8	ns	
Input setup time for: READY, D15 ... D0 (read data)	$t_{30}$ SR	18		–	ns	
Input hold time for: READY, D15 ... D0 (read data) <sup>1)</sup>	$t_{31}$ SR	-4		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of  $\overline{\text{RD}}$ . Address changes before the end of  $\overline{\text{RD}}$  have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of  $\overline{\text{RD}}$ .



**Figure 22 Multiplexed Bus Cycle**

**Bus Cycle Control with the READY Input**

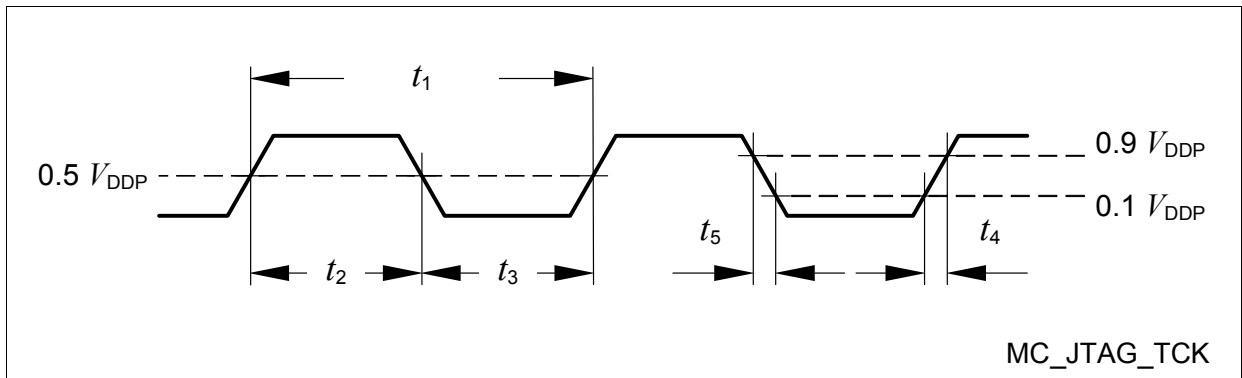
The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

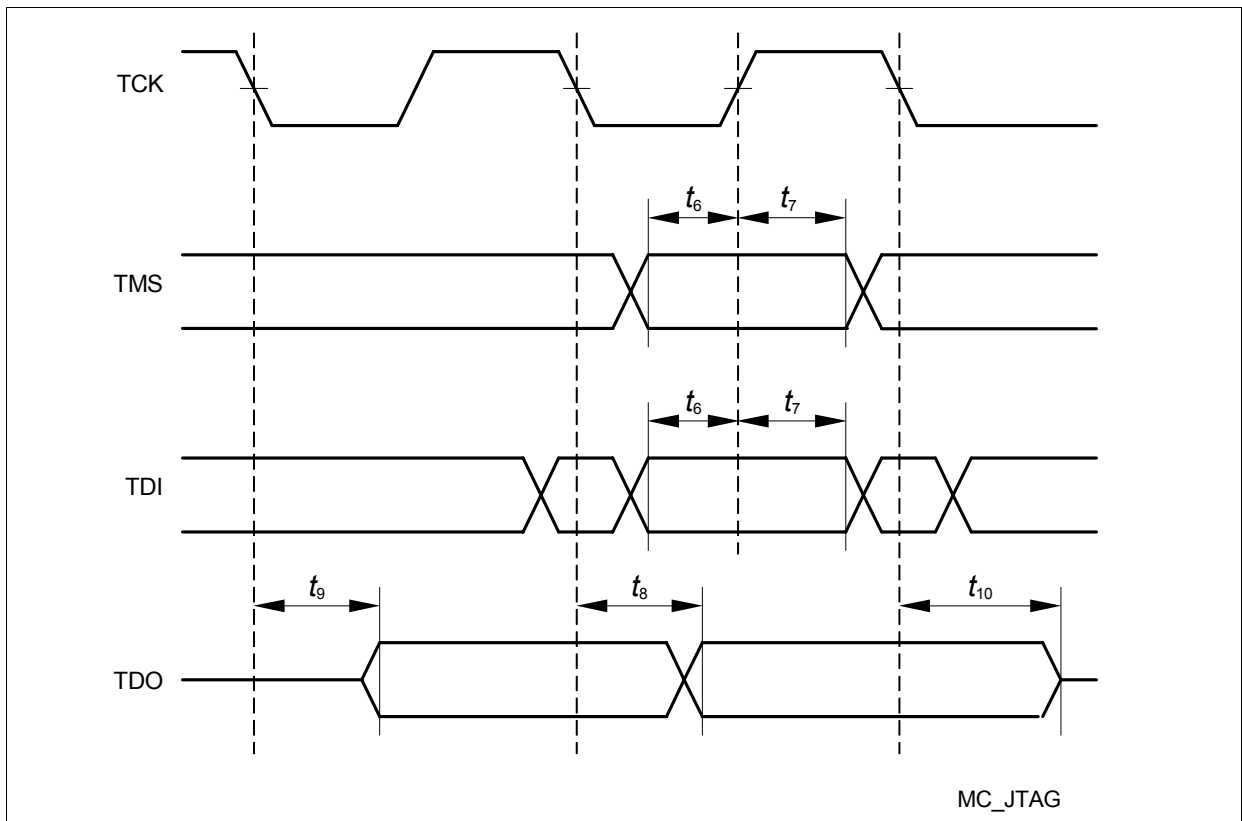
An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ( $\overline{RD}$  or  $\overline{WR}$ ).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.



**Figure 28 Test Clock Timing (TCK)**



**Figure 29 JTAG Timing**

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