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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe167f96f66lacfxuma1

Summary of Features

Table 1 XE167 Derivative Synopsis

Derivative¹⁾	Temp. Range	Program Memory²⁾	PSRAM³⁾	CCU6 Mod.	ADC⁴⁾ Chan.	Interfaces⁴⁾
SAF-XE167F-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XE167F-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XE167F-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XE167G-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	8 + 8	2 CAN Nodes, 4 Serial Chan.
SAF-XE167G-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	8 + 8	2 CAN Nodes, 4 Serial Chan.
SAF-XE167G-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	8 + 8	2 CAN Nodes, 4 Serial Chan.
SAF-XE167H-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2, 3	16 + 8	No CAN Node, 6 Serial Chan.
SAF-XE167H-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	No CAN Node, 6 Serial Chan.
SAF-XE167H-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2, 3	16 + 8	No CAN Node, 6 Serial Chan.
SAF-XE167K-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	8 + 8	No CAN Node, 4 Serial Chan.
SAF-XE167K-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	8 + 8	No CAN Node, 4 Serial Chan.
SAF-XE167K-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	8 + 8	No CAN Node, 4 Serial Chan.

1) This Data Sheet is valid for devices starting with and including design step AC.

2) Specific information about the on-chip Flash memory in [Table 2](#).

3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM.

4) Specific information about the available channels in [Table 3](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Summary of Features

The XE167 types are offered with several Flash memory sizes. [Table 2](#) describes the location of the available memory areas for each Flash memory size.

Table 2 Flash Memory Allocation

Total Flash Size	Flash Area A ¹⁾	Flash Area B	Flash Area C
768 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... CB'FFFF _H	n.a.
576 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C8'FFFF _H	n.a.
384 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C5'FFFF _H	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XE167 types are offered with different interface options. [Table 3](#) lists the available channels for each option.

Table 3 Interface Channel Association

Total Number	Available Channels
16 ADC0 channels	CH0 ... CH15
8 ADC0 channels	CH0 ... CH7
8 ADC1 channels	CH0 ... CH7
5 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4
2 CAN nodes	CAN0, CAN1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1
4 serial channels	U0C0, U0C1, U1C0, U1C1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT1 Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT2 Timer T6 Toggle Latch Output
	TDO_A	OH	St/B	JTAG Test Data Output
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input
9	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_ CCPOS1A	I	St/B	CCU62 Position Input 1
	TMS_C	I	St/B	JTAG Test Mode Selection Input
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
10	P8.2	O0 / I	St/B	Bit 2 of Port 8, General Purpose Input/Output
	CCU60_ CC62	O1 / I	St/B	CCU60 Channel 2 Input/Output
11	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	CCU62_ CTRAPA	I	St/B	CCU62 Emergency Trap Input
	BRKIN_C	I	St/B	OCDS Break Signal Input

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
66	P11.0	O0 / I	St/B	Bit 0 of Port 11, General Purpose Input/Output
	CCU63_ CCPOS0A	I	St/B	CCU63 Position Input 0
67	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output
	U0C0_ SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.
	A18	OH	St/B	External Bus Interface Address Line 18
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input
68	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.
	CS2	OH	St/B	External Bus Interface Chip Select 2 Output
	T2IN	I	St/B	GPT1 Timer T2 Count/Gate Input
69	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_ SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_ SELO1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
70	P4.4	O0 / I	St/B	Bit 4 of Port 4, General Purpose Input/Output
	CC2_28	O3 / I	St/B	CAPCOM2 CC28IO Capture Inp./ Compare Out.
	CS4	OH	St/B	External Bus Interface Chip Select 4 Output
	CLKIN2	I	St/B	RTC Count Clock Signal Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_ CC61	O3 / I	St/B	CCU61 Channel 1 Input/Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input
80	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_ SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output ¹⁾
	CC2_21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input
81	P4.7	O0 / I	St/B	Bit 7 of Port 4, General Purpose Input/Output
	CC2_31	O3 / I	St/B	CAPCOM2 CC31IO Capture Inp./ Compare Out.
	T4EUD	I	St/B	GPT1 Timer T4 External Up/Down Control Input
82	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input
	TCK_A	I	St/B	JTAG Clock Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output
	U1C0_SELO0	O1	St/B	USIC1 Channel 0 Select/Control 0 Output
	U1C1_SELO1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output
	CCU61_COUT60	O3	St/B	CCU61 Channel 0 Output
	A3	OH	St/B	External Bus Interface Address Line 3
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input
88	P3.1	O0 / I	St/B	Bit 1 of Port 3, General Purpose Input/Output
	U2C0_DOUT	O1	St/B	USIC2 Channel 0 Shift Data Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	HLDA	OH / I	St/B	External Bus Hold Acknowledge Output/Input Output in master mode, input in slave mode.
	U2C0_DX0B	I	St/B	USIC2 Channel 0 Shift Data Input
89	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC62	O2 / I	St/B	CCU60 Channel 2 Input/Output
	AD2	OH / I	St/B	External Bus Interface Address/Data Line 2
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
90	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COUT61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
104	P3.6	O0 / I	St/B	Bit 6 of Port 3, General Purpose Input/Output
	U2C1_DOUT	O1	St/B	USIC2 Channel 1 Shift Data Output
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	U0C0_SELO6	O3	St/B	USIC0 Channel 0 Select/Control 6 Output
	U2C1_DX0A	I	St/B	USIC2 Channel 1 Shift Data Input
	U2C1_DX1B	I	St/B	USIC2 Channel 1 Shift Clock Input
105	P10.7	O0 / I	St/B	Bit 7 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	AD7	OH / I	St/B	External Bus Interface Address/Data Line 7
	U0C1_DX0B	I	St/B	USIC0 Channel 1 Shift Data Input
	CCU60_CCPOS0A	I	St/B	CCU60 Position Input 0
	RxDC4C	I	St/B	CAN Node 4 Receive Data Input
106	P0.7	O0 / I	St/B	Bit 7 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	U1C0_SELO3	O2	St/B	USIC1 Channel 0 Select/Control 3 Output
	A7	OH	St/B	External Bus Interface Address Line 7
	U1C1_DX0B	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTRAPB	I	St/B	CCU61 Emergency Trap Input
107	P3.7	O0 / I	St/B	Bit 7 of Port 3, General Purpose Input/Output
	U2C1_DOUT	O1	St/B	USIC2 Channel 1 Shift Data Output
	U2C0_SELO3	O2	St/B	USIC2 Channel 0 Select/Control 3 Output
	U0C0_SELO7	O3	St/B	USIC0 Channel 0 Select/Control 7 Output
	U2C1_DX0B	I	St/B	USIC2 Channel 1 Shift Data Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
126	P9.5	O0 / I	St/B	Bit 5 of Port 9, General Purpose Input/Output
	CCU63_COUT62	O1	St/B	CCU63 Channel 2 Output
	U2C0_DOUT	O2	St/B	USIC2 Channel 0 Shift Data Output
	U2C0_DX0E	I	St/B	USIC2 Channel 0 Shift Data Input
	CCU60_CCPOS2B	I	St/B	CCU60 Position Input 2
128	P10.14	O0 / I	St/B	Bit 14 of Port 10, General Purpose Input/Output
	U1C0_SELO1	O1	St/B	USIC1 Channel 0 Select/Control 1 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	$\overline{\text{RD}}$	OH	St/B	External Bus Interface Read Strobe Output
	ESR2_2	I	St/B	ESR2 Trigger Input 2
	U0C1_DX0C	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC3C	I	St/B	CAN Node 3 Receive Data Input
129	P1.4	O0 / I	St/B	Bit 4 of Port 1, General Purpose Input/Output
	CCU62_COUT61	O1	St/B	CCU62 Channel 1 Output
	U1C1_SELO4	O2	St/B	USIC1 Channel 1 Select/Control 4 Output
	U2C0_SELO5	O3	St/B	USIC2 Channel 0 Select/Control 5 Output
	A12	OH	St/B	External Bus Interface Address Line 12
	U2C0_DX2B	I	St/B	USIC2 Channel 0 Shift Control Input
130	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input

3 Functional Description

The architecture of the XE167 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBUS, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE167.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE167.

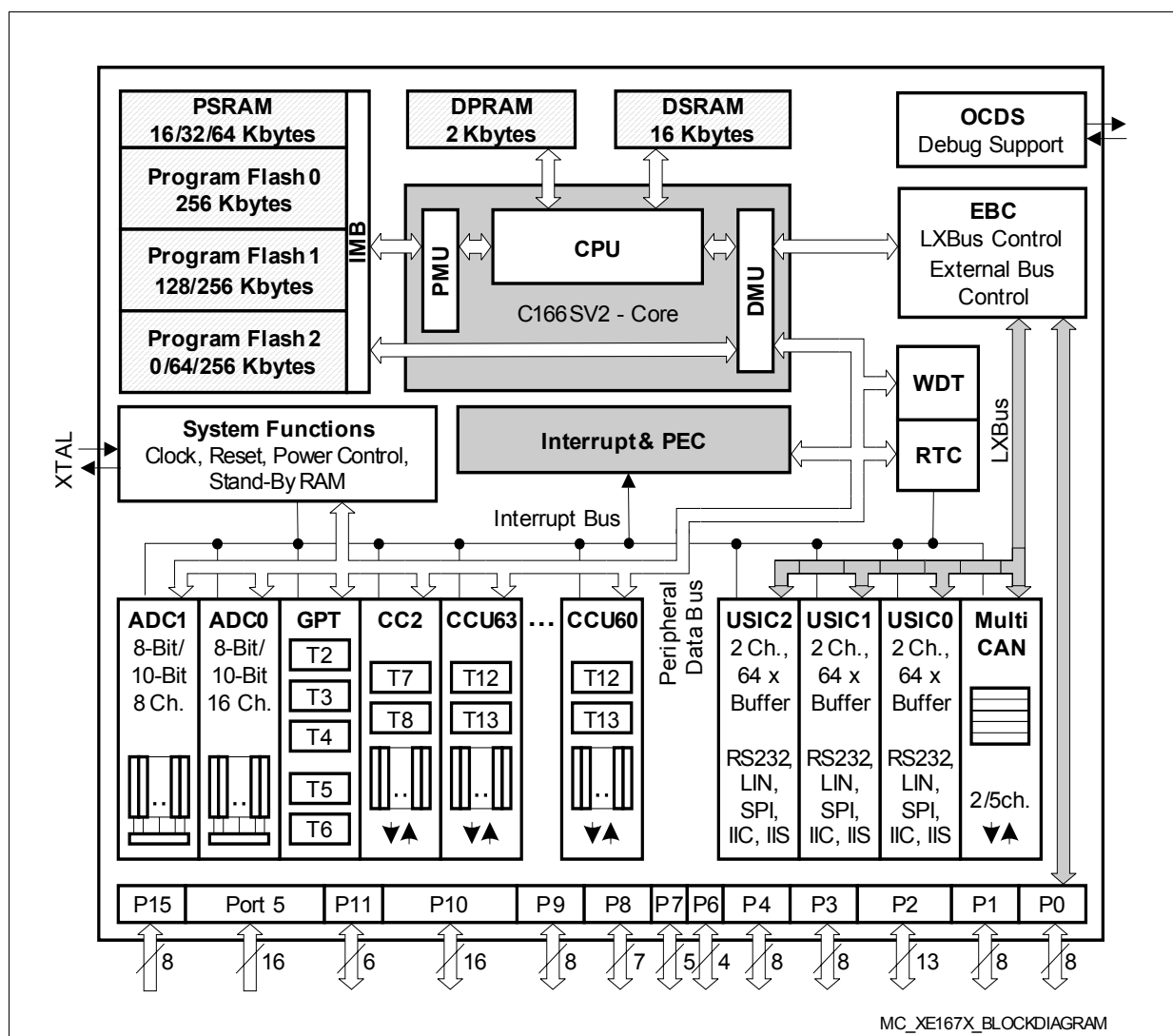


Figure 3 Block Diagram

Functional Description

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see [Table 5](#)) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Up to 768 Kbytes of on-chip Flash memory store code, constant data, and control data. The on-chip Flash memory consists of up to three modules with a maximum capacity of 256 Kbytes each. Each module is organized in 4-Kbyte sectors.

The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen derivative (see [Table 1](#)).

Each sector can be separately write protected¹⁾, erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.

For Flash parameters, please see [Section 4.5](#).

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

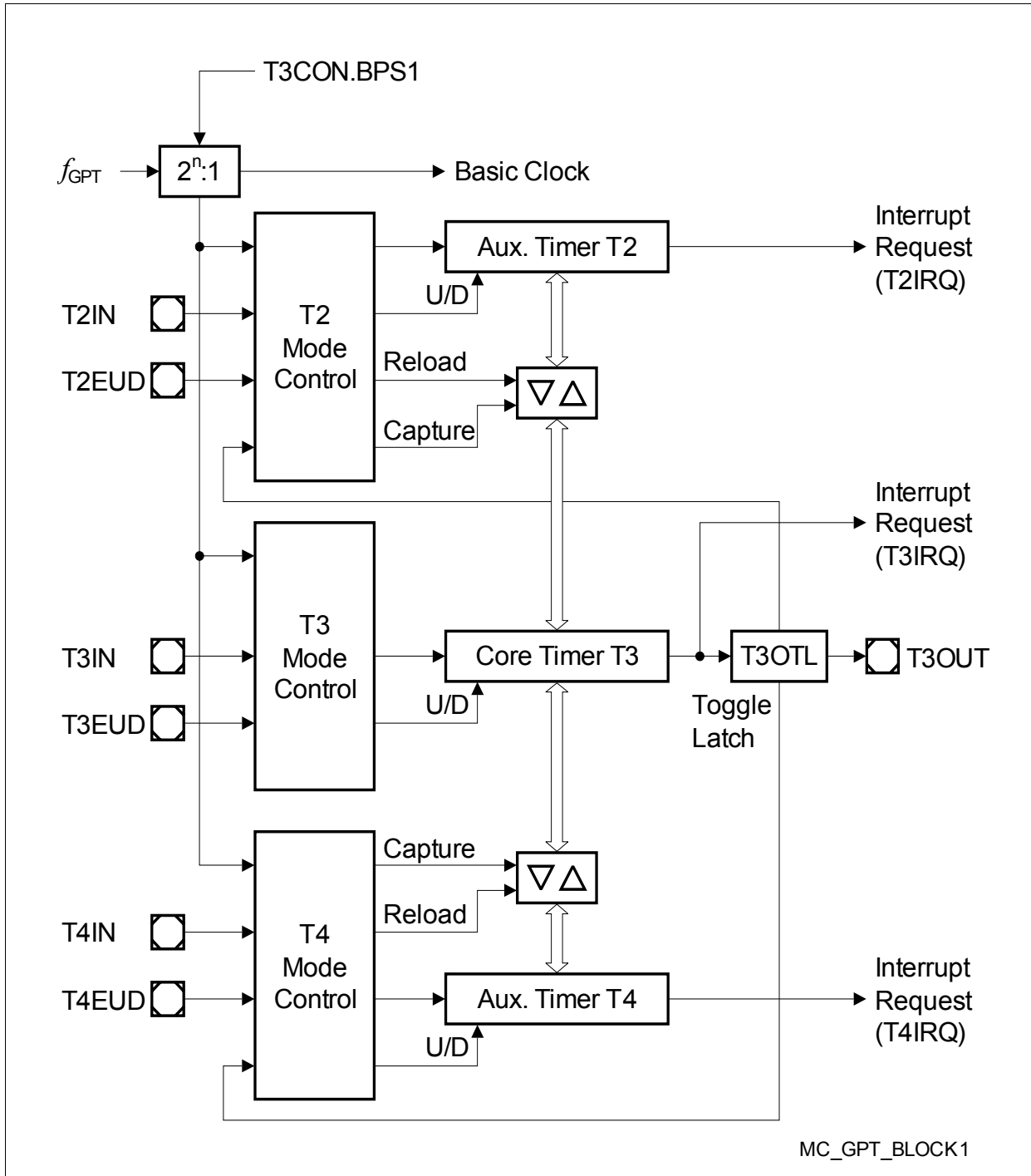


Figure 7 **Block Diagram of GPT1**

3.9 Real Time Clock

The Real Time Clock (RTC) module of the XE167 can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
 - a reloadable 10-bit timer
 - a reloadable 6-bit timer
 - a reloadable 6-bit timer
 - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

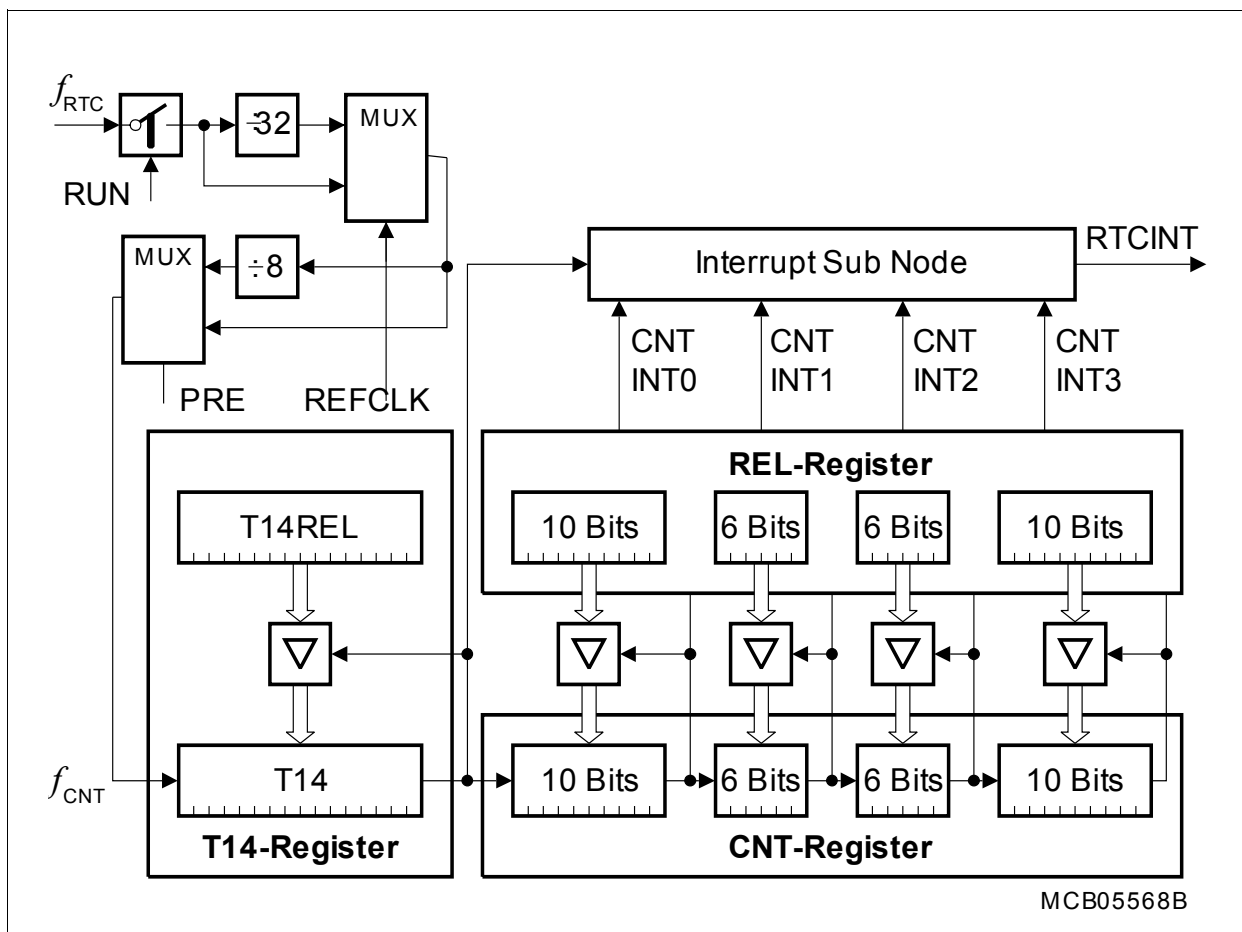


Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE167 can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of $dV/dt < 1 \text{ V/ms}$.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.

The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE167 are designed to operate in various driver modes. The DC parameter specifications refer to the current limits in [Table 13](#).

Table 13 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , $-I_{OHmax}$) ¹⁾		Nominal Output Current (I_{OLnom} , $-I_{OHnom}$)	
	$V_{DDP} \geq 4.5 \text{ V}$	$V_{DDP} < 4.5 \text{ V}$	$V_{DDP} \geq 4.5 \text{ V}$	$V_{DDP} < 4.5 \text{ V}$
Strong driver	10 mA	10 mA	2.5 mA	2.5 mA
Medium driver	4.0 mA	2.5 mA	1.0 mA	1.0 mA
Weak driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.

For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XE167 into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 20 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply watchdog (SWD) supervision level (see Table 21)	V_{SWD} CC	$V_{\text{LV}} - 0.150$	V_{LV}	$V_{\text{LV}} + 0.100$	V	V_{LV} = selected voltage in upper voltage area
		$V_{\text{LV}} - 0.125$	V_{LV}	$V_{\text{LV}} + 0.050$	V	V_{LV} = selected voltage in lower voltage area
Core voltage (PVC) supervision level (see Table 22)	V_{PVC} CC	$V_{\text{LV}} - 0.070$	V_{LV}	$V_{\text{LV}} + 0.030$	V	V_{LV} = selected voltage
Current control limit	I_{CC} CC	13	–	30	mA	Power domain DMP_M
		90	–	150	mA	Power domain DMP_1
Wakeup clock source frequency	f_{WU} CC	400	500	600	kHz	FREQSEL = 00 _B
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Startup time from stopover mode	t_{SSO} CC	200	260	320	μs	User instruction from PSRAM

4.6 AC Parameters

These parameters describe the dynamic behavior of the XE167.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

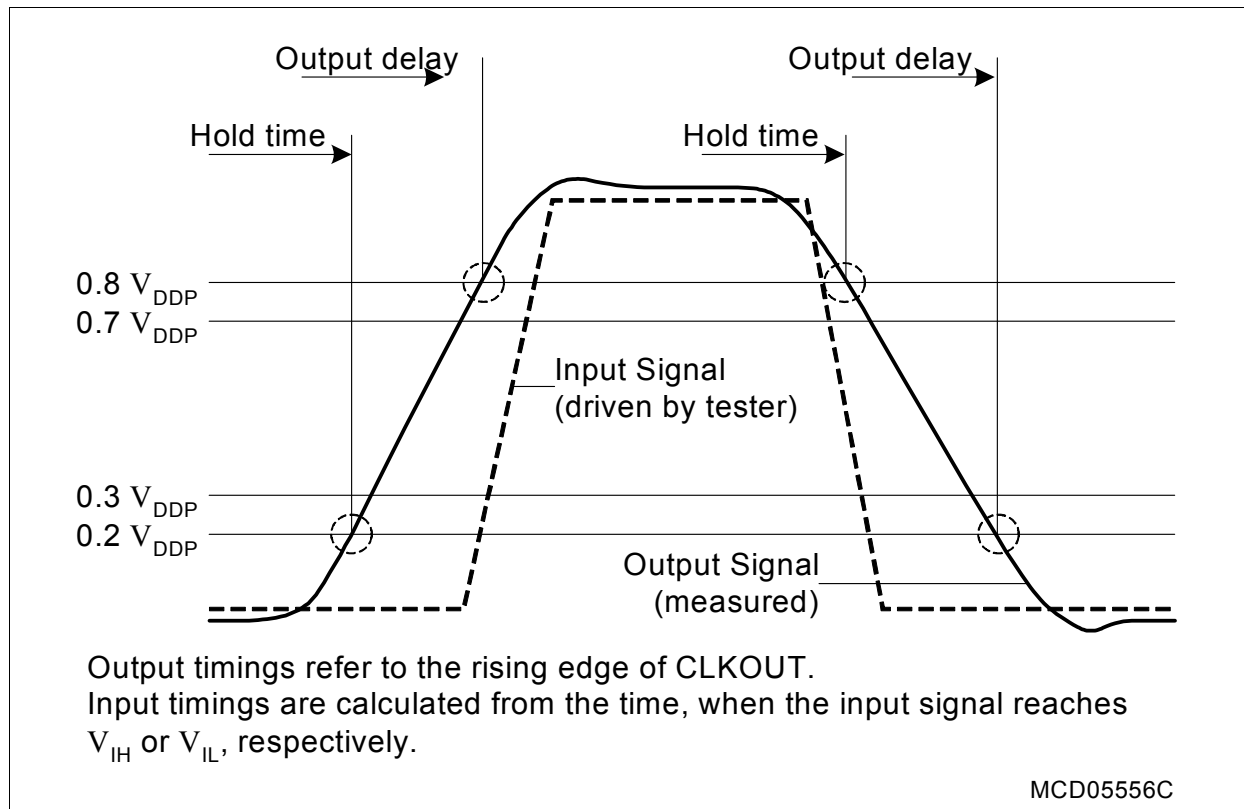


Figure 16 Input Output Waveforms

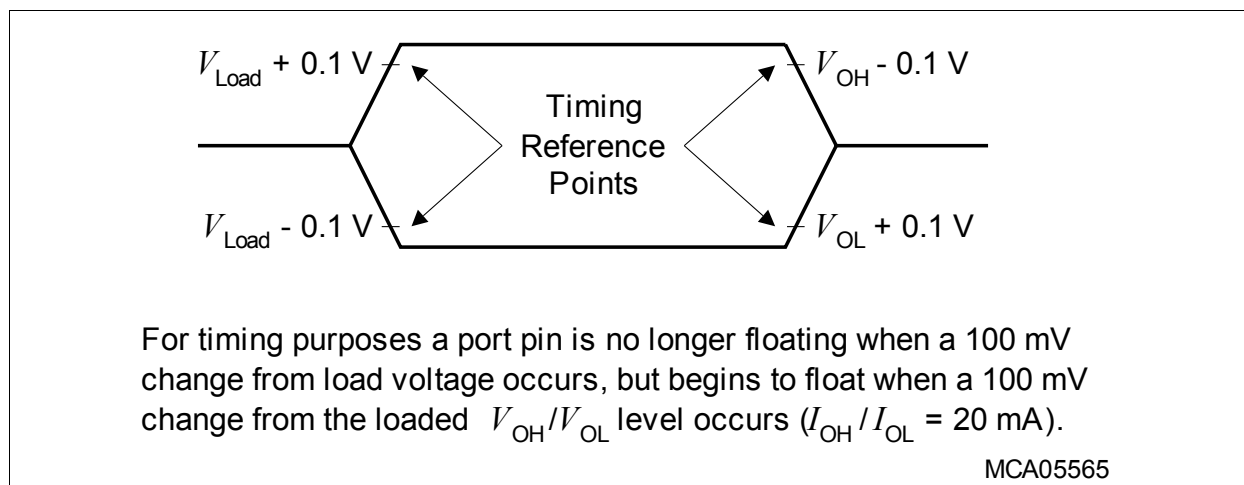


Figure 17 Floating Waveforms

4.6.4 External Bus Timing

The following parameters specify the behavior of the XE167 bus interface.

Table 27 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit	Note / Test Condition
			Min.	Max.		
CLKOUT cycle time	t_5	CC	40/25/12.5 ¹⁾		ns	
CLKOUT high time	t_6	CC	3	—	ns	
CLKOUT low time	t_7	CC	3	—	ns	
CLKOUT rise time	t_8	CC	—	3	ns	
CLKOUT fall time	t_9	CC	—	3	ns	

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to $f_{SYS} = 25/40/80$ MHz).
For longer periods the relative deviation decreases (see PLL deviation formula).

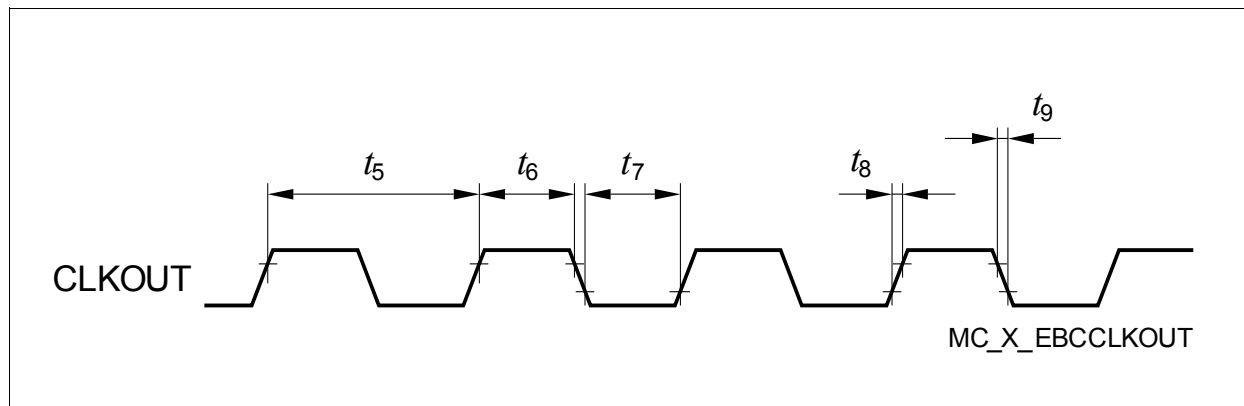


Figure 21 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

**Table 29 External Bus Cycle Timing for Upper Voltage Range
(Operating Conditions apply)**

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: $\overline{\text{RD}}$, $\overline{\text{WR}}(\text{L}/\text{H})$	t_{10} CC	–		13	ns	
Output valid delay for: $\overline{\text{BHE}}$, ALE	t_{11} CC	–		13	ns	
Output valid delay for: A23 ... A16, A15 ... A0 (on P0/P1)	t_{12} CC	–		14	ns	
Output valid delay for: A15 ... A0 (on P2/P10)	t_{13} CC	–		14	ns	
Output valid delay for: $\overline{\text{CS}}$	t_{14} CC	–		13	ns	
Output valid delay for: D15 ... D0 (write data, MUX-mode)	t_{15} CC	–		14	ns	
Output valid delay for: D15 ... D0 (write data, DEMUX-mode)	t_{16} CC	–		14	ns	
Output hold time for: $\overline{\text{RD}}$, $\overline{\text{WR}}(\text{L}/\text{H})$	t_{20} CC	0		8	ns	
Output hold time for: $\overline{\text{BHE}}$, ALE	t_{21} CC	0		8	ns	
Output hold time for: A23 ... A16, A15 ... A0 (on P2/P10)	t_{23} CC	0		8	ns	
Output hold time for: $\overline{\text{CS}}$	t_{24} CC	0		8	ns	
Output hold time for: D15 ... D0 (write data)	t_{25} CC	0		8	ns	
Input setup time for: READY, D15 ... D0 (read data)	t_{30} SR	18		–	ns	
Input hold time for: READY, D15 ... D0 (read data) ¹⁾	t_{31} SR	-4		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of $\overline{\text{RD}}$. Address changes before the end of $\overline{\text{RD}}$ have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of $\overline{\text{RD}}$.

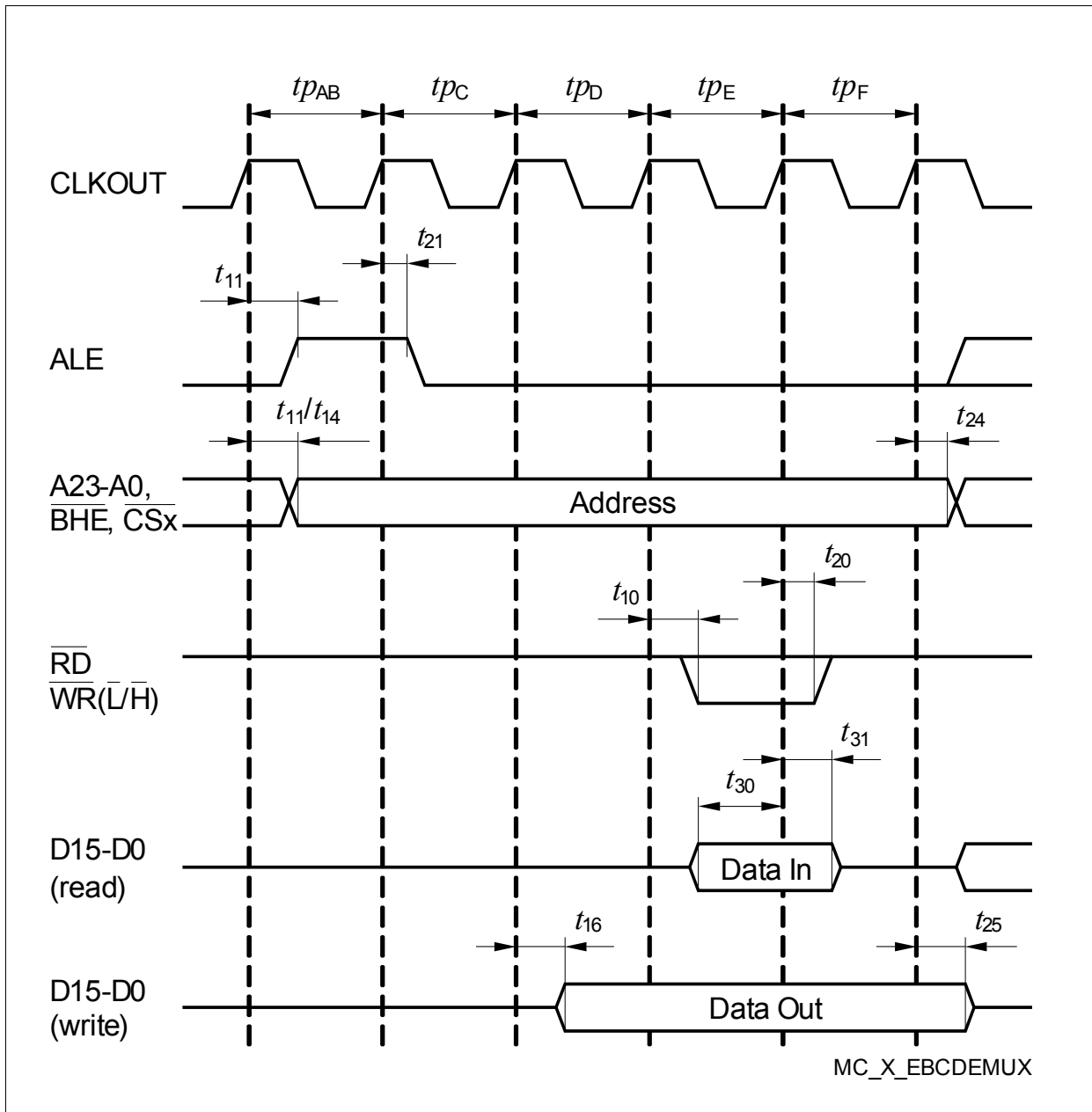


Figure 23 Demultiplexed Bus Cycle

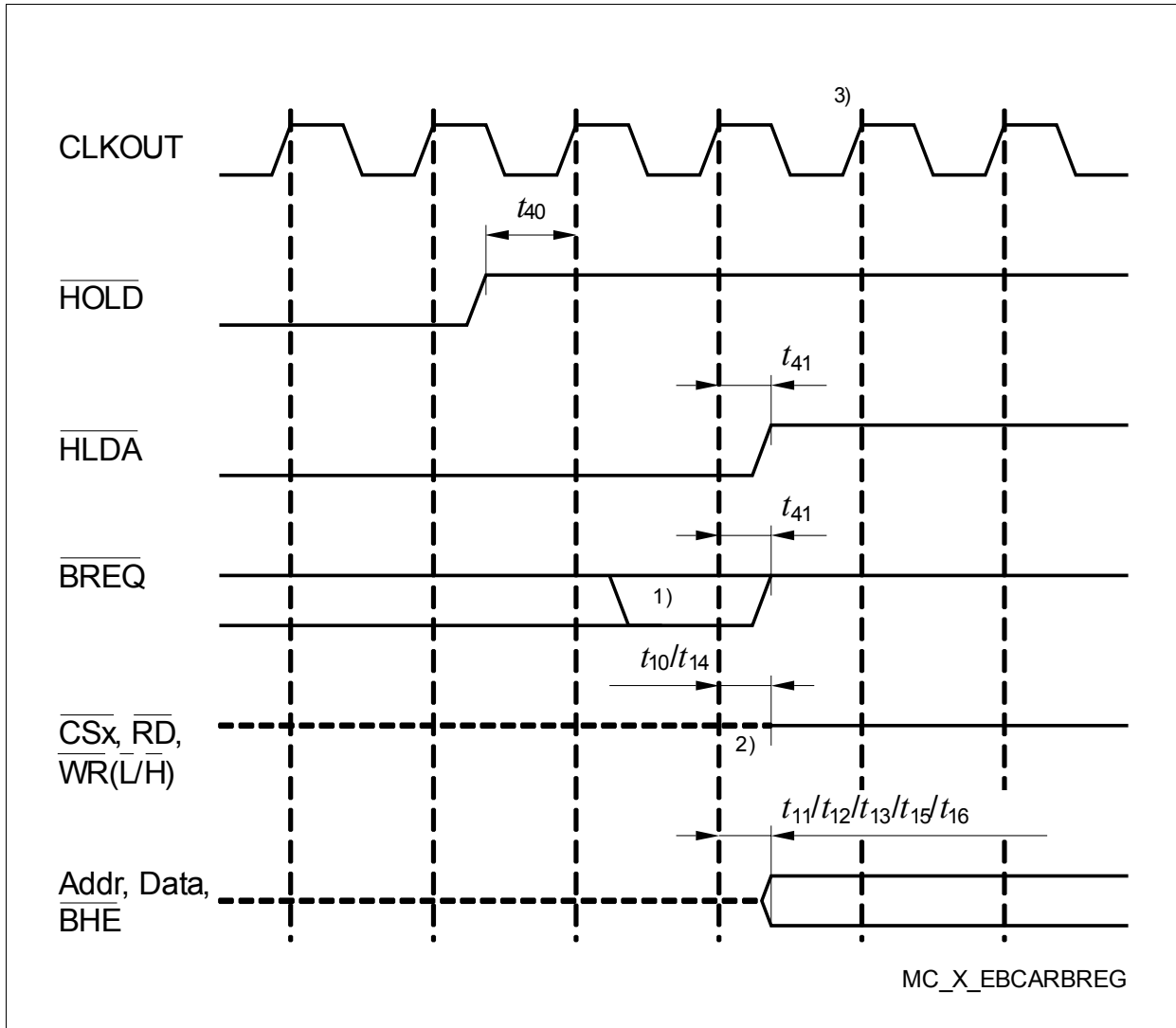


Figure 26 External Bus Arbitration, Regaining the Bus

Notes

1. This is the last chance for $\overline{BREQ}$ to trigger the indicated regain sequence. Even if $\overline{BREQ}$ is activated earlier, the regain sequence is initiated by $\overline{HOLD}$ going high. Please note that $\overline{HOLD}$ may also be deactivated without the XE167 requesting the bus.
2. The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).
3. The next XE167-driven bus cycle may start here.

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