Infineon Technologies - XE167H48F66LACFXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe167h48f66lacfxqma1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P5.8	I	In/A	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/A	**Analog Input Channel 8 for ADC0**
	CCU6x_ T12HRC	I	In/A	**External Run Control Input for T12 of CCU6x**
	CCU6x_ T13HRC	I	In/A	**External Run Control Input for T13 of CCU6x**
44	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
45	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	$\overline{\text{BRKIN\_A}}$	I	In/A	**OCDS Break Signal Input**
46	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
47	P5.12	I	In/A	**Bit 12 of Port 5, General Purpose Input**
	ADC0_CH12	I	In/A	**Analog Input Channel 12 for ADC0**
48	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
	EX0BINB	I	In/A	**External Interrupt Trigger Input**
49	P5.14	I	In/A	**Bit 14 of Port 5, General Purpose Input**
	ADC0_CH14	I	In/A	**Analog Input Channel 14 for ADC0**
50	P5.15	I	In/A	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/A	**Analog Input Channel 15 for ADC0**
51	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_ SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_ SELO3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	READY	I	St/B	**External Bus Interface READY Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P0.3	O0 / I	St/B	**Bit 3 of Port 0, General Purpose Input/Output**
	U1C0_ SELO0	O1	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U1C1_ SELO1	O2	St/B	**USIC1 Channel 1 Select/Control 1 Output**
	CCU61_ COUT60	O3	St/B	**CCU61 Channel 0 Output**
	A3	OH	St/B	**External Bus Interface Address Line 3**
	U1C0_DX2A	I	St/B	**USIC1 Channel 0 Shift Control Input**
	RxDC0B	I	St/B	**CAN Node 0 Receive Data Input**
88	P3.1	O0 / I	St/B	**Bit 1 of Port 3, General Purpose Input/Output**
	U2C0_DOUT	O1	St/B	**USIC2 Channel 0 Shift Data Output**
	TxDC3	O2	St/B	**CAN Node 3 Transmit Data Output**
	HLDA	OH / I	St/B	**External Bus Hold Acknowledge Output/Input** Output in master mode, input in slave mode.
	U2C0_DX0B	I	St/B	**USIC2 Channel 0 Shift Data Input**
89	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_ SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_ CC62	O2 / I	St/B	**CCU60 Channel 2 Input/Output**
	AD2	OH / I	St/B	**External Bus Interface Address/Data Line 2**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
90	P0.4	O0 / I	St/B	**Bit 4 of Port 0, General Purpose Input/Output**
	U1C1_ SELO0	O1	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C0_ SELO1	O2	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	CCU61_ COUT61	O3	St/B	**CCU61 Channel 1 Output**
	A4	OH	St/B	**External Bus Interface Address Line 4**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
92	TRef	IO	Sp/1	**Control Pin for Core Voltage Generation** 2)
93	P3.2	O0 / I	St/B	**Bit 2 of Port 3, General Purpose Input/Output**
	U2C0_ SCLKOUT	O1	St/B	**USIC2 Channel 0 Shift Clock Output**
	TxDC3	O2	St/B	**CAN Node 3 Transmit Data Output**
	U2C0_DX1B	I	St/B	**USIC2 Channel 0 Shift Clock Input**
	HOLD	I	St/B	**External Bus Master Hold Request Input**
94	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_ SELO3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	A23	OH	St/B	**External Bus Interface Address Line 23**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPIN	I	St/B	**GPT2 Register CAPREL Capture Input**
95	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_ COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / I	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
96	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_ SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_ SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_ COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
126	P9.5	O0 / I	St/B	**Bit 5 of Port 9, General Purpose Input/Output**
	CCU63_ COUT62	O1	St/B	**CCU63 Channel 2 Output**
	U2C0_DOUT	O2	St/B	**USIC2 Channel 0 Shift Data Output**
	U2C0_DX0E	I	St/B	**USIC2 Channel 0 Shift Data Input**
	CCU60_ CCPOS2B	I	St/B	**CCU60 Position Input 2**
128	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_ SELO1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	$\overline{RD}$	OH	St/B	**External Bus Interface Read Strobe Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC3C	I	St/B	**CAN Node 3 Receive Data Input**
129	P1.4	O0 / I	St/B	**Bit 4 of Port 1, General Purpose Input/Output**
	CCU62_ COUT61	O1	St/B	**CCU62 Channel 1 Output**
	U1C1_ SELO4	O2	St/B	**USIC1 Channel 1 Select/Control 4 Output**
	U2C0_ SELO5	O3	St/B	**USIC2 Channel 0 Select/Control 5 Output**
	A12	OH	St/B	**External Bus Interface Address Line 12**
	U2C0_DX2B	I	St/B	**USIC2 Channel 0 Shift Control Input**
130	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_ SELO2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	ALE	OH	St/B	**External Bus Interf. Addr. Latch Enable Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**

3.1 Memory Subsystem and Organization

The memory space of the XE167 is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 5 XE167 Memory Map

Address Area	Start Loc.	End Loc.	Area Size[1]	Notes
IMB register space	FF'FF00$_H$	FF'FFFF$_H$	256 Bytes	–
Reserved (Access trap)	F0'0000$_H$	FF'FEFF$_H$	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E9'0000$_H$	EF'FFFF$_H$	448 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000$_H$	E8'FFFF$_H$	64 Kbytes	Flash timing
Reserved for PSRAM	E1'0000$_H$	E7'FFFF$_H$	448 Kbytes	Mirrors PSRAM
Program SRAM	E0'0000$_H$	E0'FFFF$_H$	64 Kbytes	Maximum speed
Reserved for pr. mem.	CC'0000$_H$	DF'FFFF$_H$	<1.25 Mbytes	–
Program Flash 2	C8'0000$_H$	CB'FFFF$_H$	256 Kbytes	–
Program Flash 1	C4'0000$_H$	C7'FFFF$_H$	256 Kbytes	–
Program Flash 0	C0'0000$_H$	C3'FFFF$_H$	256 Kbytes	[2]
External memory area	40'0000$_H$	BF'FFFF$_H$	8 Mbytes	–
Available Ext. IO area[3]	20'5800$_H$	3F'FFFF$_H$	< 2 Mbytes	Minus USIC/CAN
USIC registers	20'4000$_H$	20'57FF$_H$	6 Kbytes	Accessed via EBC
MultiCAN registers	20'0000$_H$	20'3FFF$_H$	16 Kbytes	Accessed via EBC
External memory area	01'0000$_H$	1F'FFFF$_H$	< 2 Mbytes	Minus segment 0
SFR area	00'FE00$_H$	00'FFFF$_H$	0.5 Kbyte	–
Dual-Port RAM	00'F600$_H$	00'FDFF$_H$	2 Kbytes	–
Reserved for DPRAM	00'F200$_H$	00'F5FF$_H$	1 Kbyte	–
ESFR area	00'F000$_H$	00'F1FF$_H$	0.5 Kbyte	–
XSFR area	00'E000$_H$	00'EFFF$_H$	4 Kbytes	–
Data SRAM	00'A000$_H$	00'DFFF$_H$	16 Kbytes	–
Reserved for DSRAM	00'8000$_H$	00'9FFF$_H$	8 Kbytes	–
External memory area	00'0000$_H$	00'7FFF$_H$	32 Kbytes	–

1) The areas marked with "<" are slightly smaller than indicated. See column "Notes".

2) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000$_H$ to C0'FFFF$_H$).

3) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE167 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

3.11 Universal Serial Interface Channel Modules (USIC)

The XE167 includes up to three USIC modules (USIC0, USIC1, USIC2), each providing two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

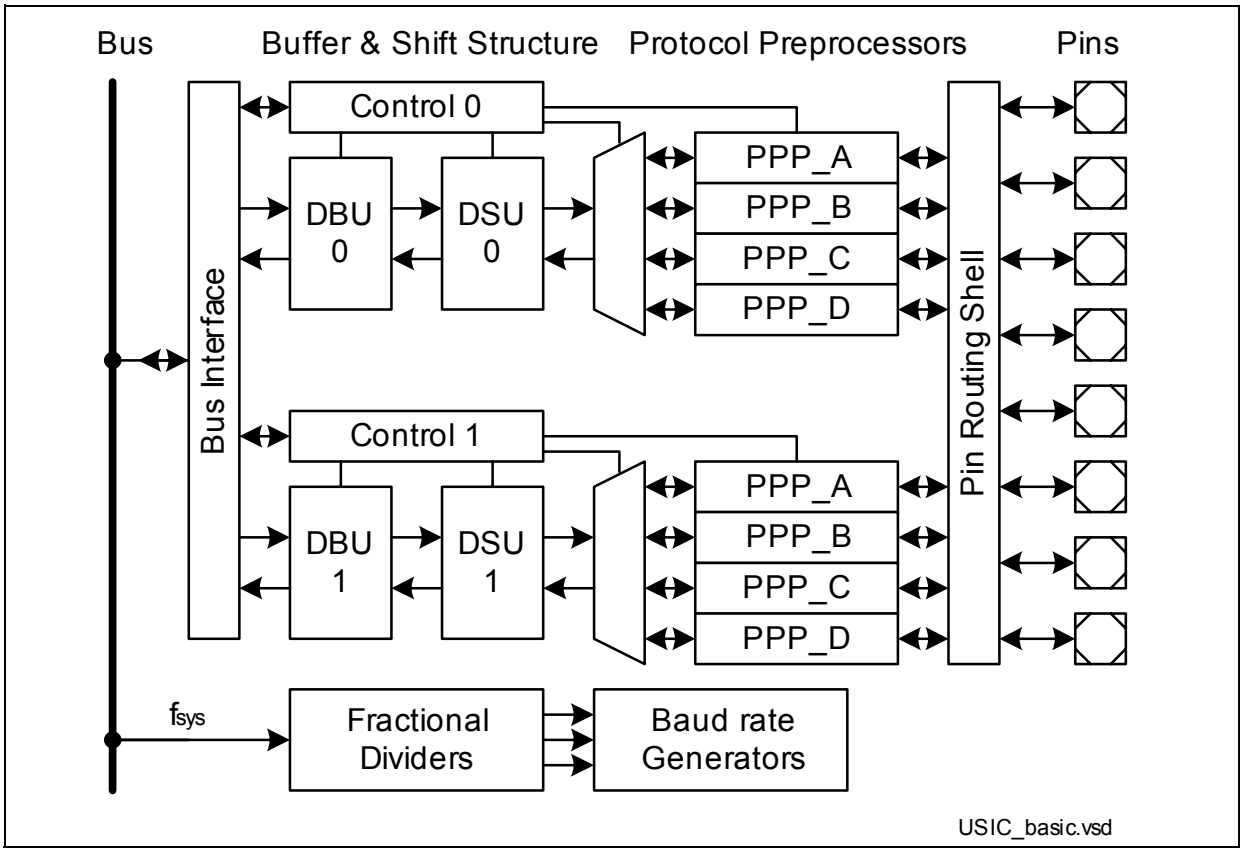

Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to five independent CAN nodes
- 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.16 Instruction Set Summary

Table 10 lists the instructions of the XE167.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 10 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE167, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

Table 12 Operating Condition Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External Pin Load Capacitance	C_L	–	20	–	pF	Pin drivers in **default** mode[6]
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM}	1.0	–	4.7	µF	[7]
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1}	0.47	–	2.2	µF	One for each supply pin[7]
Operating frequency	f_{SYS}	–	–	80	MHz	[8]
Ambient temperature	T_A	–	–	–	°C	See **Table 1**

1) If both core power domains are clocked, the difference between the power supply voltages must be less than 10 mV. This condition imposes additional constraints when using external power supplies.
Do not combine internal and external supply of different core power domains.
Do not supply the core power domains with two independent external voltage regulators. The simplest method is to supply both power domains directly via a single external power supply.

2) Performance of pad drivers, A/D Converter, and Flash module depends on V_{DDP}.
If the external supply voltage V_{DDP} becomes lower than the specified operating range, a power reset must be generated. Otherwise, the core supply voltage V_{DDI} may rise above its specified operating range due to parasitic effects.
This power reset can be generated by the on-chip SWD. If the SWD is disabled the power reset must be generated by activating the $\overline{\text{PORST}}$ input.

3) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application.
Overload conditions must not occur on pin XTAL1 (powered by V_{DDI}).

4) Not subject to production test - verified by design/characterization.

5) An overload current (I_{OV}) through a pin injects an error current (I_{INJ}) into the adjacent pins. This error current adds to that pin's leakage current (I_{OZ}). The value of the error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is reversed from the polarity of the overload current that produces it.
The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

6) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

7) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDI} pin to keep the resistance of the board tracks below 2 Ω. Connect all V_{DDI1} pins together.
The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

8) The operating frequency range may be reduced for specific types of the XE167. This is indicated in the device designation (…FxxL). 80-MHz devices are marked …F80L.

Sample time and conversion time of the XE167's A/D converters are programmable. The timing above can be calculated using **Table 19**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 19 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2	01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63	FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64	FF_H	$t_{ADCI} \times 257$

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time t_S = $t_{ADCI} \times 2$ = 100 ns

Conversion 10-bit:

$t_{C10} = 13 \times t_{ADCI} + 2 \times t_{SYS} = 13 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.675\ \mu s$

Conversion 8-bit:

$t_{C8} = 11 \times t_{ADCI} + 2 \times t_{SYS} = 11 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.575\ \mu s$

Converter Timing Example B:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H
Analog clock f_{ADCI} = f_{SYS} / 3 = 13.3 MHz, i.e. t_{ADCI} = 75 ns
Sample time t_S = $t_{ADCI} \times 5$ = 375 ns

Conversion 10-bit:

$t_{C10} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.25\ \mu s$

Conversion 8-bit:

$t_{C8} = 14 \times t_{ADCI} + 2 \times t_{SYS} = 14 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.10\ \mu s$

4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XE167 into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 20 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply watchdog (SWD) supervision level (see Table 21)	V_{SWD} CC	V_{LV} - 0.150	V_{LV}	V_{LV} + 0.100	V	V_{LV} = selected voltage in upper voltage area
		V_{LV} - 0.125	V_{LV}	V_{LV} + 0.050	V	V_{LV} = selected voltage in lower voltage area
Core voltage (PVC) supervision level (see Table 22)	V_{PVC} CC	V_{LV} - 0.070	V_{LV}	V_{LV} + 0.030	V	V_{LV} = selected voltage
Current control limit	I_{CC} CC	13	–	30	mA	Power domain DMP_M
		90	–	150	mA	Power domain DMP_1
Wakeup clock source frequency	f_{WU} CC	400	500	600	kHz	FREQSEL = 00_B
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Startup time from stopover mode	t_{SSO} CC	200	260	320	µs	User instruction from PSRAM

4.6 AC Parameters

These parameters describe the dynamic behavior of the XE167.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

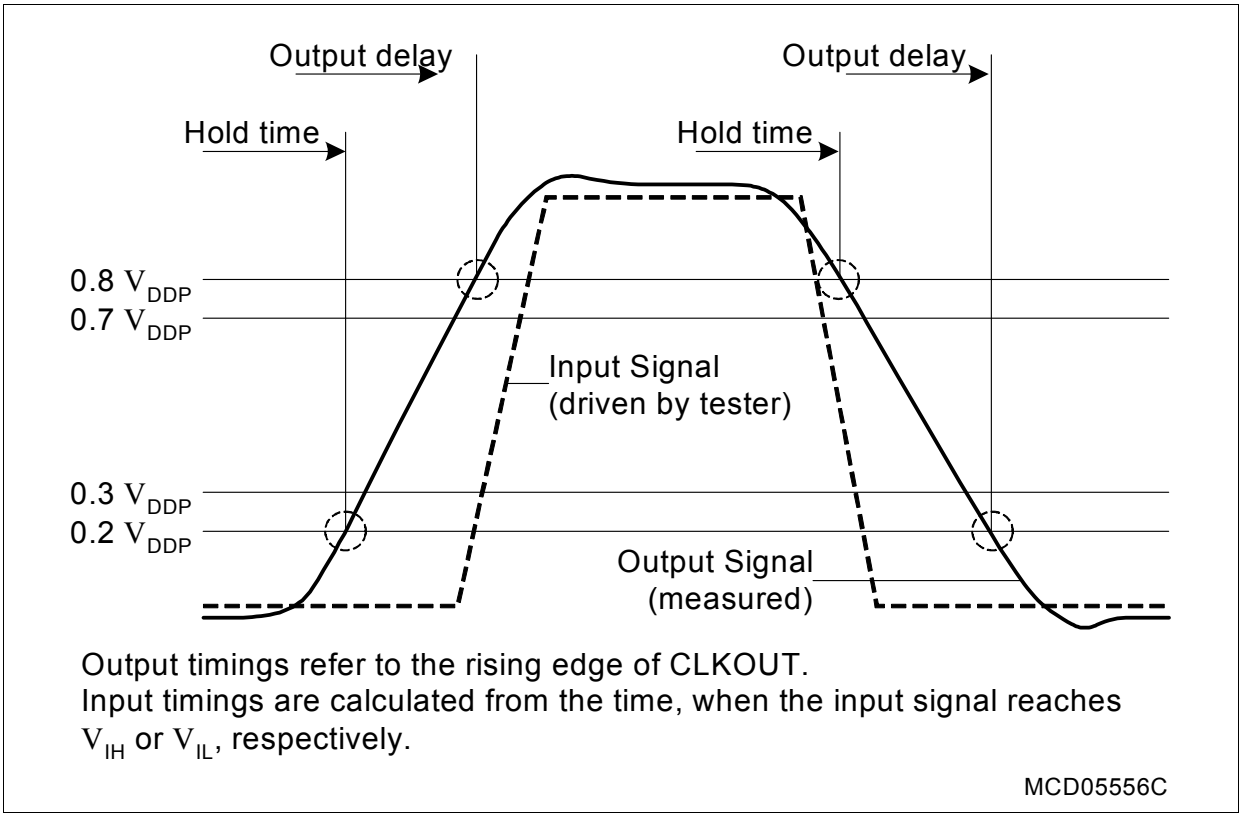

Figure 16 Input Output Waveforms

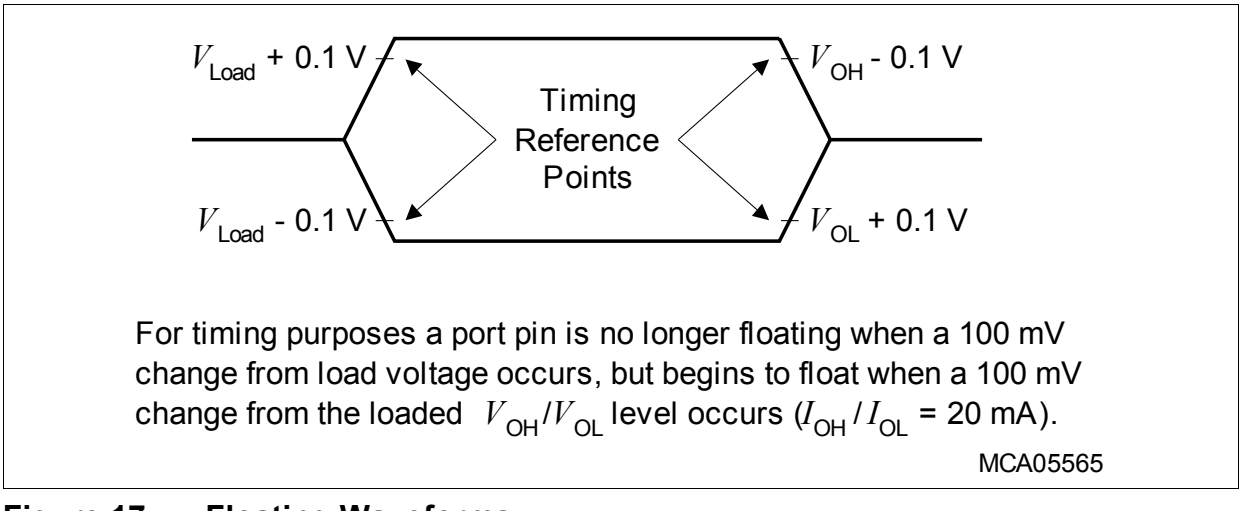

Figure 17 Floating Waveforms

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 19**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

D_{Tmax} [ns] = ±(220 / (K2 × f_{SYS}) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

D_T [ns] = D_{Tmax} × [(1 - 0.058 × K2) × (T - 1) / (0.83 × f_{SYS} - 1) + 0.058 × K2]

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

D_{max} = ±(220 / (4 × 33) + 4.3) = 5.97 ns (Not applicable directly in this case!)

D_3 = 5.97 × [(1 - 0.058 × 4) × (3 - 1) / (0.83 × 33 - 1) + 0.058 × 4]
= 5.97 × [0.768 × 2 / 26.39 + 0.232]
= 1.7 ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

D_{max} = ±(220 / (2 × 33) + 4.3) = 7.63 ns (Not applicable directly in this case!)

D_3 = 7.63 × [(1 - 0.058 × 2) × (3 - 1) / (0.83 × 33 - 1) + 0.058 × 2]
= 7.63 × [0.884 × 2 / 26.39 + 0.116]
= 1.4 ns

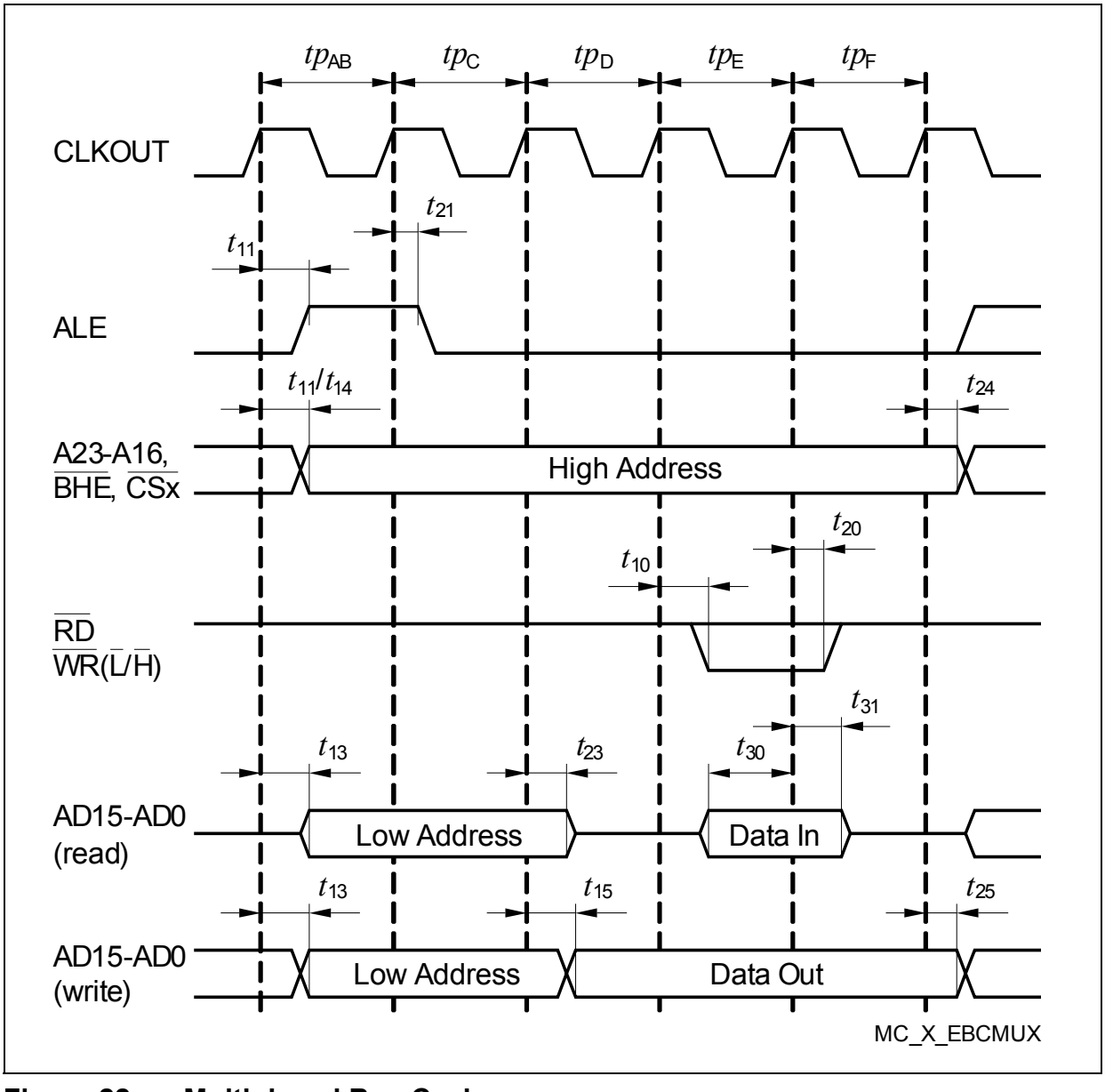

Figure 22 Multiplexed Bus Cycle

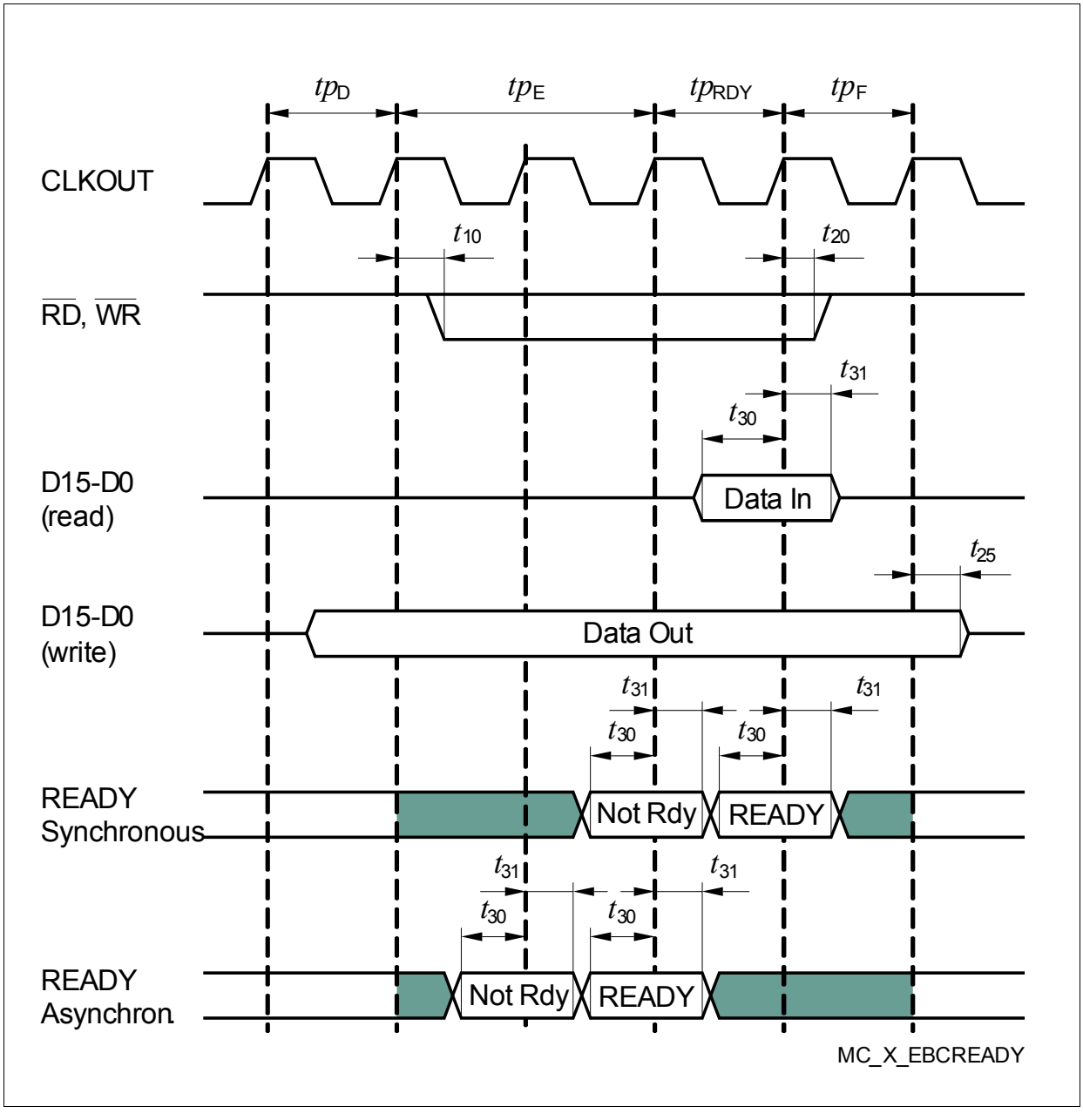

Figure 24 READY Timing

Note: If the READY input is sampled inactive at the indicated sampling point (“Not Rdy”) a READY-controlled waitstate is inserted (tpRDY),
sampling the READY input active at the indicated sampling point (“Ready”) terminates the currently running bus cycle.
Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see tpE) before the READY input value is used.

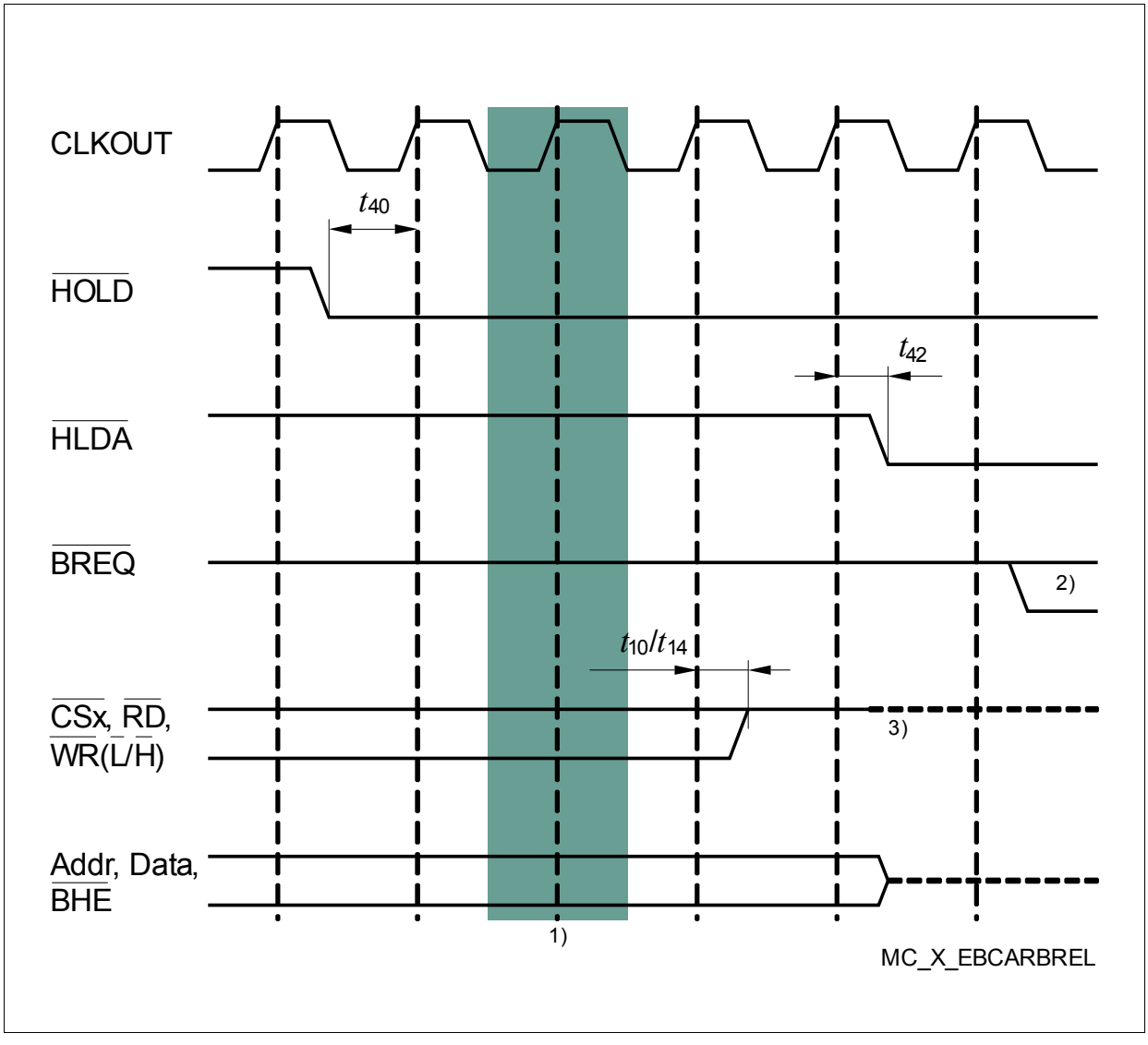

Figure 25 External Bus Arbitration, Releasing the Bus

Notes

1. *The XE167 completes the currently running bus cycle before granting bus access.*
2. *This is the first possibility for BREQ to get active.*
3. *The control outputs will be resistive high (pull-up) after being driven inactive (ALE will be low).*

Table 34 SSC Master/Slave Mode Timing for Lower Voltage Range (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	–	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0.5 × t_{BIT}	–	3)	ns	2)
Transmit data output valid time	t_3 CC	-13	–	16	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	48	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-11	–	–	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	12	–	–	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	8	–	–	ns	7)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	12	–	–	ns	7)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	8	–	–	ns	7)
Data output DOUT valid time	t_{14} CC	11	–	44	ns	7)

1) The maximum value further depends on the settings for the slave select output leading delay.

2) $t_{SYS} = 1/f_{SYS}$ (= 12.5ns @ 80 MHz)

3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).