Infineon Technologies - XE167K48F66LACFXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe167k48f66lacfxqma1

Notes to Pin Definitions

1. ***Ctrl.**: The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bitfield PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.*
   Output signal OH is controlled by hardware.
2. ***Type**: Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).*

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	**Bit 2 of Port 7, General Purpose Input/Output**
	EMUX0	O1	St/B	**External Analog MUX Control Output 0 (ADC1)**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	CCU62_ CCPOS0A	I	St/B	**CCU62 Position Input 0**
	TDI_C	I	St/B	**JTAG Test Data Input**
5	P8.4	O0 / I	St/B	**Bit 4 of Port 8, General Purpose Input/Output**
	CCU60_ COUT61	O1	St/B	**CCU60 Channel 1 Output**
	TMS_D	I	St/B	**JTAG Test Mode Selection Input**
6	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE167's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	**Bit 3 of Port 8, General Purpose Input/Output**
	CCU60_ COUT60	O1	St/B	**CCU60 Channel 0 Output**
	TDI_D	I	St/B	**JTAG Test Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT1 Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT2 Timer T6 Toggle Latch Output**
	TDO_A	OH	St/B	**JTAG Test Data Output**
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
	RxDC4B	I	St/B	**CAN Node 4 Receive Data Input**
9	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_ CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	I	St/B	**JTAG Test Mode Selection Input**
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
10	P8.2	O0 / I	St/B	**Bit 2 of Port 8, General Purpose Input/Output**
	CCU60_ CC62	O1 / I	St/B	**CCU60 Channel 2 Input/Output**
11	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	CCU62_ CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
60	P4.0	O0 / I	St/B	**Bit 0 of Port 4, General Purpose Input/Output**
	CC2_24	O3 / I	St/B	**CAPCOM2 CC24IO Capture Inp./ Compare Out.**
	$\overline{\text{CS0}}$	OH	St/B	**External Bus Interface Chip Select 0 Output**
61	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU63_ COUT63	O2	St/B	**CCU63 Channel 3 Output**
	CC2_16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	A16	OH	St/B	**External Bus Interface Address Line 16**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC0A	I	St/B	**CAN Node 0 Receive Data Input**
62	P11.2	O0 / I	St/B	**Bit 2 of Port 11, General Purpose Input/Output**
	CCU63_ CCPOS2A	I	St/B	**CCU63 Position Input 2**
63	P4.1	O0 / I	St/B	**Bit 1 of Port 4, General Purpose Input/Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_25	O3 / I	St/B	**CAPCOM2 CC25IO Capture Inp./ Compare Out.**
	$\overline{\text{CS1}}$	OH	St/B	**External Bus Interface Chip Select 1 Output**
64	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	A17	OH	St/B	**External Bus Interface Address Line 17**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
65	P11.1	O0 / I	St/B	**Bit 1 of Port 11, General Purpose Input/Output**
	CCU63_ CCPOS1A	I	St/B	**CCU63 Position Input 1**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P0.3	O0 / I	St/B	**Bit 3 of Port 0, General Purpose Input/Output**
	U1C0_ SELO0	O1	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U1C1_ SELO1	O2	St/B	**USIC1 Channel 1 Select/Control 1 Output**
	CCU61_ COUT60	O3	St/B	**CCU61 Channel 0 Output**
	A3	OH	St/B	**External Bus Interface Address Line 3**
	U1C0_DX2A	I	St/B	**USIC1 Channel 0 Shift Control Input**
	RxDC0B	I	St/B	**CAN Node 0 Receive Data Input**
88	P3.1	O0 / I	St/B	**Bit 1 of Port 3, General Purpose Input/Output**
	U2C0_DOUT	O1	St/B	**USIC2 Channel 0 Shift Data Output**
	TxDC3	O2	St/B	**CAN Node 3 Transmit Data Output**
	HLDA	OH / I	St/B	**External Bus Hold Acknowledge Output/Input** Output in master mode, input in slave mode.
	U2C0_DX0B	I	St/B	**USIC2 Channel 0 Shift Data Input**
89	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_ SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_ CC62	O2 / I	St/B	**CCU60 Channel 2 Input/Output**
	AD2	OH / I	St/B	**External Bus Interface Address/Data Line 2**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
90	P0.4	O0 / I	St/B	**Bit 4 of Port 0, General Purpose Input/Output**
	U1C1_ SELO0	O1	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C0_ SELO1	O2	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	CCU61_ COUT61	O3	St/B	**CCU61 Channel 1 Output**
	A4	OH	St/B	**External Bus Interface Address Line 4**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
140	$\overline{\text{ESR2}}$	O0 / I	St/B	**External Service Request 2**
	U1C1_DX0D	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2C	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX0E	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U2C1_DX2B	I	St/B	**USIC2 Channel 1 Shift Control Input**
	EX1AINB	I	St/B	**External Interrupt Trigger Input**
141	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** *Note: After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.*
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
142	P8.6	O0 / I	St/B	**Bit 6 of Port 8, General Purpose Input/Output**
	CCU60_ COUT63	O1	St/B	**CCU60 Channel 3 Output**
	CCU60_ CTRAPB	I	St/B	**CCU60 Emergency Trap Input**
	$\overline{\text{BRKIN\_D}}$	I	St/B	**OCDS Break Signal Input**
143	P8.5	O0 / I	St/B	**Bit 5 of Port 8, General Purpose Input/Output**
	CCU60_ COUT62	O1	St/B	**CCU60 Channel 2 Output**
	TCK_D	I	St/B	**JTAG Clock Input**
15	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see **Table 12** for details.
54, 91, 127	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see **Table 12** for details. All V_{DDI1} pins must be connected to each other.
20	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6, and P15 are fed from supply voltage V_{DDPA}.*

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 36, 38, 72, 74, 108, 110, 144	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6, and P15 are fed from supply voltage V_{DDPB}.*
1, 37, 73, 109	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected to V_{SS}. The respective board area must be connected to ground (if soldered) or left free.*

1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

2) Pin TRef was used to control the core voltage generation in step AA. For that step, pin TRef must be connected to V_{DDPB}.
This connection is no more required from step AB on. For the current step, pin TRef is logically not connected. Future derivatives will feature an additional general purpose IO pin at this position.

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to five external $\overline{CS}$ signals (four windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration; this allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software, after which pins P3.0 … P3.2 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. In Slave Mode pin $\overline{HLDA}$ is switched to be an input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

Table 6 XE167 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
USIC2 Cannel 1, Request 0	U2C1_0IC	xx'017C$_H$	5F$_H$ / 95$_D$
USIC2 Cannel 1, Request 1	U2C1_1IC	xx'0180$_H$	60$_H$ / 96$_D$
USIC2 Cannel 1, Request 2	U2C1_2IC	xx'0184$_H$	61$_H$ / 97$_D$
Unassigned node	–	xx'0188$_H$	62$_H$ / 98$_D$
Unassigned node	–	xx'018C$_H$	63$_H$ / 99$_D$
Unassigned node	–	xx'0190$_H$	64$_H$ / 100$_D$
Unassigned node	–	xx'0194$_H$	65$_H$ / 101$_D$
Unassigned node	–	xx'0198$_H$	66$_H$ / 102$_D$
Unassigned node	–	xx'019C$_H$	67$_H$ / 103$_D$
Unassigned node	–	xx'01A0$_H$	68$_H$ / 104$_D$
Unassigned node	–	xx'01A4$_H$	69$_H$ / 105$_D$
Unassigned node	–	xx'01A8$_H$	6A$_H$ / 106$_D$
SCU Request 1	SCU_1IC	xx'01AC$_H$	6B$_H$ / 107$_D$
SCU Request 0	SCU_0IC	xx'01B0$_H$	6C$_H$ / 108$_D$
Program Flash Modules	PFM_IC	xx'01B4$_H$	6D$_H$ / 109$_D$
RTC	RTC_IC	xx'01B8$_H$	6E$_H$ / 110$_D$
End of PEC Subchannel	EOPIC	xx'01BC$_H$	6F$_H$ / 111$_D$

1) Register VECSEG defines the segment where the vector table is located.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting with a distance of 4 (two words) between two vectors.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

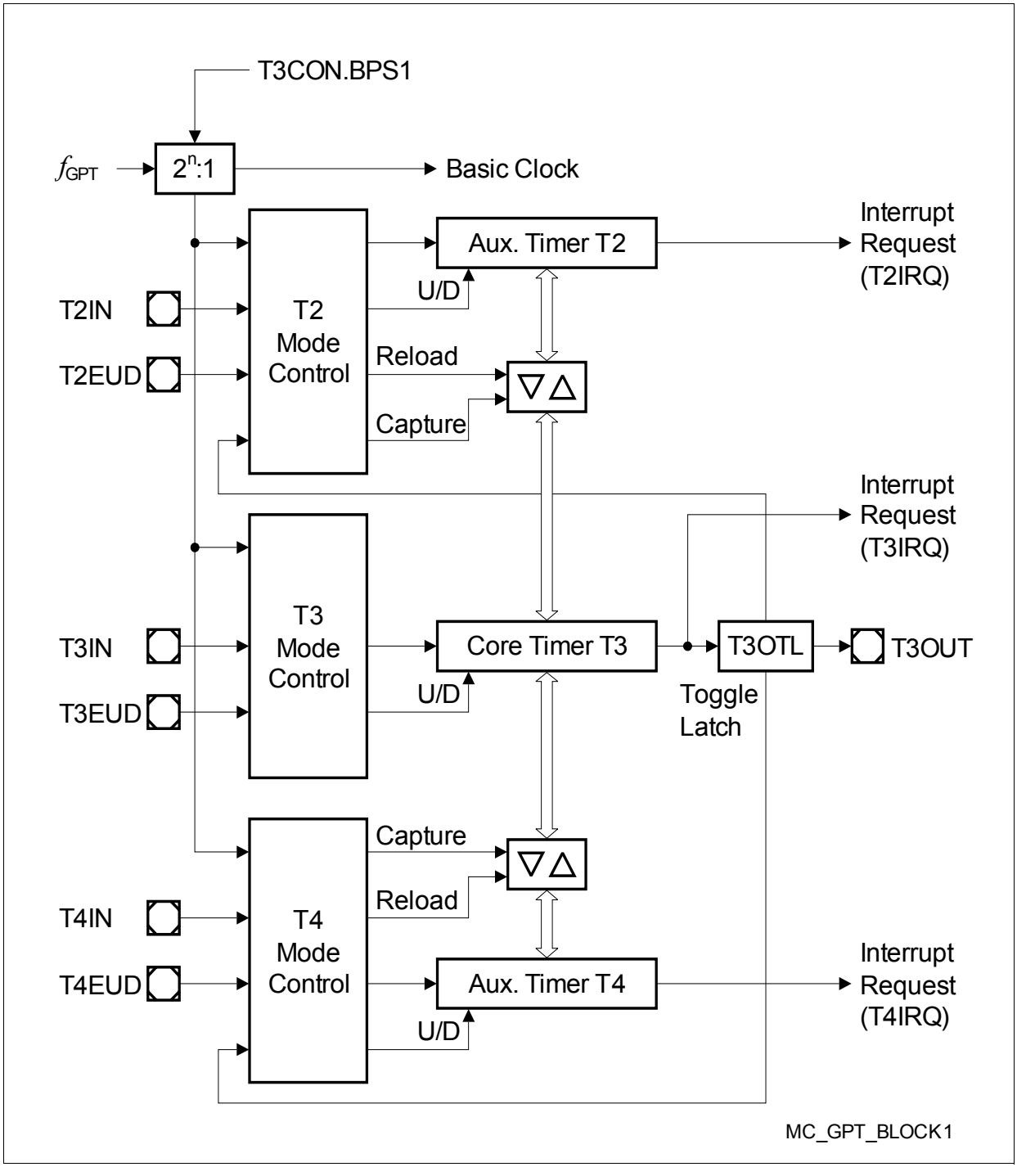

Figure 7 Block Diagram of GPT1

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE167, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

Table 12 Operating Condition Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External Pin Load Capacitance	C_L	–	20	–	pF	Pin drivers in **default** mode[6]
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM}	1.0	–	4.7	µF	[7]
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1}	0.47	–	2.2	µF	One for each supply pin[7]
Operating frequency	f_{SYS}	–	–	80	MHz	[8]
Ambient temperature	T_A	–	–	–	°C	See **Table 1**

1) If both core power domains are clocked, the difference between the power supply voltages must be less than 10 mV. This condition imposes additional constraints when using external power supplies.
Do not combine internal and external supply of different core power domains.
Do not supply the core power domains with two independent external voltage regulators. The simplest method is to supply both power domains directly via a single external power supply.

2) Performance of pad drivers, A/D Converter, and Flash module depends on V_{DDP}.
If the external supply voltage V_{DDP} becomes lower than the specified operating range, a power reset must be generated. Otherwise, the core supply voltage V_{DDI} may rise above its specified operating range due to parasitic effects.
This power reset can be generated by the on-chip SWD. If the SWD is disabled the power reset must be generated by activating the $\overline{\text{PORST}}$ input.

3) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application.
Overload conditions must not occur on pin XTAL1 (powered by V_{DDI}).

4) Not subject to production test - verified by design/characterization.

5) An overload current (I_{OV}) through a pin injects an error current (I_{INJ}) into the adjacent pins. This error current adds to that pin's leakage current (I_{OZ}). The value of the error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is reversed from the polarity of the overload current that produces it.
The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

6) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

7) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDI} pin to keep the resistance of the board tracks below 2 Ω. Connect all V_{DDI1} pins together.
The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

8) The operating frequency range may be reduced for specific types of the XE167. This is indicated in the device designation (…FxxL). 80-MHz devices are marked …F80L.

4.2.2 DC Parameters for Lower Voltage Area

These parameters apply to the lower IO voltage range, 3.0 V ≤ V_{DDP} ≤ 4.5 V.

Table 15 DC Characteristics for Lower Voltage Range (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input Hysteresis[2)]	HYS CC	0.07 × V_{DDP}	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \ge I_{OHmax}$[3)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5, Port 15)[6)]	I_{OZ1} CC	–	±10	±200	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±2.5	µA	$T_J \le$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Pull level keep current	I_{PLK}	–	–	±10	µA	$V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn)
Pull level force current	I_{PLF}	±150	–	–	µA	$V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn)
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

4.2.3 Power Consumption

The power consumed by the XE167 depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S (**Table 16**) and leakage current I_{LK} (**Table 17**) must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
*After a power reset, the decoupling capacitors for V_{DDI} are charged with the maximum possible current, see parameter I_{CC} in **Table 20**.*

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Table 16 Switching Power Consumption XE167 (Operating Conditions apply)

Parameter	Sym-bol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT}	–	10 + 0.6×f_{SYS}	10 + 1.0×f_{SYS}	mA	Active mode[1)2)] f_{SYS} in [MHz]
Power supply current in stopover mode, EVVRs on	I_{SSO}	–	1.0	2.0	mA	Stopover Mode[2)]

1) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers' input stages are switched.

2) The pad supply voltage has only a minor influence on this parameter.

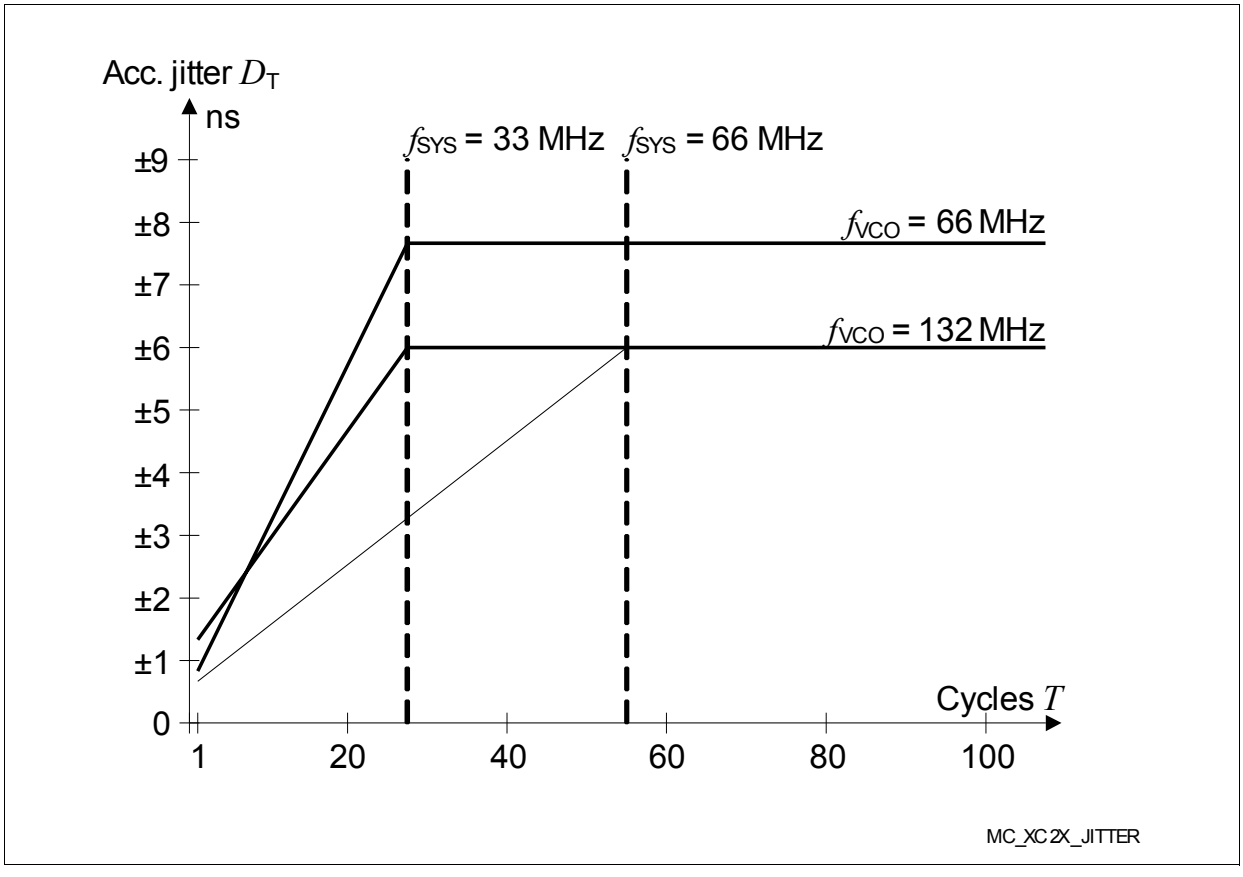

Figure 19 Approximated Accumulated PLL Jitter

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF (see **Table 12**).*
The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100/144 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 25 VCO Bands for PLL Operation[1)]

PLLCON0.VCOSEL	VCO Frequency Range	Base Frequency Range
00	50 … 110 MHz	10 … 40 MHz
01	100 … 160 MHz	20 … 80 MHz
1X	Reserved	

1) Not subject to production test - verified by design/characterization.

4.6.4 External Bus Timing

The following parameters specify the behavior of the XE167 bus interface.

Table 27 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit	Note / Test Condition
			Min.	Max.		
CLKOUT cycle time	t_5	CC	40/25/12.5[1]		ns	
CLKOUT high time	t_6	CC	3	–	ns	
CLKOUT low time	t_7	CC	3	–	ns	
CLKOUT rise time	t_8	CC	–	3	ns	
CLKOUT fall time	t_9	CC	–	3	ns	

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{SYS} = 25/40/80 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

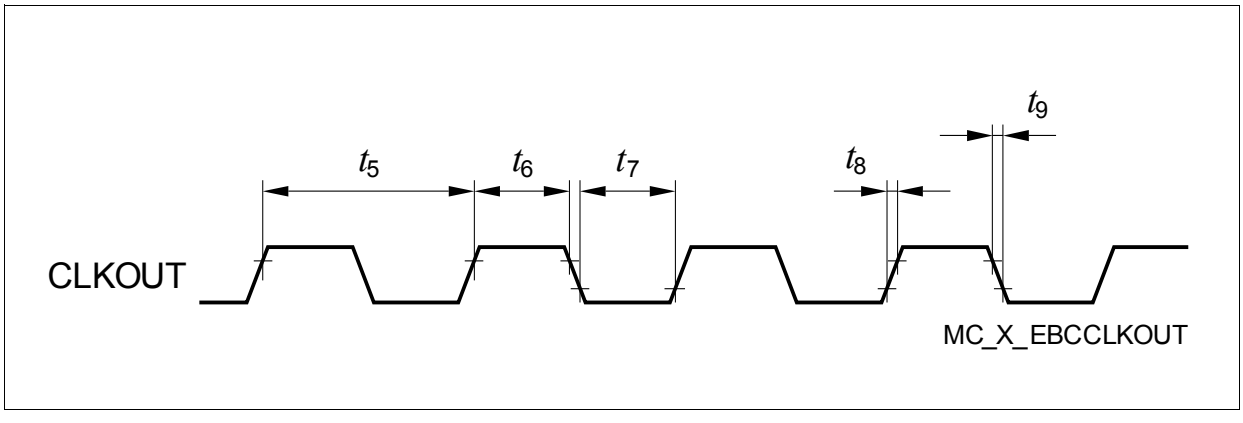

Figure 21 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

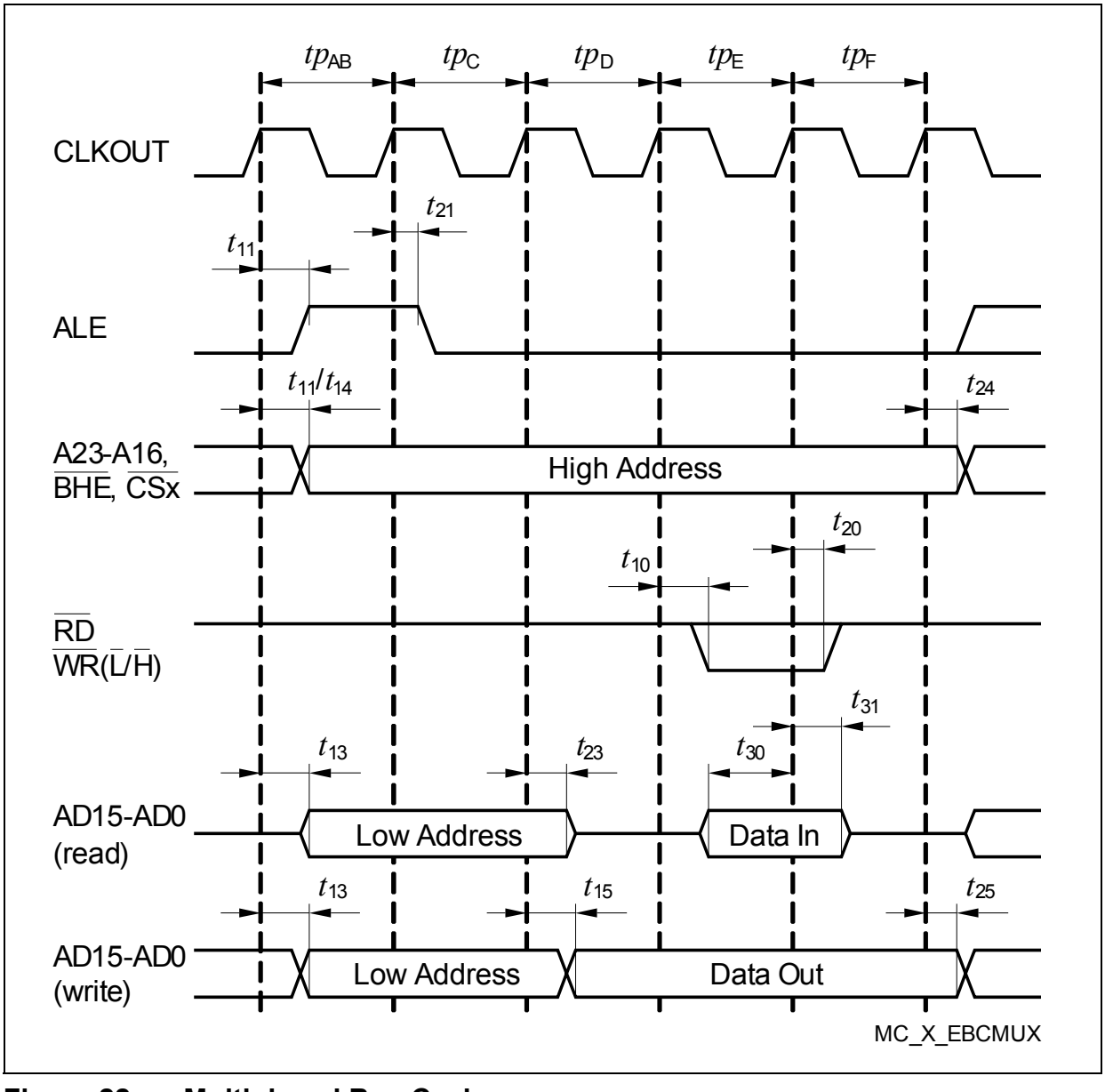

Figure 22 Multiplexed Bus Cycle

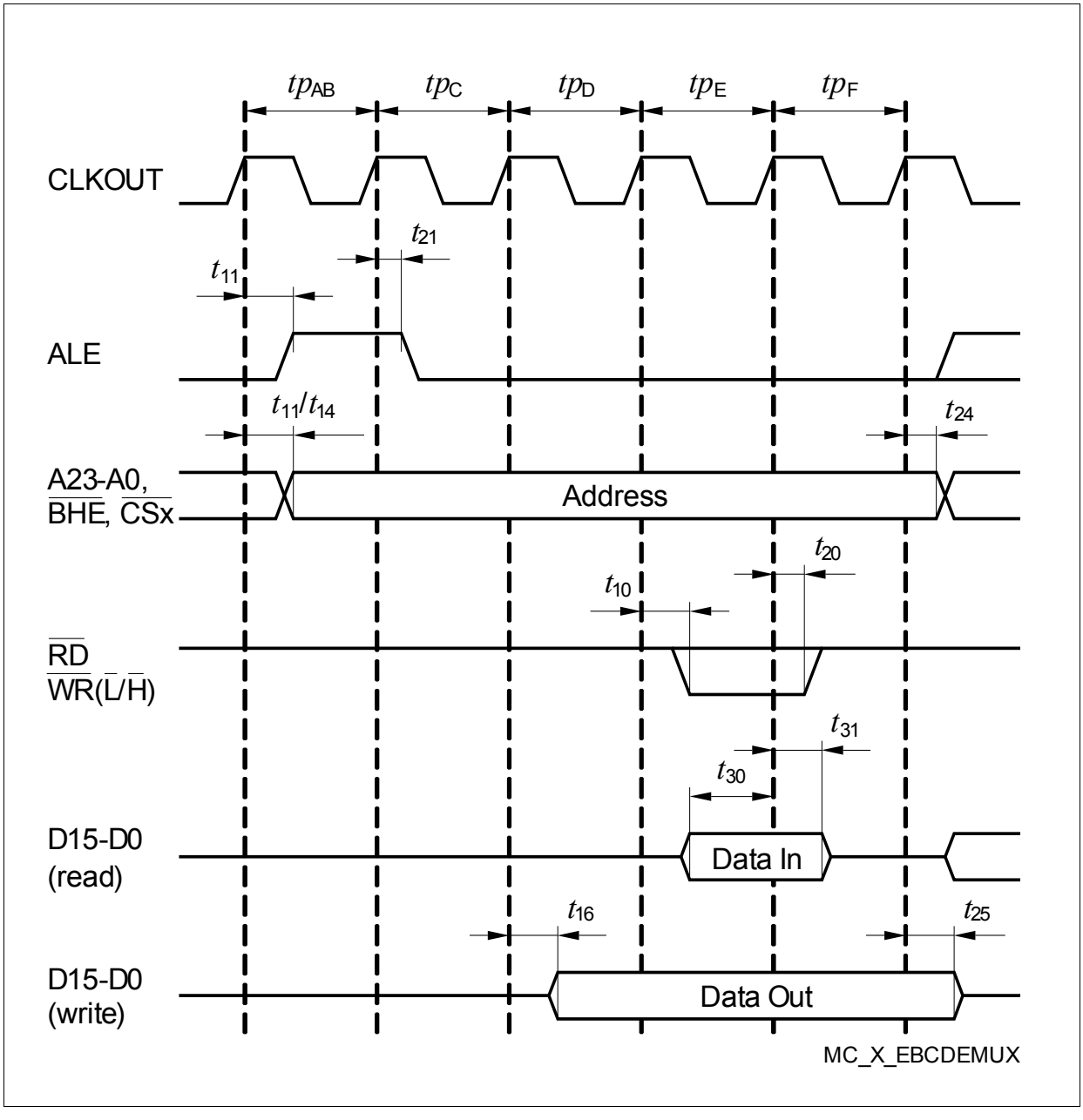

Figure 23 Demultiplexed Bus Cycle

Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.