Infineon Technologies - XE167K72F66LACFXQMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe167k72f66lacfxqma1

  - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 5 CAN nodes and gateway functionality
  - On-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Five programmable chip-select signals
  - Hold- and hold-acknowledge bus arbitration support
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 118 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via JTAG interface
- 144-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For ordering codes for the XE167 please contact your sales representative or local distributor.

This document describes several derivatives of the XE167 group. **Table 1** lists these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity the term **XE167** is used for all derivatives throughout this document.

Table 1 XE167 Derivative Synopsis

Derivative[1]	Temp. Range	Program Memory[2]	PSRAM[3]	CCU6 Mod.	ADC[4] Chan.	Interfaces[4]
SAF-XE167F-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XE167F-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XE167F-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2, 3	16 + 8	5 CAN Nodes, 6 Serial Chan.
SAF-XE167G-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	8 + 8	2 CAN Nodes, 4 Serial Chan.
SAF-XE167G-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	8 + 8	2 CAN Nodes, 4 Serial Chan.
SAF-XE167G-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	8 + 8	2 CAN Nodes, 4 Serial Chan.
SAF-XE167H-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2, 3	16 + 8	No CAN Node, 6 Serial Chan.
SAF-XE167H-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	No CAN Node, 6 Serial Chan.
SAF-XE167H-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2, 3	16 + 8	No CAN Node, 6 Serial Chan.
SAF-XE167K-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	8 + 8	No CAN Node, 4 Serial Chan.
SAF-XE167K-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	8 + 8	No CAN Node, 4 Serial Chan.
SAF-XE167K-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	8 + 8	No CAN Node, 4 Serial Chan.

1) This Data Sheet is valid for devices starting with and including design step AC.

2) Specific inormation about the on-chip Flash memory in **Table 2**.

3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM.

4) Specific information about the available channels in **Table 3**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

2.1 Pin Configuration and Definition

The pins of the XE167 are described in detail in **Table 4**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. **Figure 2** summarizes all pins, showing their locations on the four sides of the package.

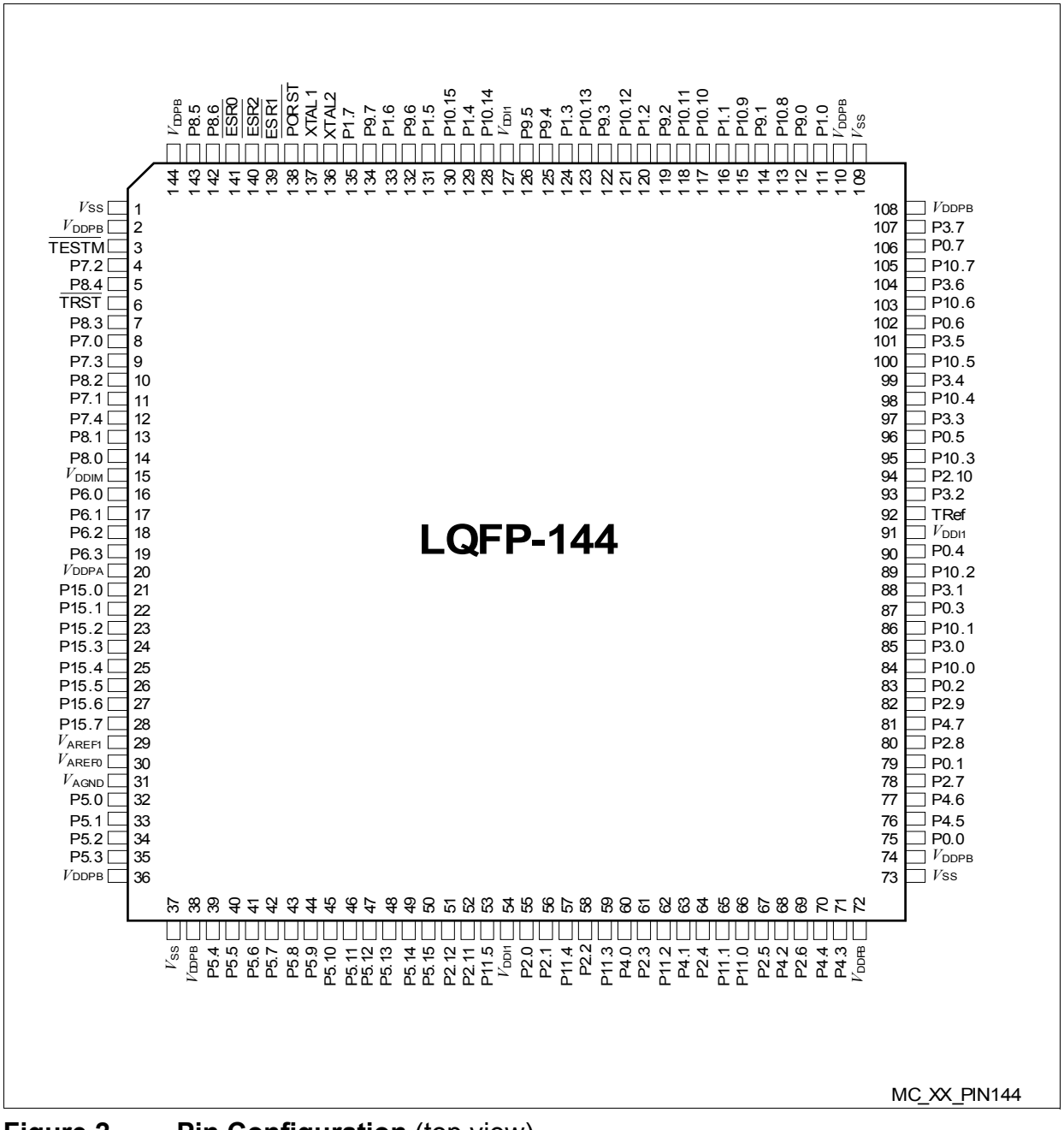

Figure 2 Pin Configuration (top view)

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
18	P6.2	O0 / I	St/A	**Bit 2 of Port 6, General Purpose Input/Output**
	EMUX2	O1	St/A	**External Analog MUX Control Output 2 (ADC0)**
	T6OUT	O2	St/A	**GPT2 Timer T6 Toggle Latch Output**
	U1C1_ SCLKOUT	O3	St/A	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1C	I	St/A	**USIC1 Channel 1 Shift Clock Input**
19	P6.3	O0 / I	St/A	**Bit 3 of Port 6, General Purpose Input/Output**
	T3OUT	O2	St/A	**GPT1 Timer T3 Toggle Latch Output**
	U1C1_ SELO0	O3	St/A	**USIC1 Channel 1 Select/Control 0 Output**
	U1C1_DX2D	I	St/A	**USIC1 Channel 1 Shift Control Input**
	ADCx_ REQTRyD	I	St/A	**External Request Trigger Input for ADC0/1**
21	P15.0	I	In/A	**Bit 0 of Port 15, General Purpose Input**
	ADC1_CH0	I	In/A	**Analog Input Channel 0 for ADC1**
22	P15.1	I	In/A	**Bit 1 of Port 15, General Purpose Input**
	ADC1_CH1	I	In/A	**Analog Input Channel 1 for ADC1**
23	P15.2	I	In/A	**Bit 2 of Port 15, General Purpose Input**
	ADC1_CH2	I	In/A	**Analog Input Channel 2 for ADC1**
	T5IN	I	In/A	**GPT2 Timer T5 Count/Gate Input**
24	P15.3	I	In/A	**Bit 3 of Port 15, General Purpose Input**
	ADC1_CH3	I	In/A	**Analog Input Channel 3 for ADC1**
	T5EUD	I	In/A	**GPT2 Timer T5 External Up/Down Control Input**
25	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6IN	I	In/A	**GPT2 Timer T6 Count/Gate Input**
26	P15.5	I	In/A	**Bit 5 of Port 15, General Purpose Input**
	ADC1_CH5	I	In/A	**Analog Input Channel 5 for ADC1**
	T6EUD	I	In/A	**GPT2 Timer T6 External Up/Down Control Input**
27	P15.6	I	In/A	**Bit 6 of Port 15, General Purpose Input**
	ADC1_CH6	I	In/A	**Analog Input Channel 6 for ADC1**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P5.8	I	In/A	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/A	**Analog Input Channel 8 for ADC0**
	CCU6x_ T12HRC	I	In/A	**External Run Control Input for T12 of CCU6x**
	CCU6x_ T13HRC	I	In/A	**External Run Control Input for T13 of CCU6x**
44	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
45	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	$\overline{\text{BRKIN\_A}}$	I	In/A	**OCDS Break Signal Input**
46	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
47	P5.12	I	In/A	**Bit 12 of Port 5, General Purpose Input**
	ADC0_CH12	I	In/A	**Analog Input Channel 12 for ADC0**
48	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
	EX0BINB	I	In/A	**External Interrupt Trigger Input**
49	P5.14	I	In/A	**Bit 14 of Port 5, General Purpose Input**
	ADC0_CH14	I	In/A	**Analog Input Channel 14 for ADC0**
50	P5.15	I	In/A	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/A	**Analog Input Channel 15 for ADC0**
51	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_ SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_ SELO3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	READY	I	St/B	**External Bus Interface READY Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
126	P9.5	O0 / I	St/B	**Bit 5 of Port 9, General Purpose Input/Output**
	CCU63_ COUT62	O1	St/B	**CCU63 Channel 2 Output**
	U2C0_DOUT	O2	St/B	**USIC2 Channel 0 Shift Data Output**
	U2C0_DX0E	I	St/B	**USIC2 Channel 0 Shift Data Input**
	CCU60_ CCPOS2B	I	St/B	**CCU60 Position Input 2**
128	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_ SELO1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	$\overline{RD}$	OH	St/B	**External Bus Interface Read Strobe Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC3C	I	St/B	**CAN Node 3 Receive Data Input**
129	P1.4	O0 / I	St/B	**Bit 4 of Port 1, General Purpose Input/Output**
	CCU62_ COUT61	O1	St/B	**CCU62 Channel 1 Output**
	U1C1_ SELO4	O2	St/B	**USIC1 Channel 1 Select/Control 4 Output**
	U2C0_ SELO5	O3	St/B	**USIC2 Channel 0 Select/Control 5 Output**
	A12	OH	St/B	**External Bus Interface Address Line 12**
	U2C0_DX2B	I	St/B	**USIC2 Channel 0 Shift Control Input**
130	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_ SELO2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	ALE	OH	St/B	**External Bus Interf. Addr. Latch Enable Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
131	P1.5	O0 / I	St/B	**Bit 5 of Port 1, General Purpose Input/Output**
	CCU62_ COUT60	O1	St/B	**CCU62 Channel 0 Output**
	U1C1_ SELO3	O2	St/B	**USIC1 Channel 1 Select/Control 3 Output**
	$\overline{\text{BRKOUT}}$	O3	St/B	**OCDS Break Signal Output**
	A13	OH	St/B	**External Bus Interface Address Line 13**
	U2C0_DX0C	I	St/B	**USIC2 Channel 0 Shift Data Input**
132	P9.6	O0 / I	St/B	**Bit 6 of Port 9, General Purpose Input/Output**
	CCU63_ COUT63	O1	St/B	**CCU63 Channel 3 Output**
	CCU63_ COUT62	O2	St/B	**CCU63 Channel 2 Output**
	CCU63 _ CTRAPA	I	St/B	**CCU63 Emergency Trap Input**
	CCU60_ CCPOS1B	I	St/B	**CCU60 Position Input 1**
133	P1.6	O0 / I	St/B	**Bit 6 of Port 1, General Purpose Input/Output**
	CCU62_ CC61	O1 / I	St/B	**CCU62 Channel 1 Input/Output**
	U1C1_ SELO2	O2	St/B	**USIC1 Channel 1 Select/Control 2 Output**
	U2C0_DOUT	O3	St/B	**USIC2 Channel 0 Shift Data Output**
	A14	OH	St/B	**External Bus Interface Address Line 14**
	U2C0_DX0D	I	St/B	**USIC2 Channel 0 Shift Data Input**
134	P9.7	O0 / I	St/B	**Bit 7 of Port 9, General Purpose Input/Output**
	CCU63_ CTRAPB	I	St/B	**CCU63 Emergency Trap Input**
	U2C0_DX1D	I	St/B	**USIC2 Channel 0 Shift Clock Input**
	CCU60_ CCPOS0B	I	St/B	**CCU60 Position Input 0**

3 Functional Description

The architecture of the XE167 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE167.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE167.

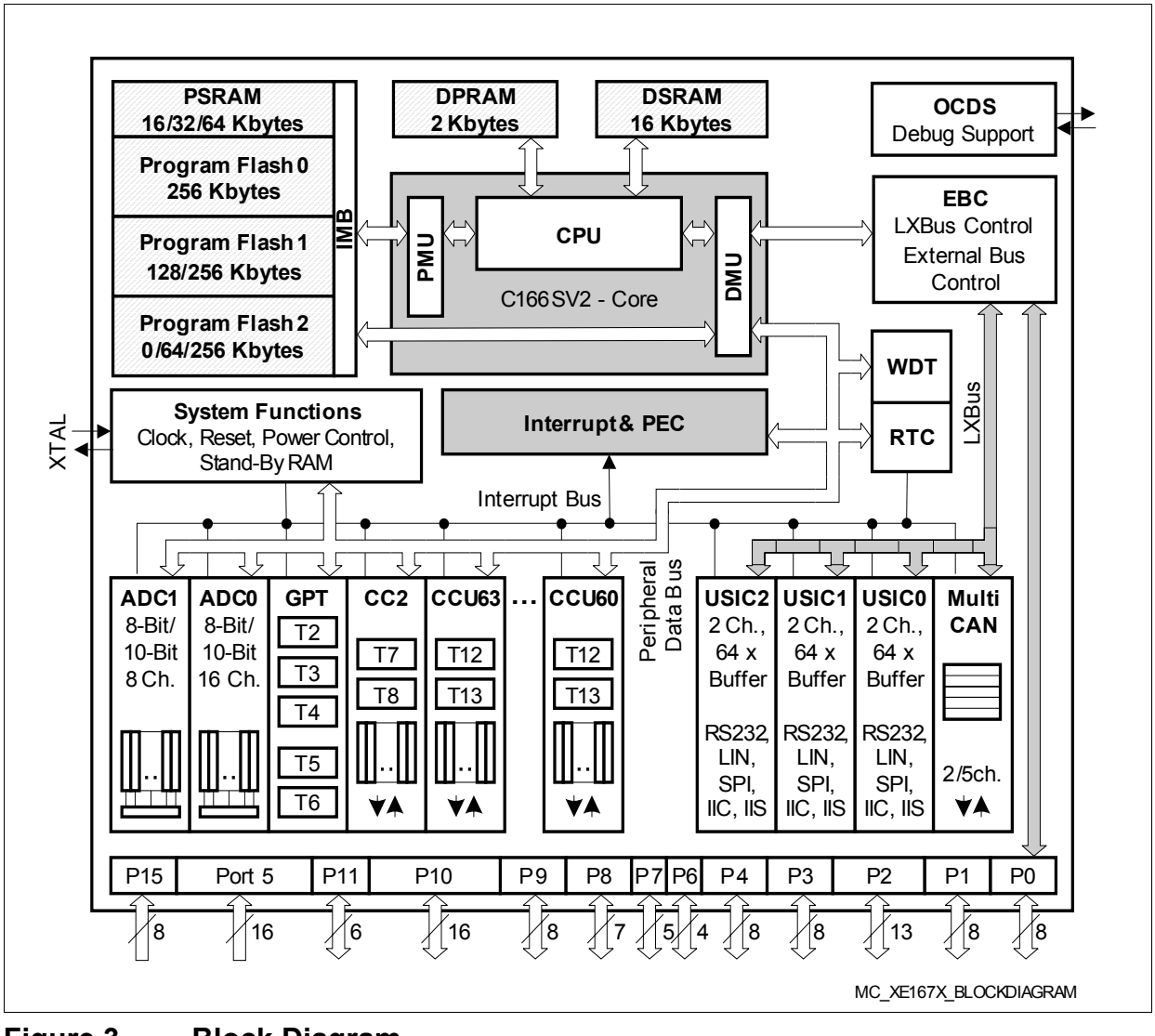

Figure 3 Block Diagram

3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XE167 provides a broad range of debug and emulation features. User software running on the XE167 can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This consists of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the debug interface, or via the external bus interface for increased performance.

The JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

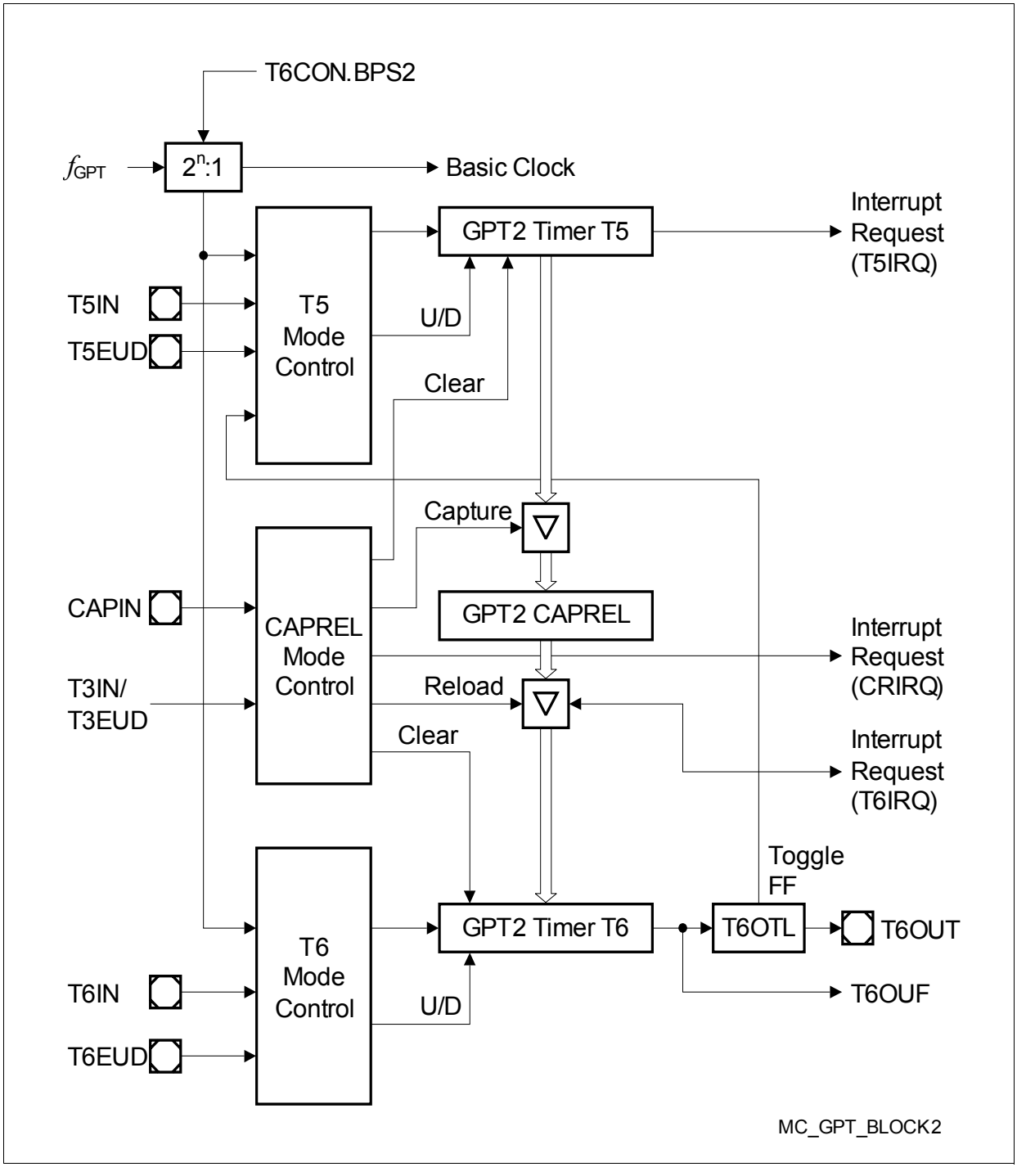

Figure 8 Block Diagram of GPT2

Table 12 Operating Condition Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External Pin Load Capacitance	C_L	–	20	–	pF	Pin drivers in **default** mode[6]
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM}	1.0	–	4.7	µF	[7]
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1}	0.47	–	2.2	µF	One for each supply pin[7]
Operating frequency	f_{SYS}	–	–	80	MHz	[8]
Ambient temperature	T_A	–	–	–	°C	See **Table 1**

1) If both core power domains are clocked, the difference between the power supply voltages must be less than 10 mV. This condition imposes additional constraints when using external power supplies.
Do not combine internal and external supply of different core power domains.
Do not supply the core power domains with two independent external voltage regulators. The simplest method is to supply both power domains directly via a single external power supply.

2) Performance of pad drivers, A/D Converter, and Flash module depends on V_{DDP}.
If the external supply voltage V_{DDP} becomes lower than the specified operating range, a power reset must be generated. Otherwise, the core supply voltage V_{DDI} may rise above its specified operating range due to parasitic effects.
This power reset can be generated by the on-chip SWD. If the SWD is disabled the power reset must be generated by activating the $\overline{\text{PORST}}$ input.

3) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application.
Overload conditions must not occur on pin XTAL1 (powered by V_{DDI}).

4) Not subject to production test - verified by design/characterization.

5) An overload current (I_{OV}) through a pin injects an error current (I_{INJ}) into the adjacent pins. This error current adds to that pin's leakage current (I_{OZ}). The value of the error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is reversed from the polarity of the overload current that produces it.
The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

6) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

7) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDI} pin to keep the resistance of the board tracks below 2 Ω. Connect all V_{DDI1} pins together.
The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

8) The operating frequency range may be reduced for specific types of the XE167. This is indicated in the device designation (…FxxL). 80-MHz devices are marked …F80L.

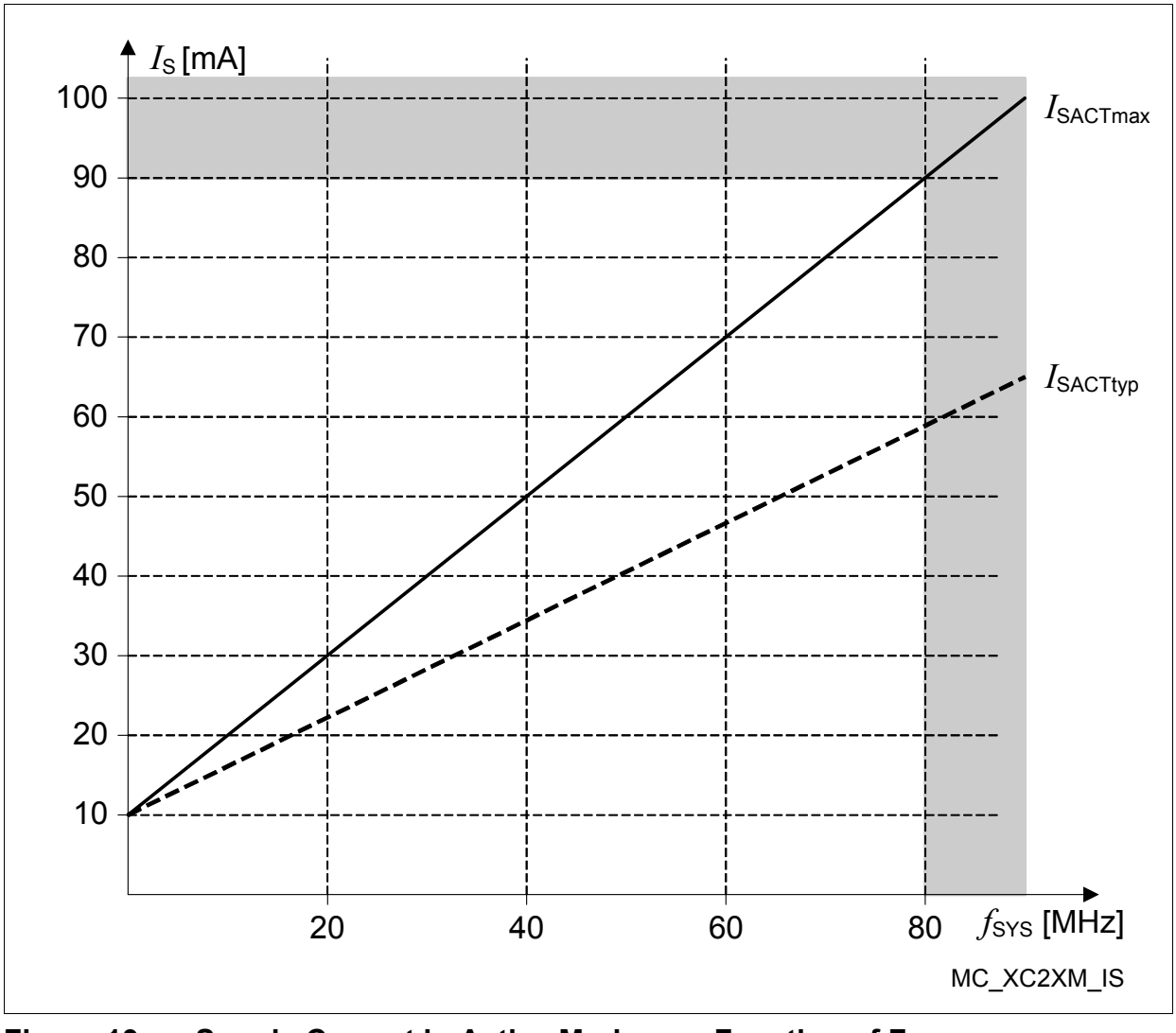

Figure 13 Supply Current in Active Mode as a Function of Frequency

4.5 Flash Memory Parameters

The XE167 is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE167's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 23 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Programming time per 128-byte page	t_{PR}	–	3[1)]	3.5	ms	ms
Erase time per sector/page	t_{ER}	–	4[1)]	5	ms	ms
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles
Flash erase endurance for user sectors[2)]	N_{ER}	15,000	–	–	cycles	Data retention time 5 years
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	Data retention time 20 years
Drain disturb limit	N_{DD}	64	–	–	cycles	[3)]

1) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.
In the XE167 erased areas must be programmed completely (with actual code/data or dummy values) before that area is read.

2) A maximum of 64 Flash sectors can be cycled 15,000 times. For all other sectors the limit is 1,000 cycles.

3) This parameter limits the number of subsequent programming operations within a physical sector. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated.

Access to the XE167 Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.6 AC Parameters

These parameters describe the dynamic behavior of the XE167.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

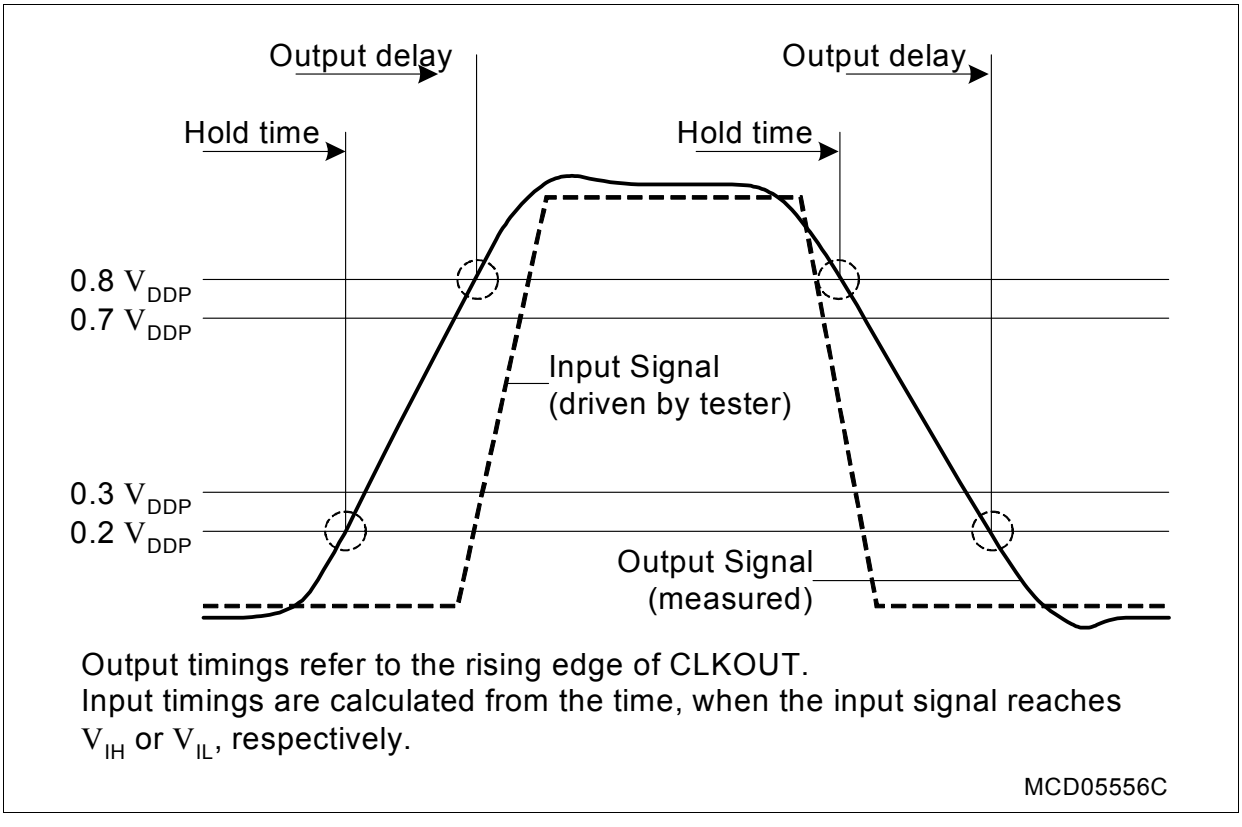

Figure 16 Input Output Waveforms

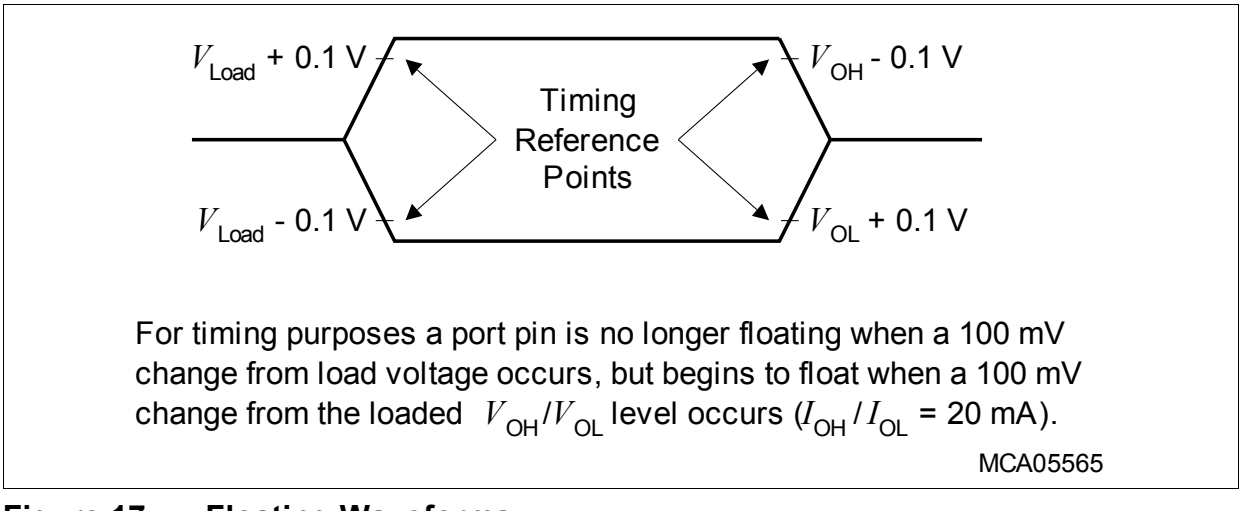

Figure 17 Floating Waveforms

External Bus Arbitration

If the arbitration signals are enabled, the XE167 makes its external resources available in response to an arbitration request.

Table 31 Bus Arbitration Timing for Upper Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Input setup time for: HOLD input	t_{40} SR	18		–	ns	
Output delay rising edge for: HLDA, BREQ	t_{41} CC	0		13	ns	
Output delay falling edge for: HLDA	t_{42} CC	1		14	ns	

Table 32 Bus Arbitration Timing for Lower Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Input setup time for: HOLD input	t_{40} SR	28		–	ns	
Output delay rising edge for: HLDA, BREQ	t_{41} CC	0		19	ns	
Output delay falling edge for: HLDA	t_{42} CC	1		21	ns	

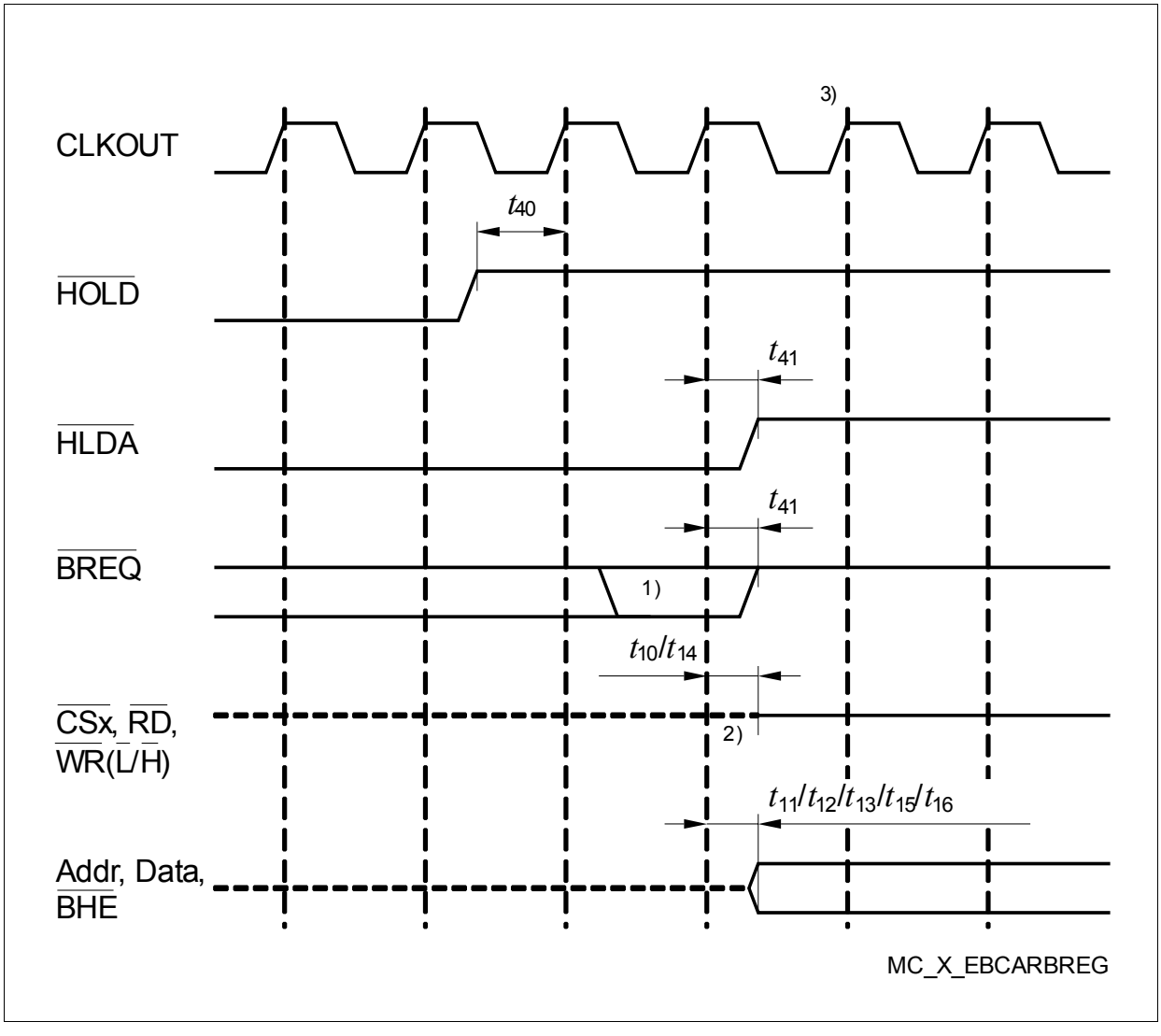

Figure 26 External Bus Arbitration, Regaining the Bus

Notes

1. *This is the last chance for BREQ to trigger the indicated regain sequence. Even if BREQ is activated earlier, the regain sequence is initiated by HOLD going high. Please note that HOLD may also be deactivated without the XE167 requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XE167-driven bus cycle may start here.*

4.6.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 33 SSC Master/Slave Mode Timing for Upper Voltage Range (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	–	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0.5 × t_{BIT}	–	3)	ns	
Transmit data output valid time	t_3 CC	-6	–	13	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-7	–	–	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	7	–	–	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	5	–	–	ns	7)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	7	–	–	ns	7)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	5	–	–	ns	7)
Data output DOUT valid time	t_{14} CC	8	–	29	ns	7)

1) The maximum value further depends on the settings for the slave select output leading delay.

2) $t_{SYS} = 1/f_{SYS}$ (= 12.5 ns @ 80 MHz)

3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

4.6.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 35 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	60	50	–	ns	–
TCK high time	t_2 SR	16	–	–	ns	–
TCK low time	t_3 SR	16	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	8	ns	–
TCK clock fall time	t_5 SR	–	–	8	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1]	t_8 CC	–	–	30	ns	C_L = 50 pF
	t_8 CC	10	–	–	ns	C_L = 20 pF
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	30	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1)]	t_{10} CC	–	–	30	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

Package Outlines

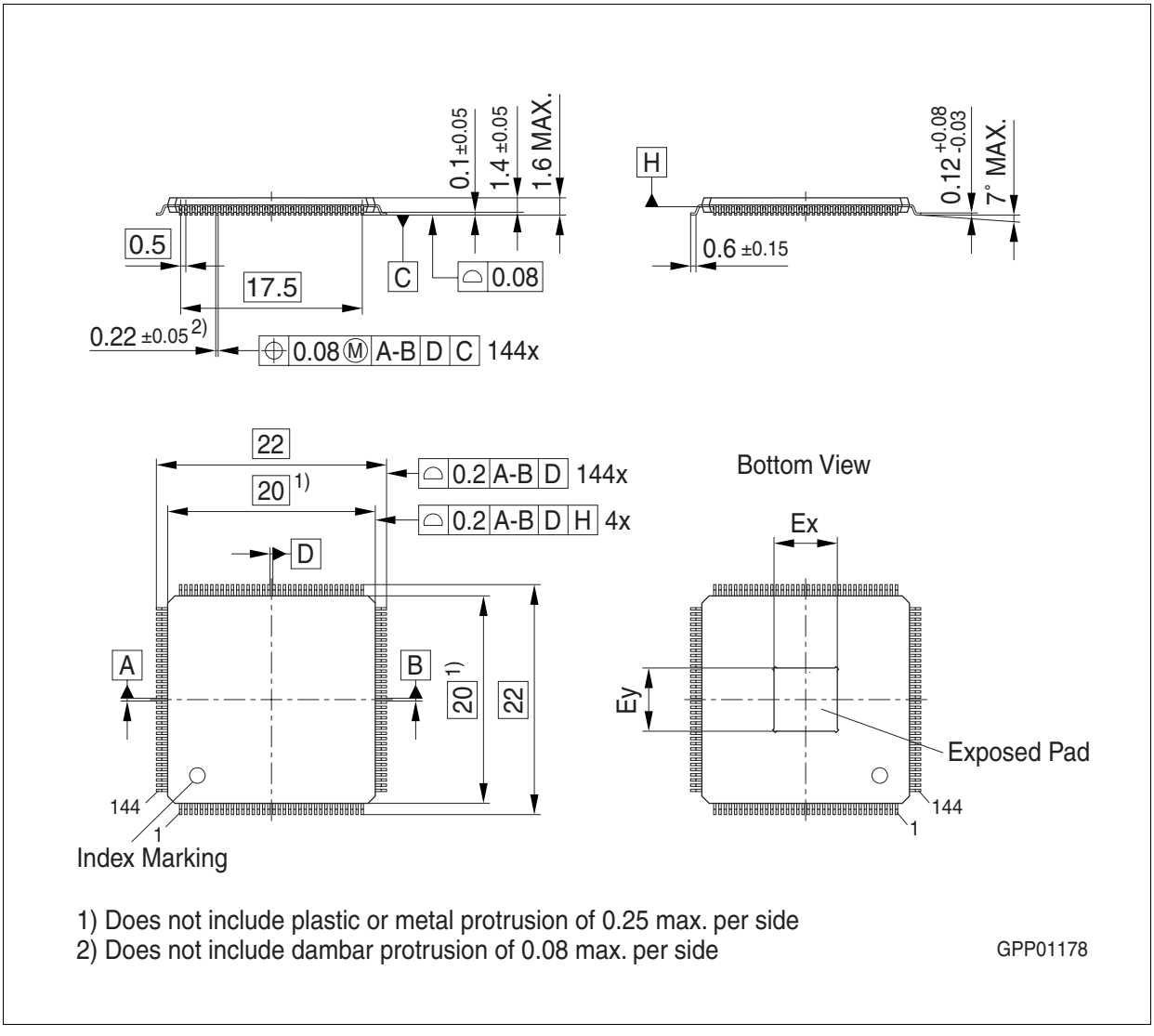

Figure 30 PG-LQFP-144-4 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**