Infineon Technologies - XE167K96F66LACFXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	66MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe167k96f66lacfxqma1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT1 Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT2 Timer T6 Toggle Latch Output**
	TDO_A	OH	St/B	**JTAG Test Data Output**
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
	RxDC4B	I	St/B	**CAN Node 4 Receive Data Input**
9	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_ CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	I	St/B	**JTAG Test Mode Selection Input**
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
10	P8.2	O0 / I	St/B	**Bit 2 of Port 8, General Purpose Input/Output**
	CCU60_ CC62	O1 / I	St/B	**CCU60 Channel 2 Input/Output**
11	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	CCU62_ CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
52	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_ SELO2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_ SELO2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	$\overline{BHE}$/$\overline{WRH}$	OH	St/B	**External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{BHE}$) or as Write strobe for High Byte ($\overline{WRH}$).
53	P11.5	O0 / I	St/B	**Bit 5 of Port 11, General Purpose Input/Output**
55	P2.0	O0 / I	St/B	**Bit 0 of Port 2, General Purpose Input/Output**
	CCU63_ CC60	O2 / I	St/B	**CCU63 Channel 0 Input/Output**
	AD13	OH / I	St/B	**External Bus Interface Address/Data Line 13**
	RxDC0C	I	St/B	**CAN Node 0 Receive Data Input**
56	P2.1	O0 / I	St/B	**Bit 1 of Port 2, General Purpose Input/Output**
	TxDC0	O1	St/B	**CAN Node 0 Transmit Data Output**
	CCU63_ CC61	O2 / I	St/B	**CCU63 Channel 1 Input/Output**
	AD14	OH / I	St/B	**External Bus Interface Address/Data Line 14**
	ESR1_5	I	St/B	**ESR1 Trigger Input 5**
	EX0AINA	I	St/B	**External Interrupt Trigger Input**
57	P11.4	O0 / I	St/B	**Bit 4 of Port 11, General Purpose Input/Output**
58	P2.2	O0 / I	St/B	**Bit 2 of Port 2, General Purpose Input/Output**
	TxDC1	O1	St/B	**CAN Node 1 Transmit Data Output**
	CCU63_ CC62	O2 / I	St/B	**CCU63 Channel 2 Input/Output**
	AD15	OH / I	St/B	**External Bus Interface Address/Data Line 15**
	ESR2_5	I	St/B	**ESR2 Trigger Input 5**
	EX1AINA	I	St/B	**External Interrupt Trigger Input**
59	P11.3	O0 / I	St/B	**Bit 3 of Port 11, General Purpose Input/Output**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
71	P4.3	O0 / I	St/B	**Bit 3 of Port 4, General Purpose Input/Output**
	CC2_27	O3 / I	St/B	**CAPCOM2 CC27IO Capture Inp./ Compare Out.**
	$\overline{CS3}$	OH	St/B	**External Bus Interface Chip Select 3 Output**
	RxDC2A	I	St/B	**CAN Node 2 Receive Data Input**
	T2EUD	I	St/B	**GPT1 Timer T2 External Up/Down Control Input**
75	P0.0	O0 / I	St/B	**Bit 0 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	CCU61_ CC60	O3 / I	St/B	**CCU61 Channel 0 Input/Output**
	A0	OH	St/B	**External Bus Interface Address Line 0**
	U1C0_DX0A	I	St/B	**USIC1 Channel 0 Shift Data Input**
76	P4.5	O0 / I	St/B	**Bit 5 of Port 4, General Purpose Input/Output**
	CC2_29	O3 / I	St/B	**CAPCOM2 CC29IO Capture Inp./Compare Out.**
77	P4.6	O0 / I	St/B	**Bit 6 of Port 4, General Purpose Input/Output**
	CC2_30	O3 / I	St/B	**CAPCOM2 CC30IO Capture Inp./ Compare Out.**
	T4IN	I	St/B	**GPT1 Timer T4 Count/Gate Input**
78	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_ SELO0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_ SELO1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	A20	OH	St/B	**External Bus Interface Address Line 20**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P0.1	O0 / I	St/B	**Bit 1 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_ CC61	O3 / I	St/B	**CCU61 Channel 1 Input/Output**
	A1	OH	St/B	**External Bus Interface Address Line 1**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
80	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_ SCLKOUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output** 1)
	CC2_21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	A21	OH	DP/B	**External Bus Interface Address Line 21**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**
81	P4.7	O0 / I	St/B	**Bit 7 of Port 4, General Purpose Input/Output**
	CC2_31	O3 / I	St/B	**CAPCOM2 CC31IO Capture Inp./ Compare Out.**
	T4EUD	I	St/B	**GPT1 Timer T4 External Up/Down Control Input**
82	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	A22	OH	St/B	**External Bus Interface Address Line 22**
	CLKIN1	I	St/B	**Clock Signal Input**
	TCK_A	I	St/B	**JTAG Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
111	P1.0	O0 / I	St/B	**Bit 0 of Port 1, General Purpose Input/Output**
	U1C0_ MCLKOUT	O1	St/B	**USIC1 Channel 0 Master Clock Output**
	U1C0_ SELO4	O2	St/B	**USIC1 Channel 0 Select/Control 4 Output**
	A8	OH	St/B	**External Bus Interface Address Line 8**
	ESR1_3	I	St/B	**ESR1 Trigger Input 3**
	EX0BINA	I	St/B	**External Interrupt Trigger Input**
	CCU62_ CTRAPB	I	St/B	**CCU62 Emergency Trap Input**
112	P9.0	O0 / I	St/B	**Bit 0 of Port 9, General Purpose Input/Output**
	CCU63_ CC60	O1 / I	St/B	**CCU63 Channel 0 Input/Output**
113	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_ MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_ SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	AD8	OH / I	St/B	**External Bus Interface Address/Data Line 8**
	CCU60_ CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
114	P9.1	O0 / I	St/B	**Bit 1 of Port 9, General Purpose Input/Output**
	CCU63_ CC61	O1 / I	St/B	**CCU63 Channel 1 Input/Output**

The XE167 includes an excellent mechanism to identify and process exceptions or error conditions that arise during run-time, the so-called ‘Hardware Traps’. A hardware trap causes an immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 7 shows all possible exceptions or error conditions that can arise during runtime:

Table 7 Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions	–	RESET	xx’0000$_H$	00$_H$	III
Class A Hardware Traps:					
• System Request 0	SR0	SR0TRAP	xx’0008$_H$	02$_H$	II
• Stack Overflow	STKOF	STOTRAP	xx’0010$_H$	04$_H$	II
• Stack Underflow	STKUF	STUTRAP	xx’0018$_H$	06$_H$	II
• Software Break	SOFTBRK	SBRKTRAP	xx’0020$_H$	08$_H$	II
Class B Hardware Traps:					
• System Request 1	SR1	BTRAP	xx’0028$_H$	0A$_H$	I
• Undefined Opcode	UNDOPC	BTRAP	xx’0028$_H$	0A$_H$	I
• Memory Access Error	ACER	BTRAP	xx’0028$_H$	0A$_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx’0028$_H$	0A$_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx’0028$_H$	0A$_H$	I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps: • TRAP Instruction	–	–	Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

3.7 Capture/Compare Units CCU6x

The XE167 features up to four CCU6 units (CCU60, CCU61, CCU62, CCU63).

The CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

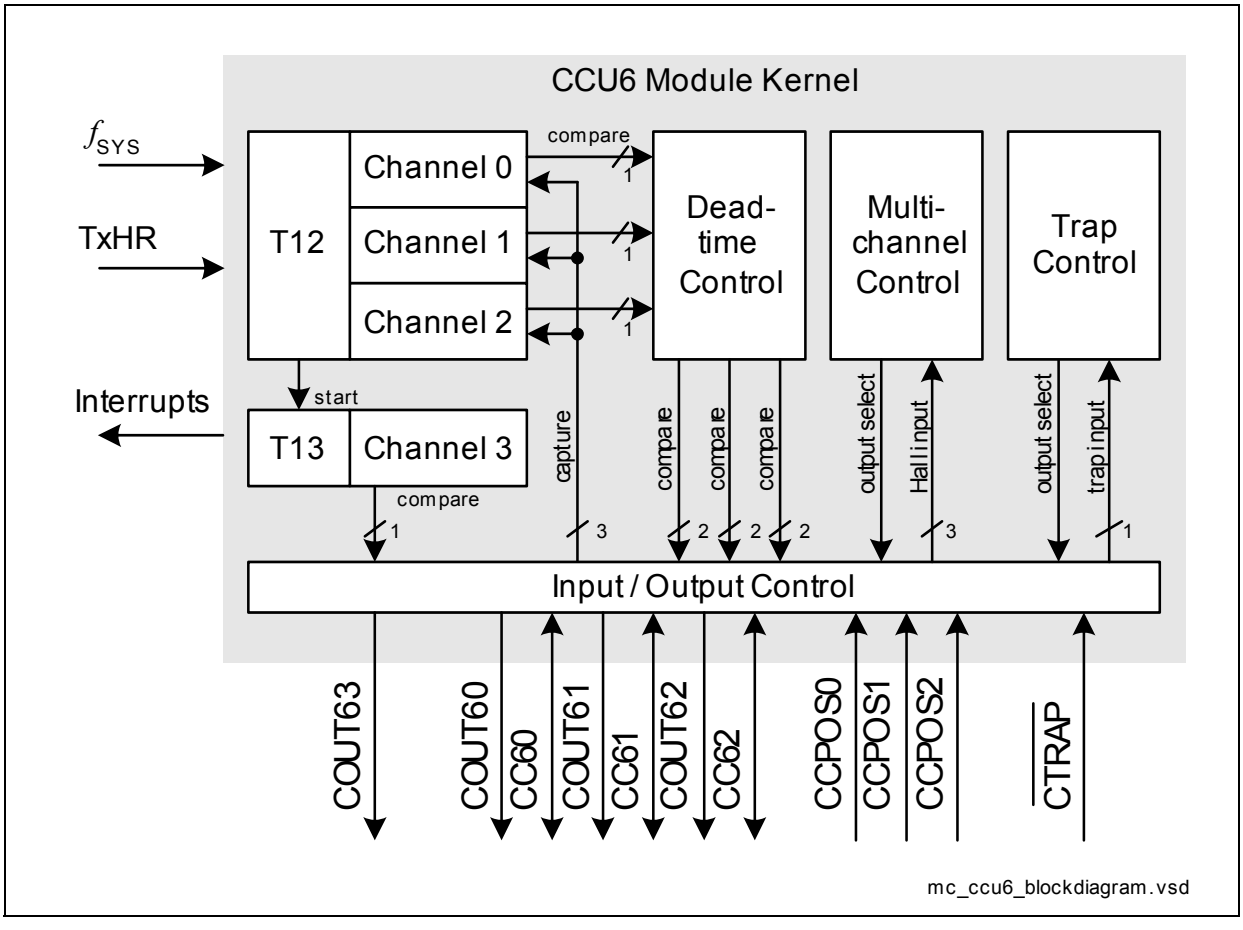

Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

3.9 Real Time Clock

The Real Time Clock (RTC) module of the XE167 can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

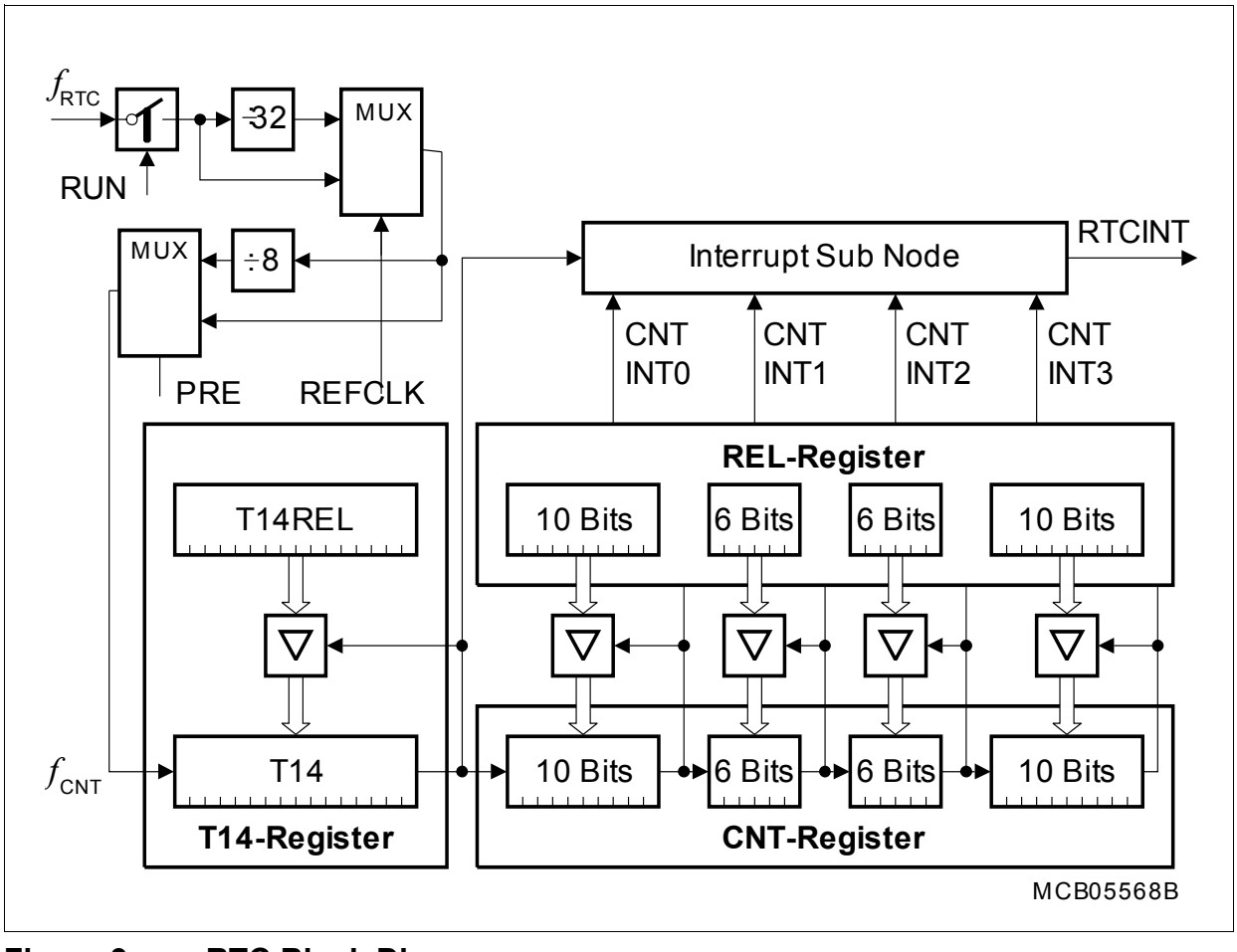

Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

3.10 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 16 + 8 multiplexed input channels and a sample and hold circuit have been integrated on-chip. They use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically.

For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XE167 support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features, such as limit checking or result accumulation, reduce the number of required CPU access operations allowing the precise evaluation of analoginputs (high conversion rate) even at a low CPU speed.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately with registers P5_DIDIS and P15_DIDIS (Port x Digital Input Disable).

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Table 9 Summary of the XE167's Parallel Ports (cont'd)

Port	Width	Alternate Functions
Port 5	16	Analog input channels to ADC0, Input/Output lines for CCU6x, Timer control signals, JTAG, OCDS control, interrupts
Port 6	4	ADC control lines, Serial interface lines of USIC1, Timer control signals, OCDS control
Port 7	5	ADC control lines, Serial interface lines of USIC0 and CAN4, Input/Output lines for CCU62, Timer control signals, JTAG, OCDS control,system clock output
Port 8	7	Input/Output lines for CCU60, JTAG, OCDS control
Port 9	8	Serial interface lines of USIC2, Input/Output lines for CCU60 and CCU63, OCDS control
Port 10	16	Address and/or data lines, bus control, Serial interface lines of USIC0, USIC1, CAN2, CAN3, and CAN4, Input/Output lines for CCU60, JTAG, OCDS control
Port 11	6	Input/Output lines for CCU63
Port 15	8	Analog input channels to ADC1, Timer control signals

4 Electrical Parameters

The operating range for the XE167 is defined by its electrical parameters. For proper operation the specified limits must be respected during system design.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature	T_{ST}	-65	–	150	°C	–
Junction temperature	T_J	-40	–	125	°C	under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDIM}, V_{DDI1}	-0.5	–	1.65	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDPA}, V_{DDPB}	-0.5	–	6.0	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} < V_{DDPmax}$
Input current on any pin during overload condition	–	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	–	–	–	|100|	mA	–
Output current on any pin	I_{OH}, I_{OL}	–	–	|30|	mA	–

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE167 can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE167 are designed to operate in various driver modes. The DC parameter specifications refer to the current limits in **Table 13**.

Table 13 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]		Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)	
	$V_{DDP} \geq$ 4.5 V	$V_{DDP} <$ 4.5 V	$V_{DDP} \geq$ 4.5 V	$V_{DDP} <$ 4.5 V
Strong driver	10 mA	10 mA	2.5 mA	2.5 mA
Medium driver	4.0 mA	2.5 mA	1.0 mA	1.0 mA
Weak driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Table 16 Switching Power Consumption XE167 (Operating Conditions apply)

Parameter	Sym-bol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT}	–	10 + 0.6×f_{SYS}	10 + 1.0×f_{SYS}	mA	Active mode[1)2)] f_{SYS} in [MHz]
Power supply current in stopover mode, EVVRs on	I_{SSO}	–	1.0	2.0	mA	Stopover Mode[2)]

1) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers' input stages are switched.

2) The pad supply voltage has only a minor influence on this parameter.

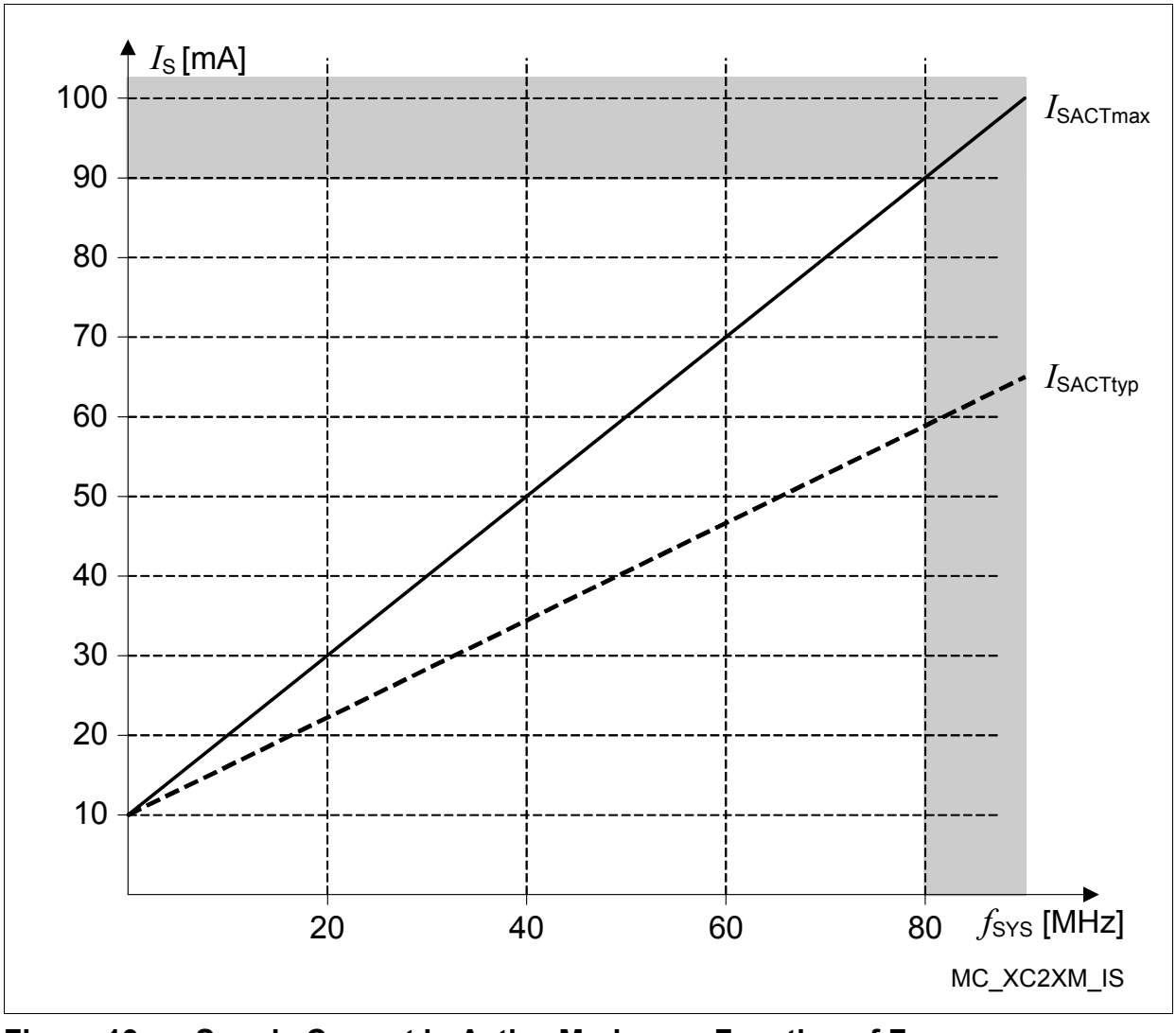

Figure 13 Supply Current in Active Mode as a Function of Frequency

Table 21 Coding of Bitfields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	2.9 V	
0001_B	3.0 V	LEV1V: reset request
0010_B	3.1 V	
0011_B	3.2 V	
0100_B	3.3 V	
0101_B	3.4 V	
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B	4.6 V	
1011_B	4.7 V	
1100_B	4.8 V	
1101_B	4.9 V	
1110_B	5.0 V	
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B	0.9 V	
001_B	1.0 V	
010_B	1.1 V	
011_B	1.2 V	
100_B	1.3 V	LEV1V: reset request
101_B	1.4 V	LEV2V: interrupt request
110_B	1.5 V	
111_B	1.6 V	

1) The indicated default levels are selected automatically after a power reset.

Table 30 External Bus Cycle Timing for Lower Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: RD, WR(L/H)	t_{10} CC	–		20	ns	
Output valid delay for: BHE, ALE	t_{11} CC	–		20	ns	
Output valid delay for: A23 … A16, A15 … A0 (on P0/P1)	t_{12} CC	–		22	ns	
Output valid delay for: A15 … A0 (on P2/P10)	t_{13} CC	–		22	ns	
Output valid delay for: CS	t_{14} CC	–		20	ns	
Output valid delay for: D15 … D0 (write data, MUX-mode)	t_{15} CC	–		21	ns	
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	t_{16} CC	–		21	ns	
Output hold time for: RD, WR(L/H)	t_{20} CC	0		10	ns	
Output hold time for: BHE, ALE	t_{21} CC	0		10	ns	
Output hold time for: A23 … A16, A15 … A0 (on P2/P10)	t_{23} CC	0		10	ns	
Output hold time for: CS	t_{24} CC	0		10	ns	
Output hold time for: D15 … D0 (write data)	t_{25} CC	0		10	ns	
Input setup time for: READY, D15 … D0 (read data)	t_{30} SR	29		–	ns	
Input hold time for: READY, D15 … D0 (read data)[1)]	t_{31} SR	-6		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

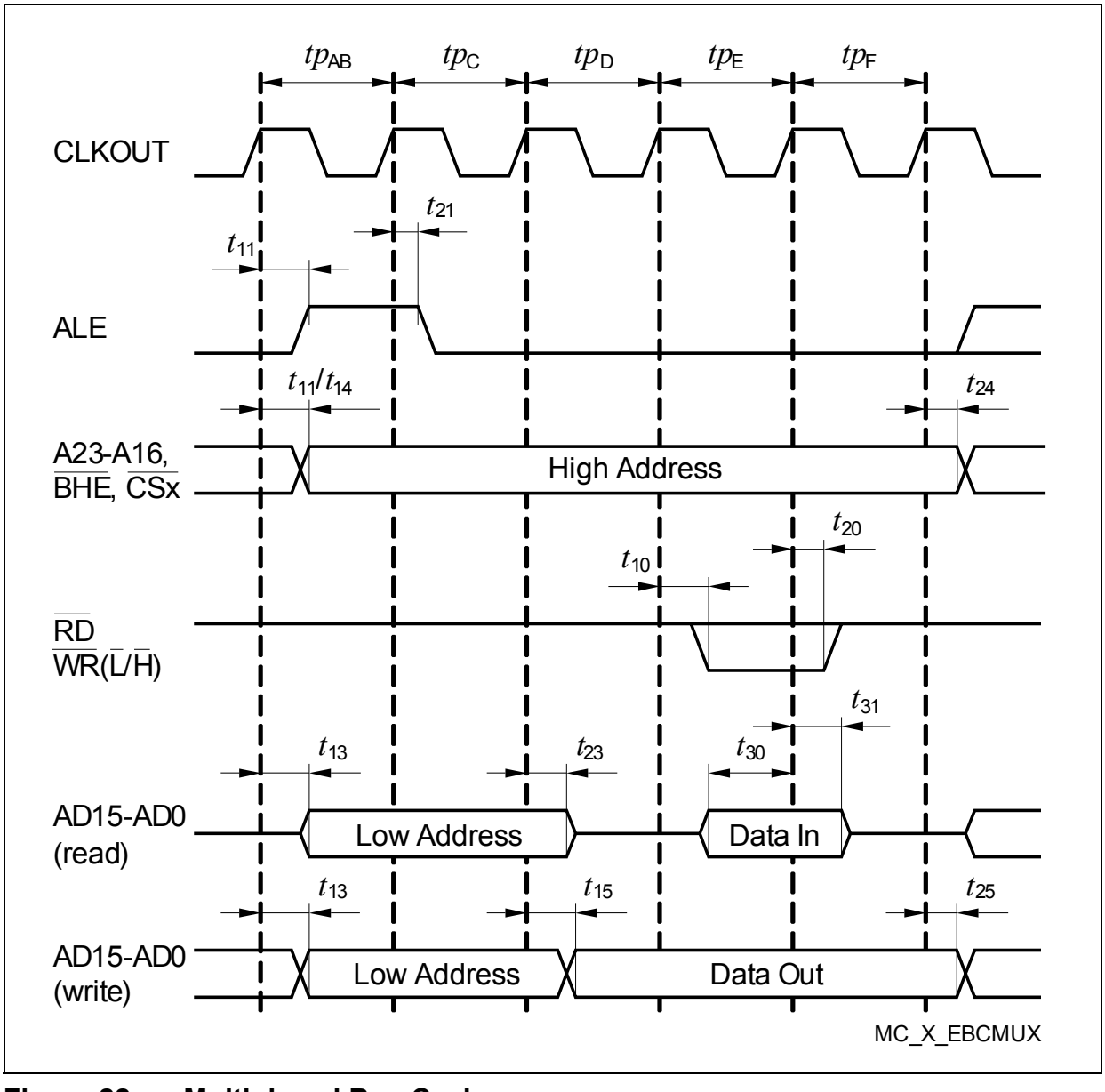

Figure 22 Multiplexed Bus Cycle

w w w . i n f i n e o n . c o m

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