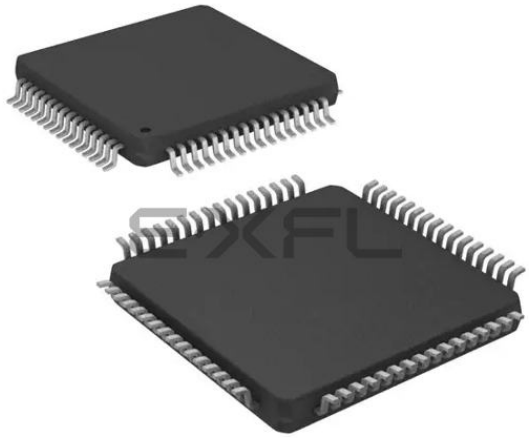

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega384c3-anr

3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA C3 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; two-channel DMA controller, four-channel event system and programmable multilevel interrupt controller, 50 general purpose I/O lines, 16-bit real-time counter (RTC); five, 16-bit timer/counters with compare and PWM channels; three USARTs; two two-wire serial interfaces (TWIs); one full speed USB 2.0 interface; two serial peripheral interfaces (SPIs); AES cryptographic engine; one sixteen-channel, 12-bit ADC with programmable gain; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The ATx devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, DMA controller, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

9. Event System

9.1 Features

- **System for direct peripheral-to-peripheral communication and signaling**
- **Peripherals can directly send, receive, and react to peripheral events**
  - **CPU and DMA controller independent operation**
  - **100% predictable signal timing**
  - **Short and guaranteed response time**
- **Four event channels for up to four different and parallel signal routing configurations**
- **Events can be sent and/or used by most peripherals, clock system, and software**
- **Additional functions include**
  - **Quadrature decoders**
  - **Digital filtering of I/O pin state**
- **Works in active mode and idle sleep mode**

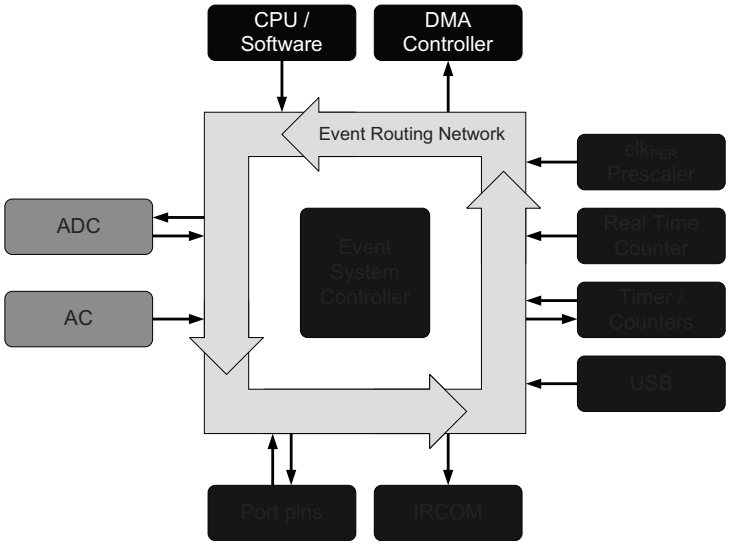
9.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts, CPU, or DMA controller resources, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It also allows for synchronized timing of actions in several peripheral modules.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure on page 17 shows a basic diagram of all connected peripherals. The event system can directly connect together analog to digital converter, analog comparators, I/O port pins, the real-time counter, timer/counters, IR communication module (IRCOM), and USB interface. It can also be used to trigger DMA transactions (DMA controller). Events can also be generated from software and the peripheral clock.

Figure 9-1. Event System Overview and Connected Peripherals



The event routing network consists of four software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to four parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

10. System Clock and Clock Options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal oscillators:**
  - **32MHz run-time calibrated and tuneable oscillator**
  - **2MHz run-time calibrated oscillator**
  - **32.768kHz calibrated oscillator**
  - **32kHz ultra low power (ULP) oscillator with 1kHz output**
- **External clock options**
  - **0.4MHz - 16MHz crystal oscillator**
  - **32.768kHz crystal oscillator**
  - **External clock**
- **PLL with 20MHz - 128MHz output frequency**
  - **Internal and external clock options and 1x to 31x multiplication**
  - **Lock detector**
- **Clock prescalers with 1x to 2048x division**
- **Fast peripheral clocks running at two and four times the CPU clock**
- **Automatic run-time calibration of internal oscillators**
- **External oscillator and PLL lock failure detection with optional non-maskable interrupt**

10.2 Overview

Atmel AVR XMEGA C3 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 10-1 on page 19 presents the principal clock system. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 21.

13. WDT – Watchdog Timer

13.1 Features

- **Issues a device reset if the timer is not reset before its timeout period**
- **Asynchronous operation from dedicated oscillator**
- **1kHz output of the 32kHz ultra low power oscillator**
- **11 selectable timeout periods, from 8ms to 8s**
- **Two operation modes:**
  - **Normal mode**
  - **Window mode**
- **Configuration lock to prevent unwanted changes**

13.2 Overview

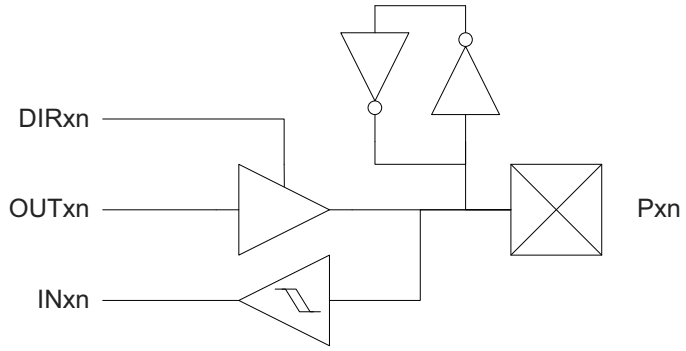
The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

Figure 15-4. I/O Configuration - Totem-pole with Bus-keeper



15.3.5 Others

Figure 15-5. Output Configuration - Wired-OR with Optional Pull-down

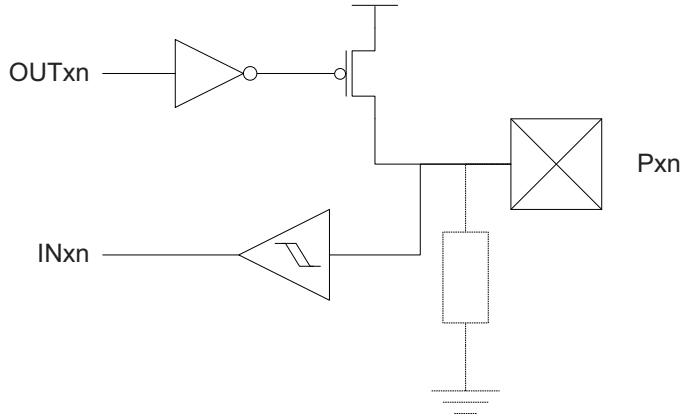
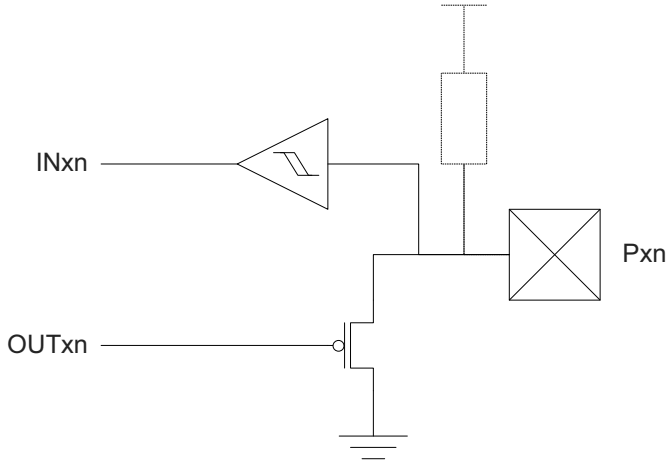


Figure 15-6. I/O Configuration - Wired-AND with Optional Pull-up



20. RTC – 16-bit Real-Time Counter

20.1 Features

- **16-bit resolution**
- **Selectable clock source**
  - **32.768kHz external crystal**
  - **External clock**
  - **32.768kHz internal oscillator**
  - **32kHz internal ULP oscillator**
- **Programmable 10-bit clock prescaling**
- **One compare register**
- **One period register**
- **Clear counter on period overflow**
- **Optional interrupt/event on overflow and compare match**

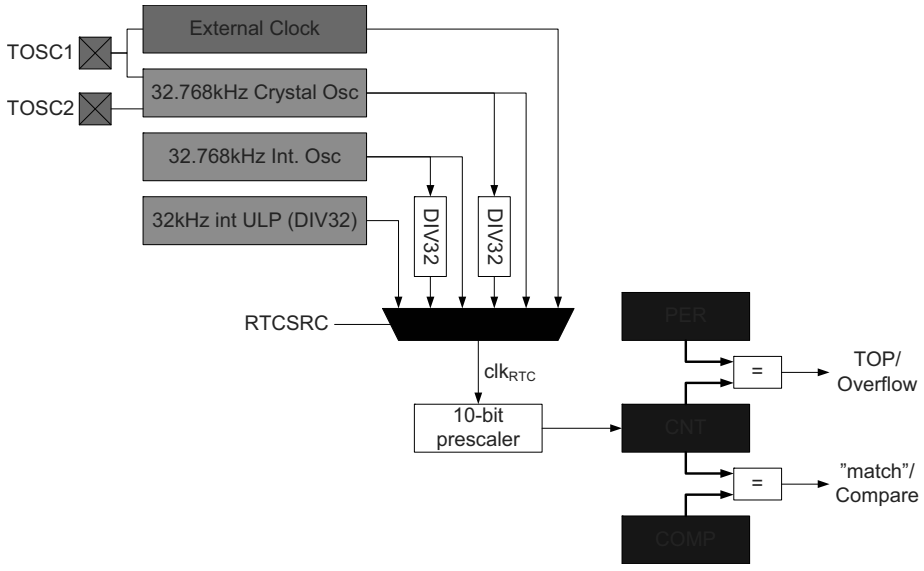
20.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 20-1. Real-time Counter Overview



23. SPI – Serial Peripheral Interface

23.1 Features

- **Two Identical SPI peripherals**
- **Full-duplex, three-wire synchronous data transfer**
- **Master or slave operation**
- **Lsb first or msb first data transfer**
- **Eight programmable bit rates**
- **Interrupt flag at the end of transmission**
- **Write collision flag to indicate data collision**
- **Wake up from idle sleep mode**
- **Double speed master mode**

23.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

24. USART

24.1 Features

- **Three identical USART peripherals**
- **Full-duplex operation**
- **Asynchronous or synchronous operation**
  - **Synchronous clock rates up to 1/2 of the device clock frequency**
  - **Asynchronous clock rates up to 1/8 of the device clock frequency**
- **Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits**
- **Fractional baud rate generator**
  - **Can generate desired baud rate from any system clock frequency**
  - **No need for external oscillator with certain frequencies**
- **Built-in error detection and correction schemes**
  - **Odd or even parity generation and parity check**
  - **Data overrun and framing error detection**
  - **Noise filtering includes false start bit detection and digital low-pass filter**
- **Separate interrupts for**
  - **Transmit complete**
  - **Transmit data register empty**
  - **Receive complete**
- **Multiprocessor communication mode**
  - **Addressing scheme to address a specific devices on a multidevice bus**
  - **Enable unaddressed devices to automatically ignore all frames**
- **Master SPI mode**
  - **Double buffered operation**
  - **Operation up to 1/2 of the peripheral clock frequency**
- **IRCOM module for IrDA compliant pulse modulation/demodulation**

24.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

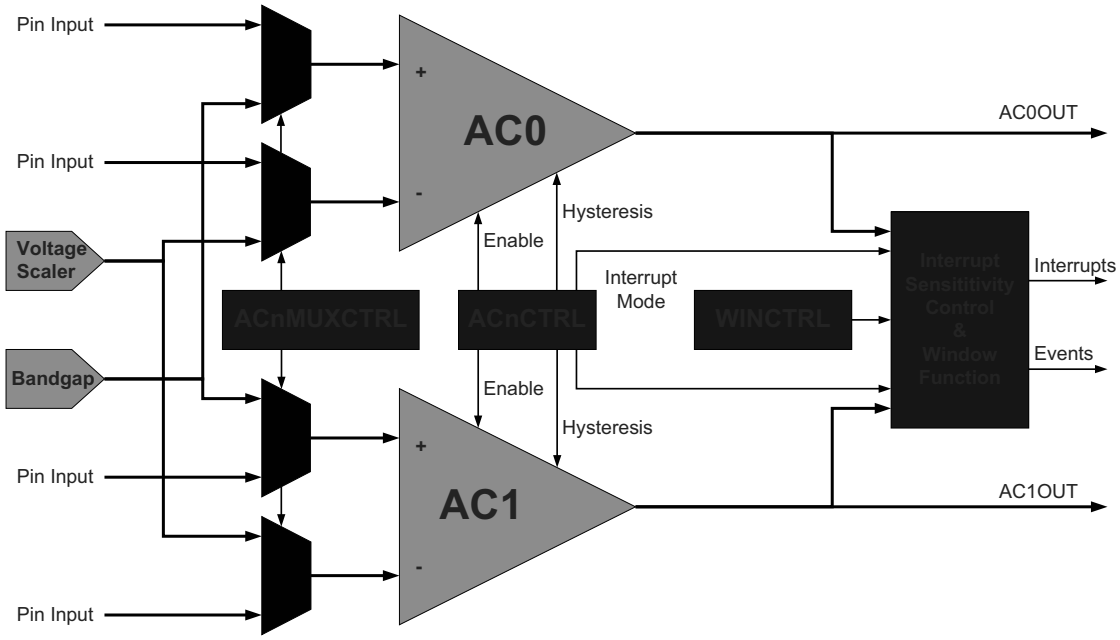
The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2kbps.

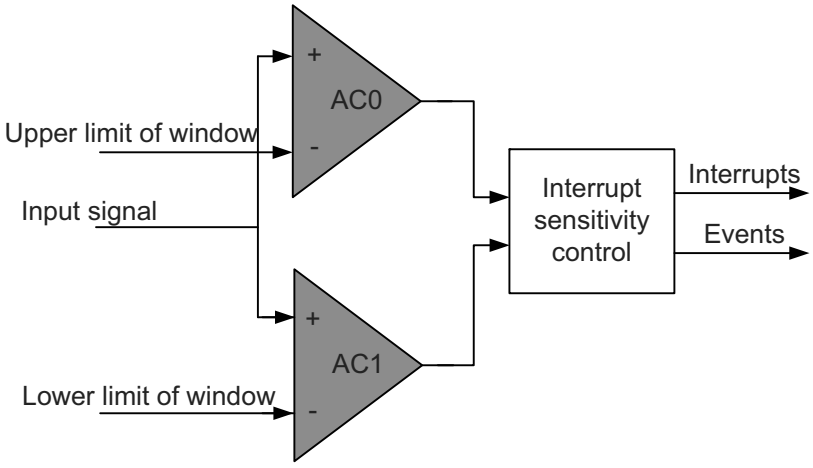
PORTC, PORTD, and PORTE each has one USART. Notation of these peripherals are USARTC0, USARTD0, and USARTE0, respectively.

Figure 29-1. Analog Comparator Overview



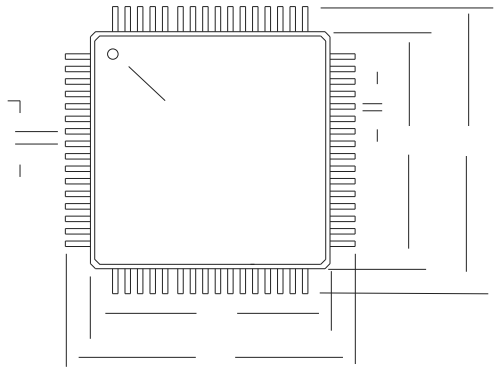
The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 29-2.

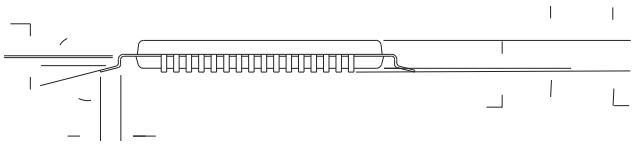
Figure 29-2. Analog Comparator Window Function



34. Packaging Information

34.1 64A

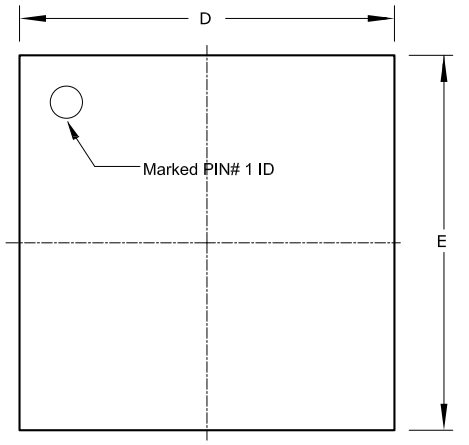




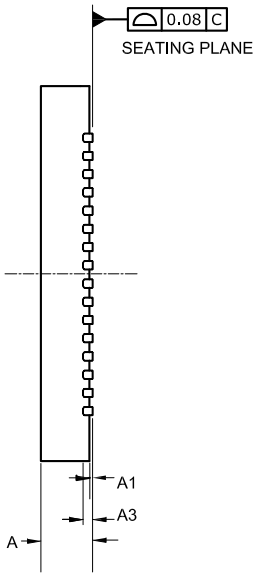
2325 Orchard Parkway San Jose, CA 95131	TITLE	DRAWING NO.	REV.

34.2 64Z3

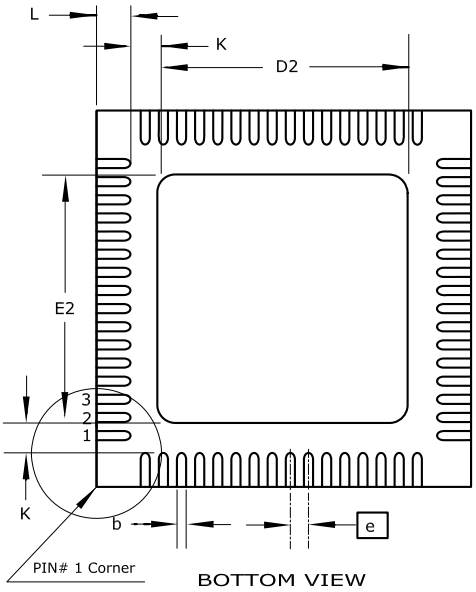
DRAWINGS NOT SCALED



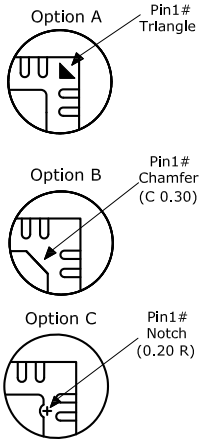
TOP VIEW



SIDE VIEW



BOTTOM VIEW



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	----	----	1.00	
A1	----	0.02	0.05	
A3		0.20 REF		
D/E	8.90	9.00	9.10	
D2/E2	7.50	7.65	7.80	
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	
b	0.18	----	0.30	2
e		0.50 BSC		
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

12/18/2012

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	PP, 64 Lds - 0.50mm Pitch, 9x9x1mm Body size Very Thin Quad Flat Package (VQFN) Sawn	ZFF	PP	A

35.3 Current Consumption

Table 35-4. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		150		µA
			V_{CC} = 3.0V		320		
		1MHz, Ext. Clk	V_{CC} = 1.8V		410		
			V_{CC} = 3.0V		830		
		2MHz, Ext. Clk	V_{CC} = 1.8V		660	800	
			V_{CC} = 3.0V		1.3	1.8	mA
		32MHz, Ext. Clk			10	15	
	Idle power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4		µA
			V_{CC} = 3.0V		5		
		1MHz, Ext. Clk	V_{CC} = 1.8V		50		
			V_{CC} = 3.0V		100		
		2MHz, Ext. Clk	V_{CC} = 1.8V		100	350	
			V_{CC} = 3.0V		200	600	
		32MHz, Ext. Clk			3.3	7	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.2	1.0	µA
		T = 85°C			3.5	6.0	
		T = 105°C			16	27	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.5	2.0	
		WDT and sampled BOD enabled, T = 85°C			6	10	
		WDT and sampled BOD enabled, T = 105°C			15	27	
	Power-save power consumption(2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.4		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2	
			V_{CC} = 3.0V		0.8	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3	
			V_{CC} = 3.0V		1.1	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Figure 36-11.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

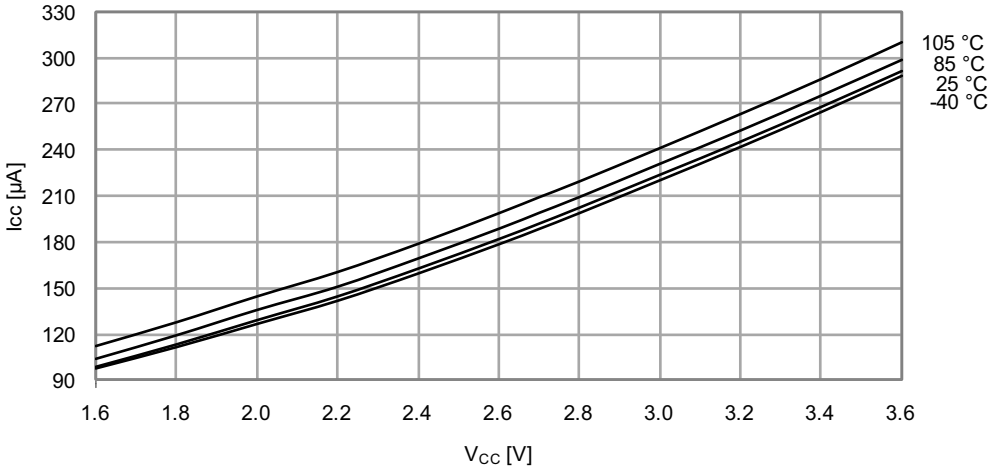


Figure 36-12.Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

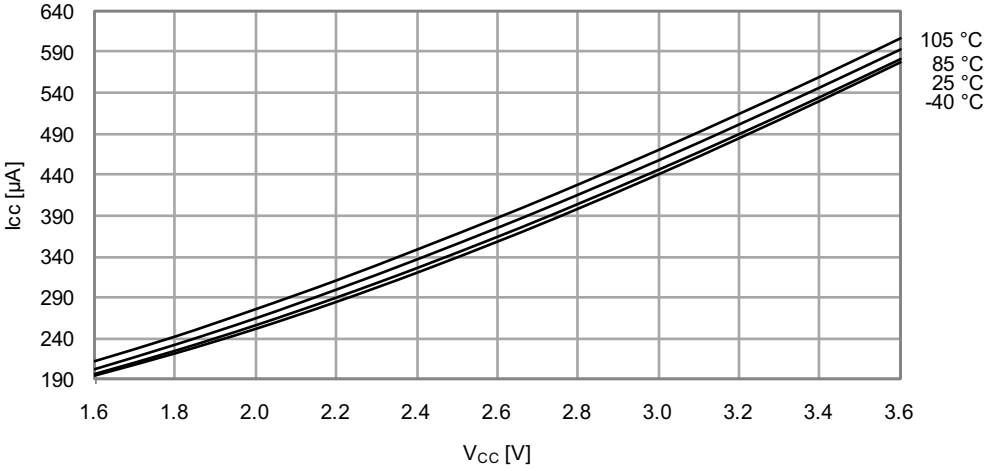


Figure 36-31.INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

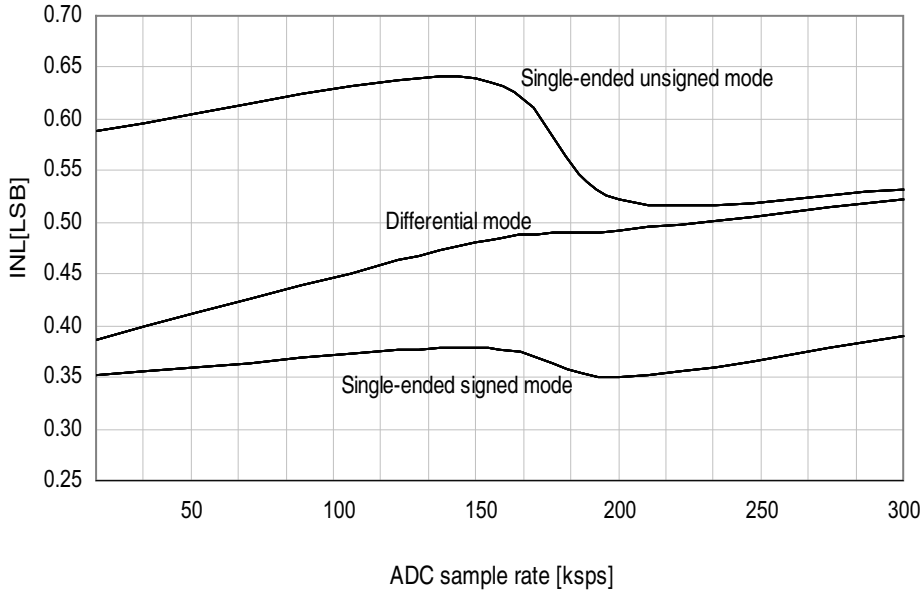


Figure 36-32.INL Error vs. Input Code

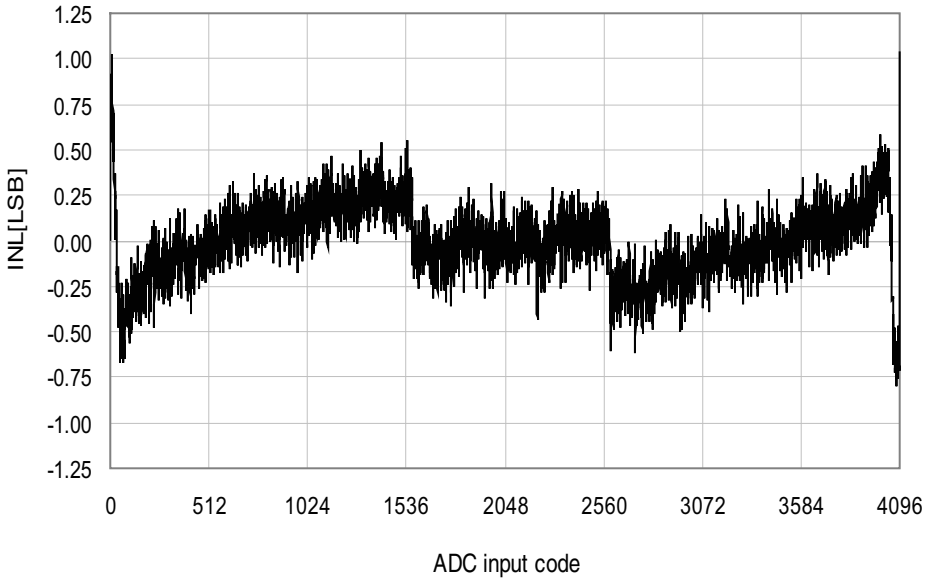


Figure 36-33.DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

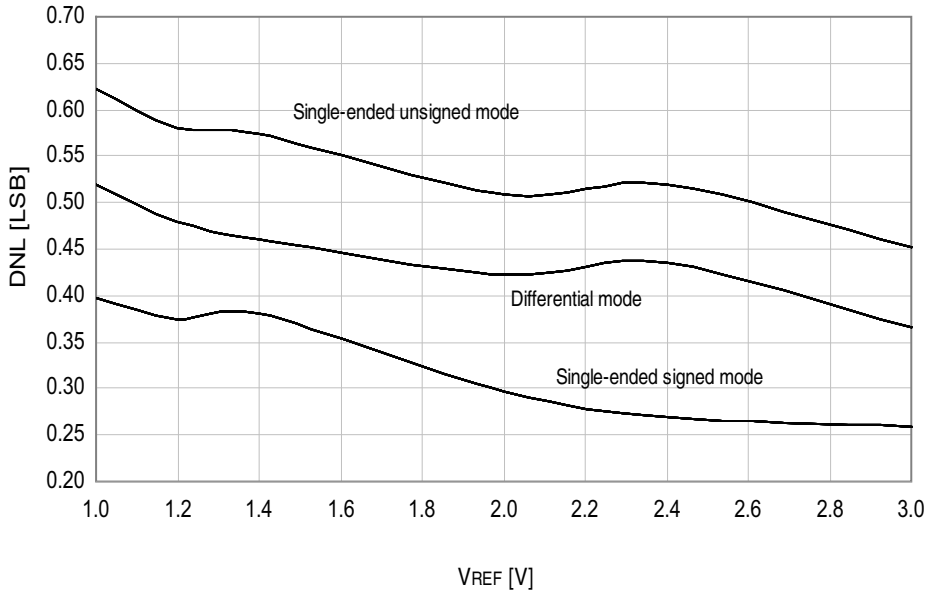


Figure 36-34.DNL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

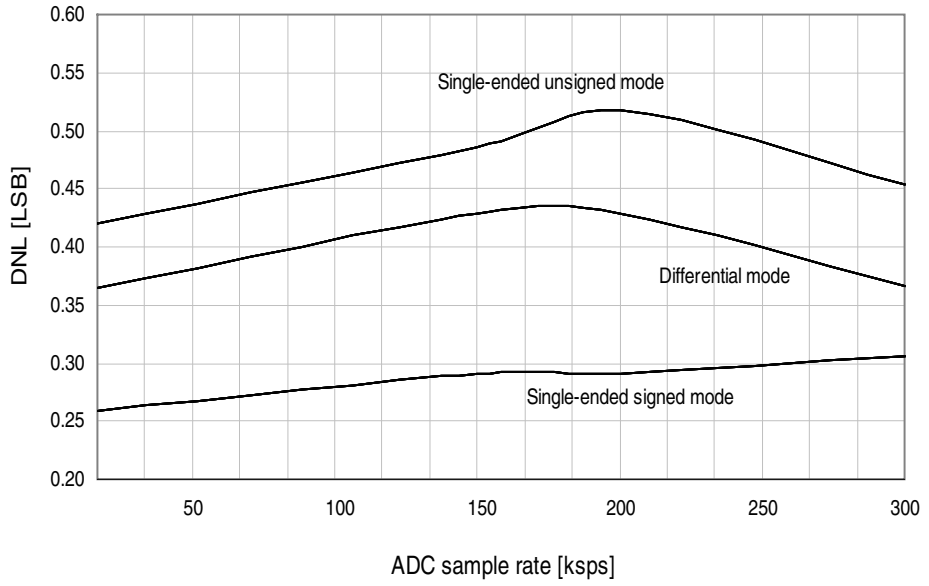


Figure 36-35.DNL Error vs. Input Code

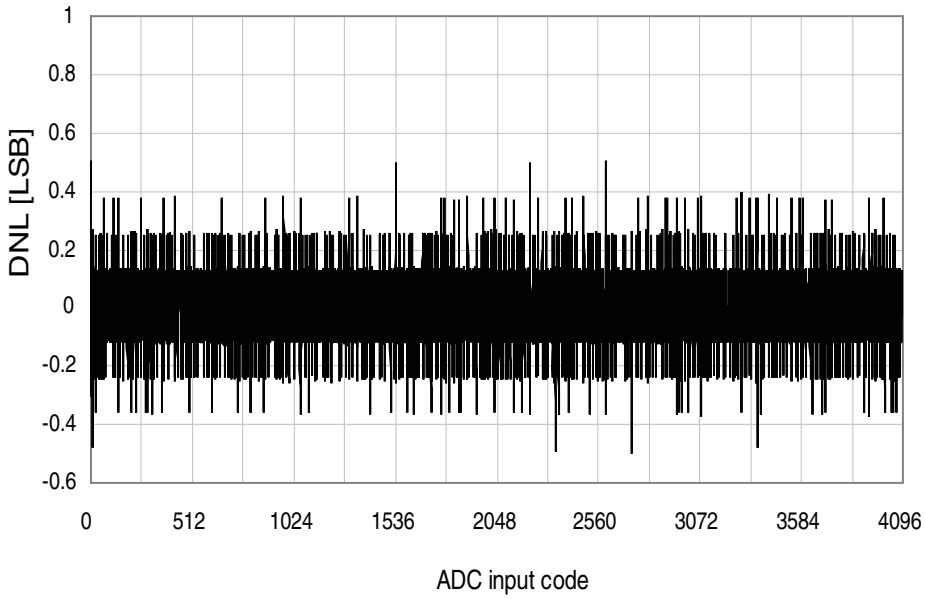


Figure 36-36.Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

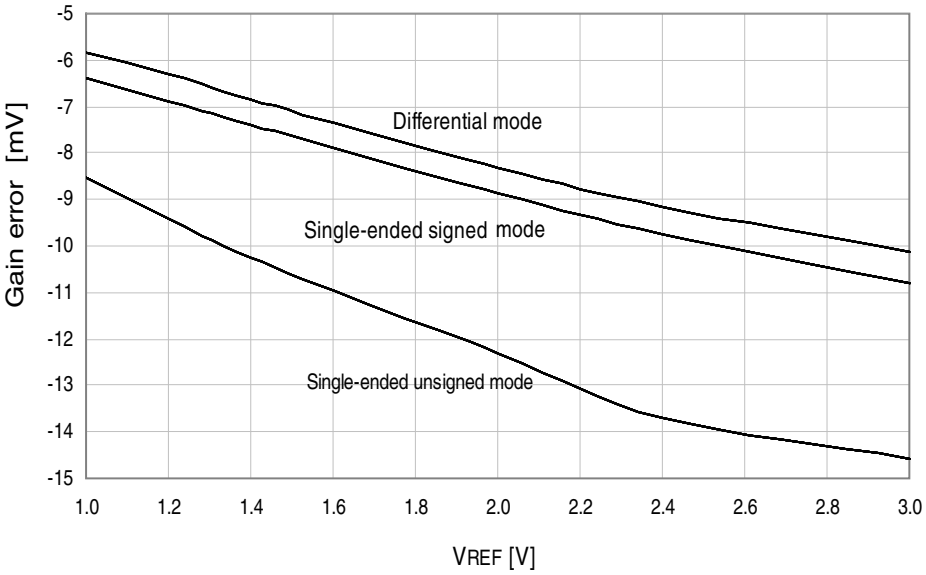


Figure 36-57. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

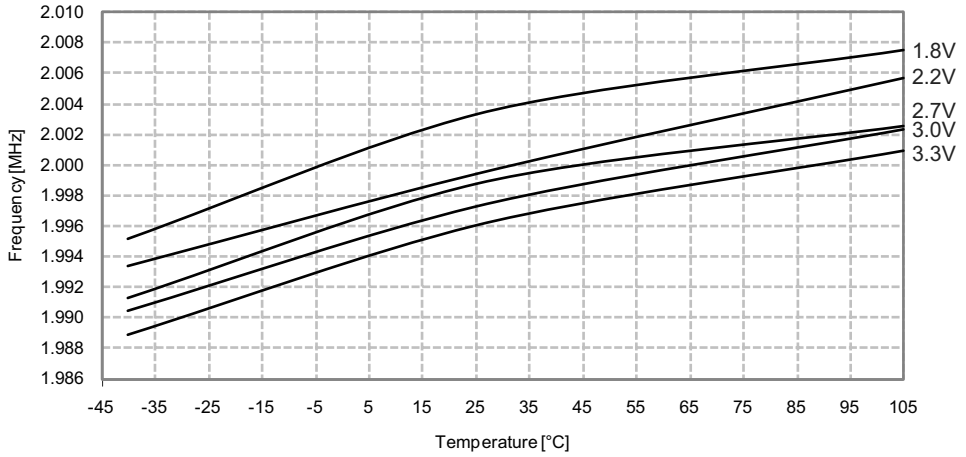
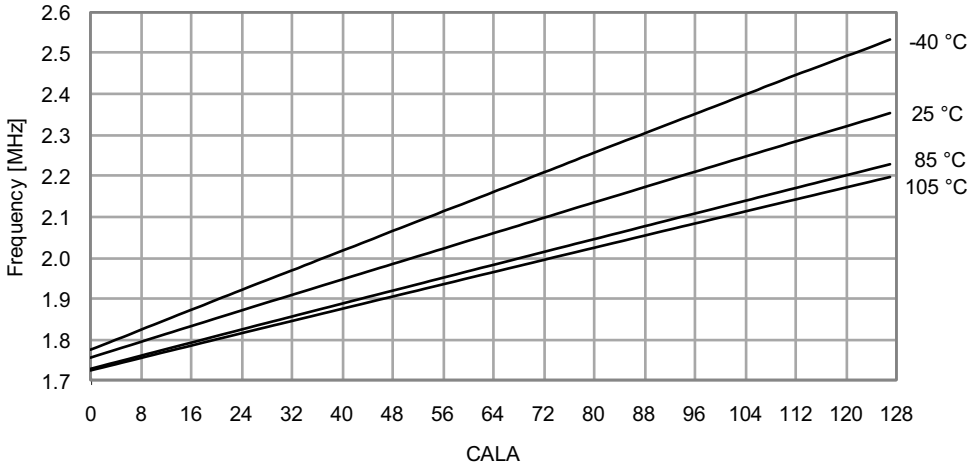


Figure 36-58. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V



36.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 36-63. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

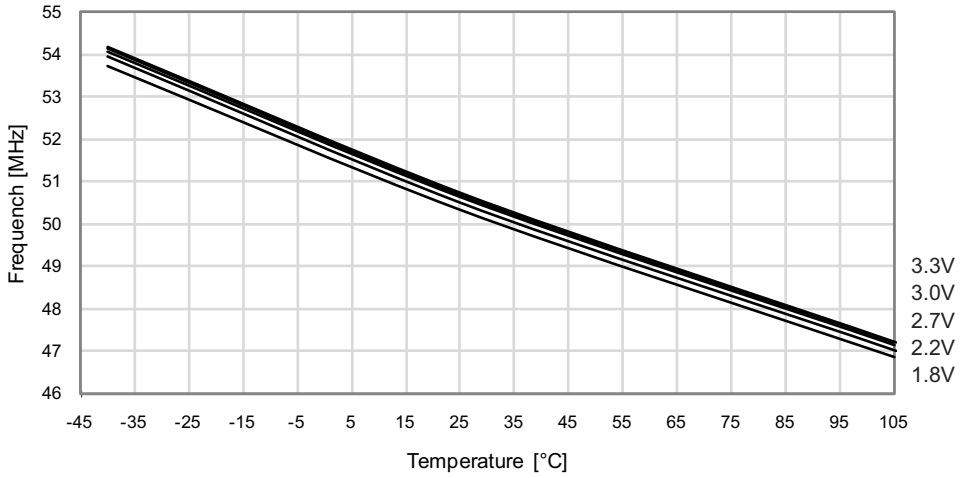
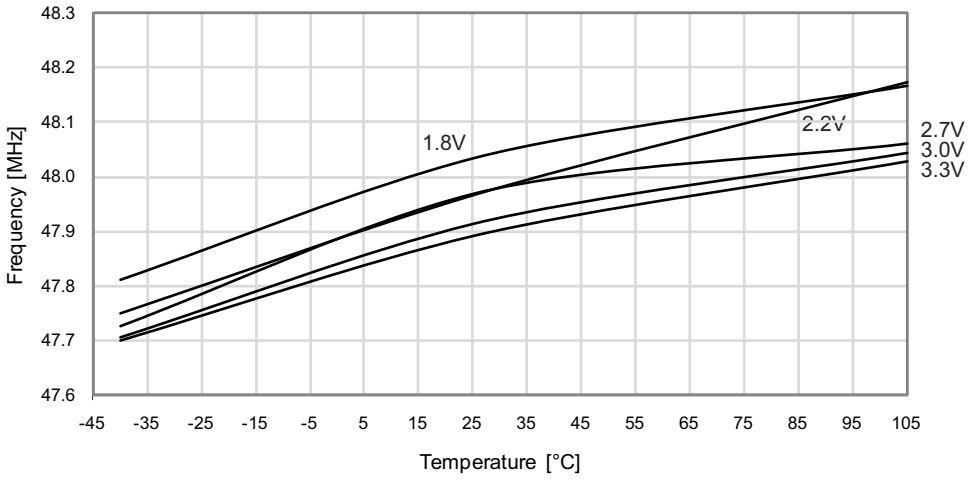


Figure 36-64. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



36.9 Two-Wire Interface Characteristics

Figure 36-65. SDA Hold Time vs. Temperature

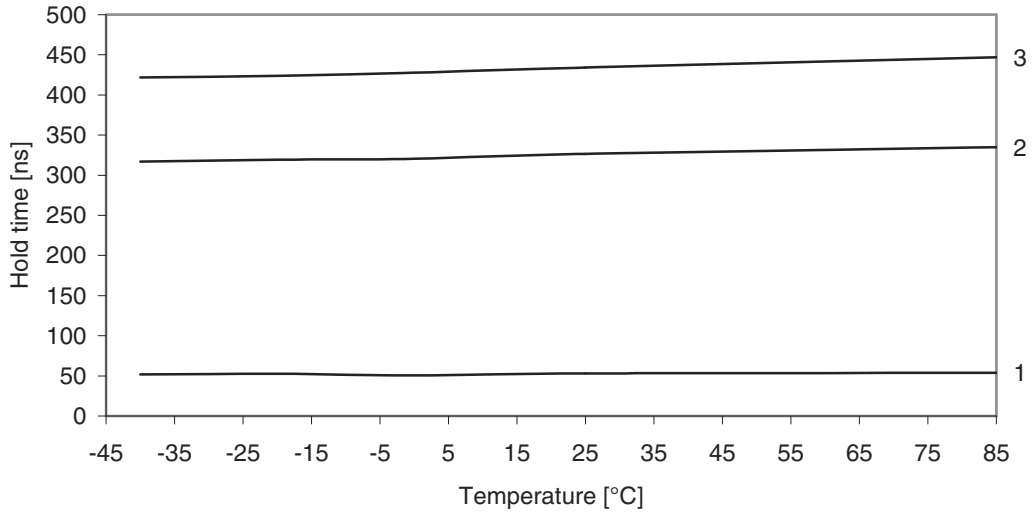
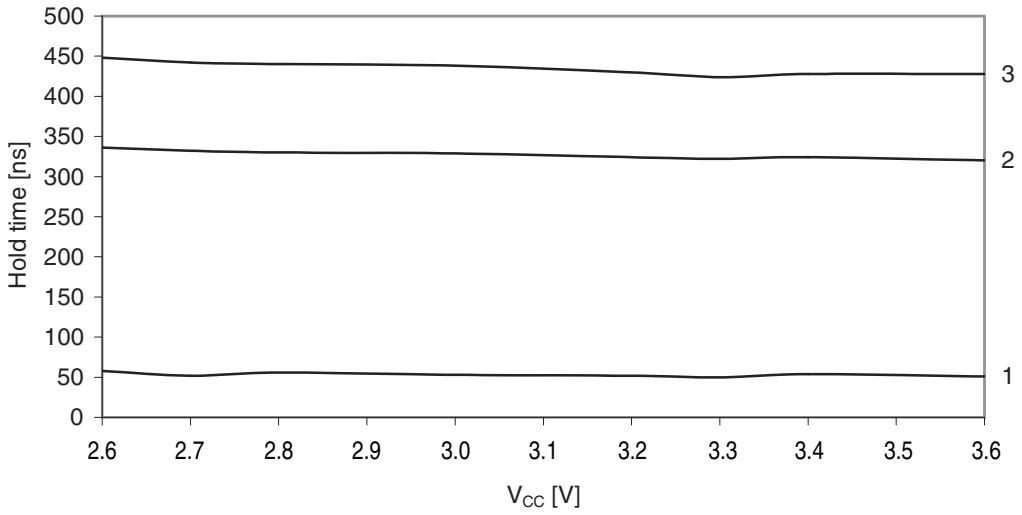


Figure 36-66. SDA Hold Time vs. Supply Voltage



38.7 8361A – 02/2012

1. Initial revision.