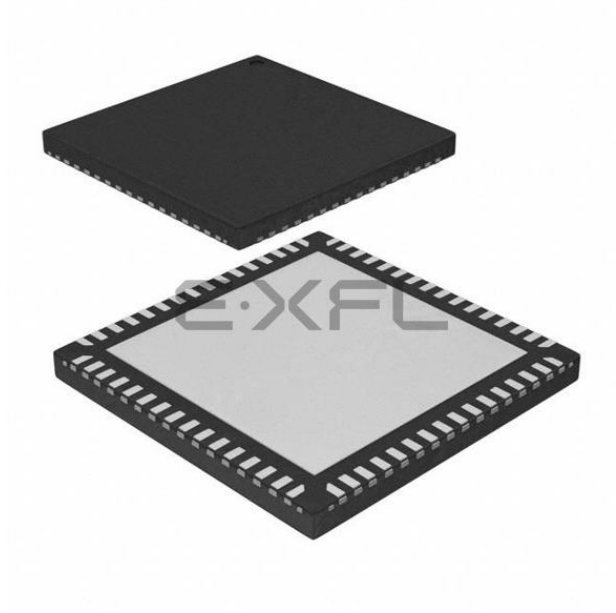

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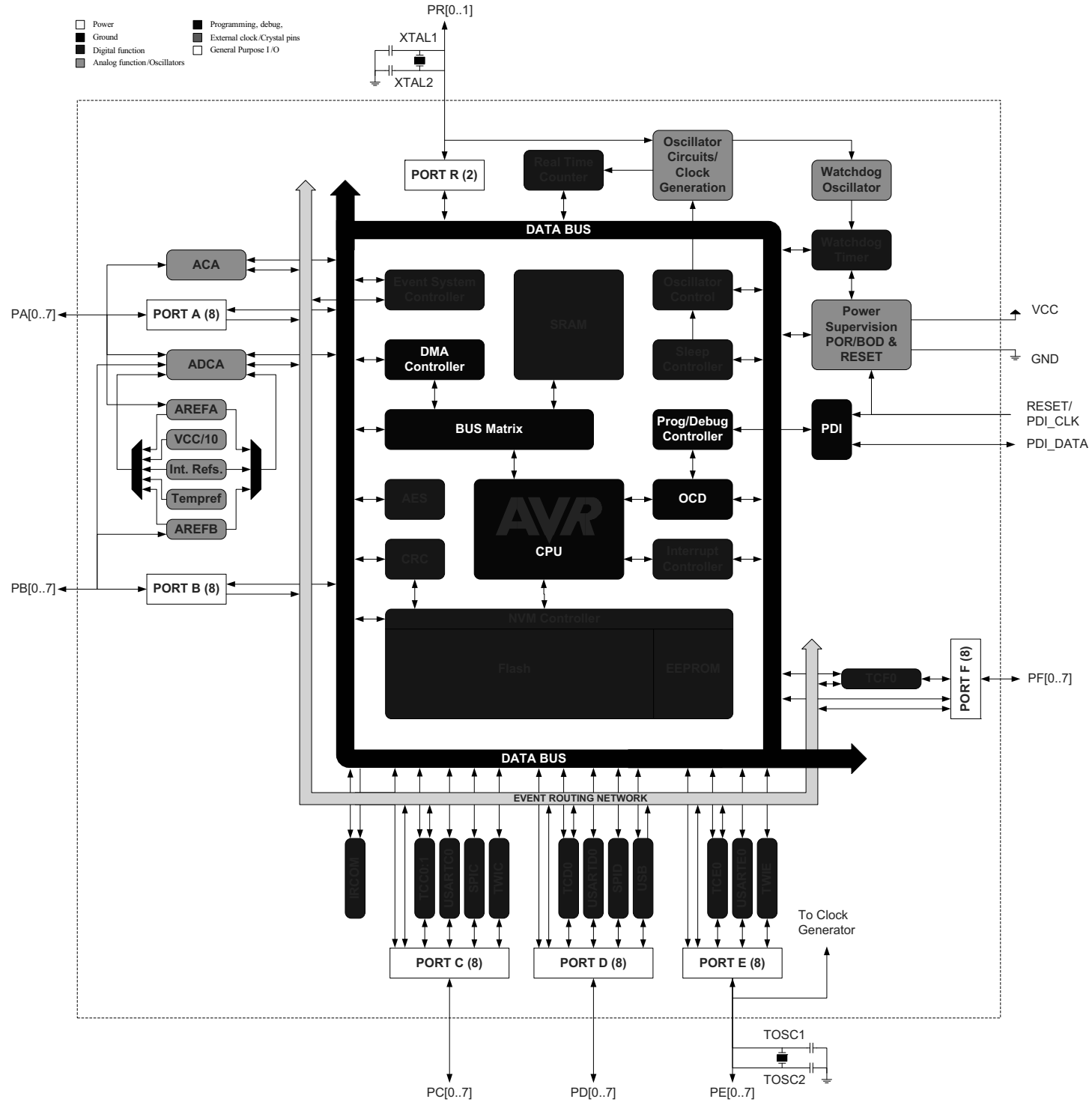
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega384c3-mh

3.1 Block Diagram

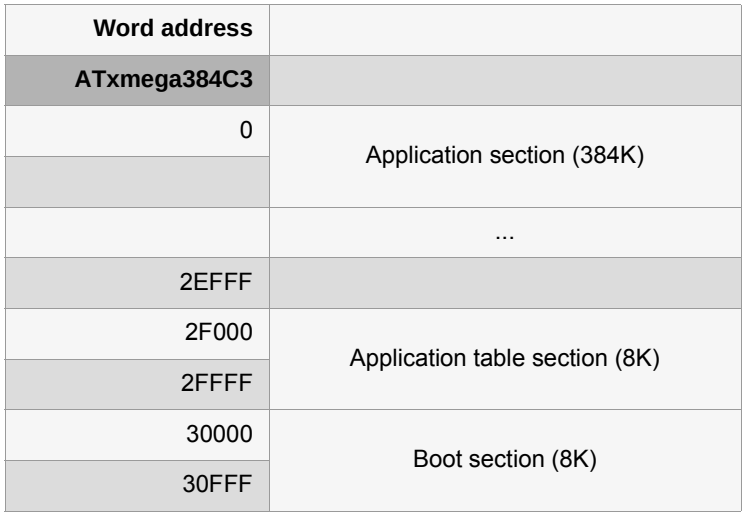
Figure 3-1. XMEGA C3 Block Diagram



device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash Program Memory (hexadecimal address)



7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 65.

10. System Clock and Clock Options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal oscillators:**
  - **32MHz run-time calibrated and tuneable oscillator**
  - **2MHz run-time calibrated oscillator**
  - **32.768kHz calibrated oscillator**
  - **32kHz ultra low power (ULP) oscillator with 1kHz output**
- **External clock options**
  - **0.4MHz - 16MHz crystal oscillator**
  - **32.768kHz crystal oscillator**
  - **External clock**
- **PLL with 20MHz - 128MHz output frequency**
  - **Internal and external clock options and 1x to 31x multiplication**
  - **Lock detector**
- **Clock prescalers with 1x to 2048x division**
- **Fast peripheral clocks running at two and four times the CPU clock**
- **Automatic run-time calibration of internal oscillators**
- **External oscillator and PLL lock failure detection with optional non-maskable interrupt**

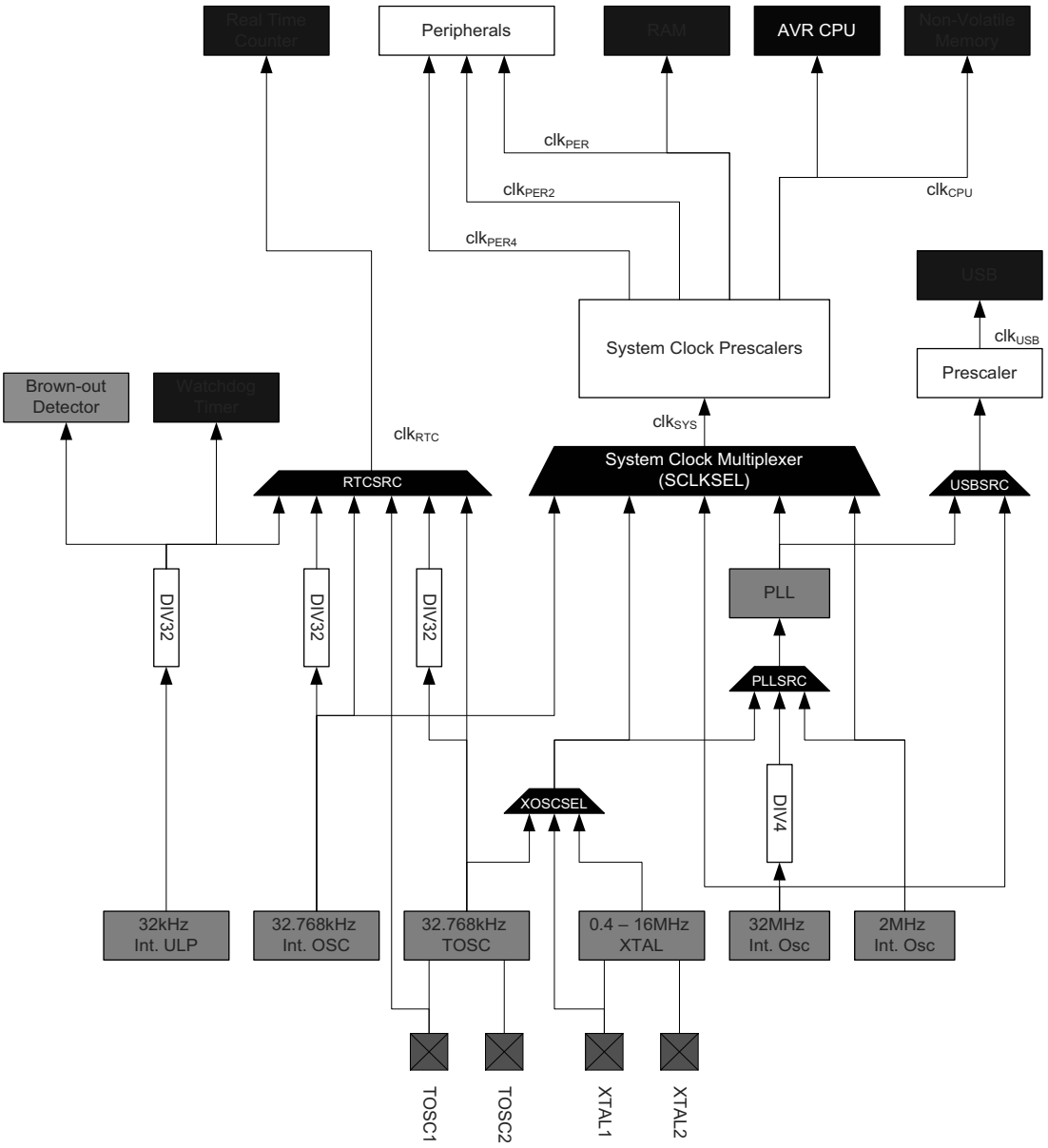
10.2 Overview

Atmel AVR XMEGA C3 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 10-1 on page 19 presents the principal clock system. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 21.

Figure 10-1. The Clock System, Clock Sources, and Clock Distribution



10.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources, DFLLs and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

10.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

11. Power Management and Sleep Modes

11.1 Features

- **Power management for adjusting power consumption and functions**
- **Five sleep modes**
  - **Idle**
  - **Power down**
  - **Power save**
  - **Standby**
  - **Extended standby**
- **Power reduction register to disable clock and turn off unused peripherals in active and idle modes**

11.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

11.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

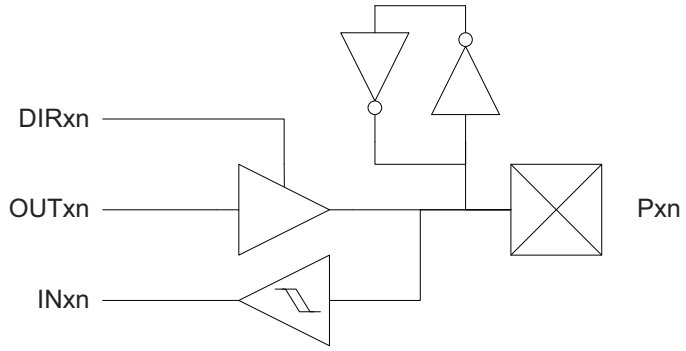
11.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, event system and DMA controller are kept running. Any enabled interrupt will wake the device.

11.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

Figure 15-4. I/O Configuration - Totem-pole with Bus-keeper



15.3.5 Others

Figure 15-5. Output Configuration - Wired-OR with Optional Pull-down

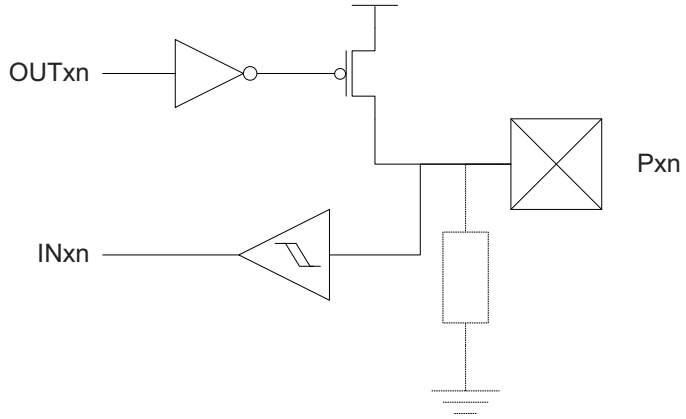
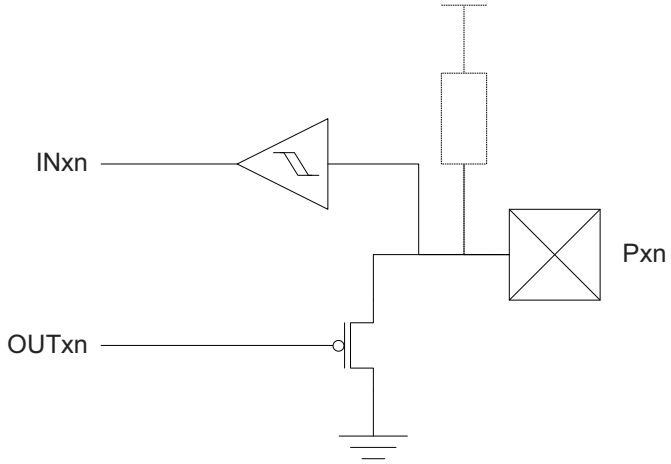


Figure 15-6. I/O Configuration - Wired-AND with Optional Pull-up

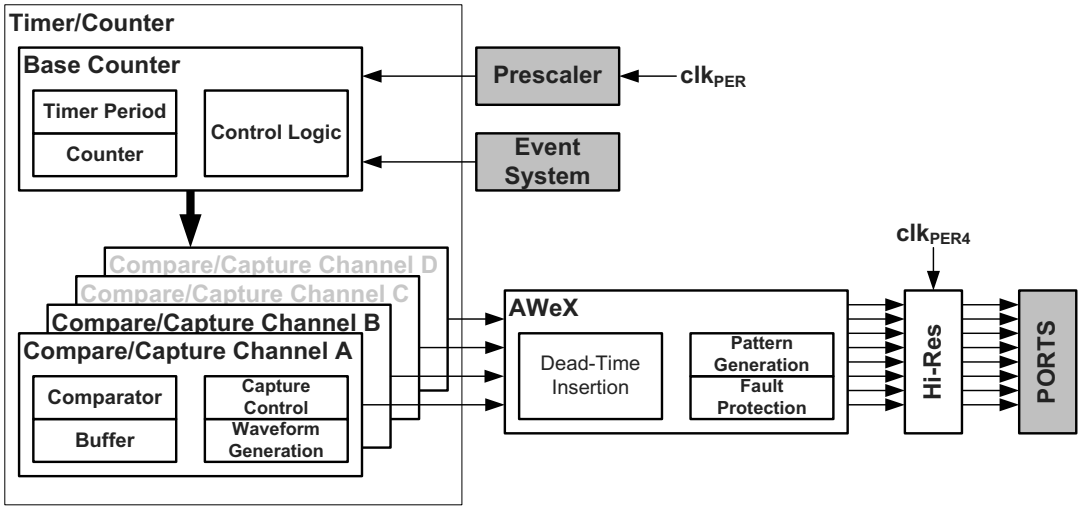


Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See “AWeX – Advanced Waveform Extension” on page 35 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 36 for more details.

Figure 16-1. Overview of a Timer/Counter and Closely Related Peripherals



PORTC has one Timer/Counter 0 and one Timer/Counter1. PORTD, PORTE, and PORTF each has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCE0, and TCF0, respectively.

19. Hi-Res – High Resolution Extension

19.1 Features

- **Increases waveform generator resolution up to 8x (three bits)**
- **Supports frequency, single-slope PWM, and dual-slope PWM generation**
- **Supports the AWeX when this is used for the same timer/counter**

19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There is one hi-res extensions that can be enabled for timer/counters pair on PORTC. The notation of this is HIRESC.

25. IRCOM – IR Communication Module

25.1 Features

- **Pulse modulation/demodulation for infrared communication**
- **IrDA compatible for baud rates up to 115.2Kbps**
- **Selectable pulse modulation scheme**
  - **3/16 of the baud rate period**
  - **Fixed pulse period, 8-bit programmable**
  - **Pulse modulation disabled**
- **Built-in filtering**
- **Can be connected to and used by any USART**

25.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

31. Pinout and Pin Functions

The device pinout is shown in “Pinout/Block Diagram” on page 3. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

31.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

31.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

31.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

31.1.3 Analog Functions

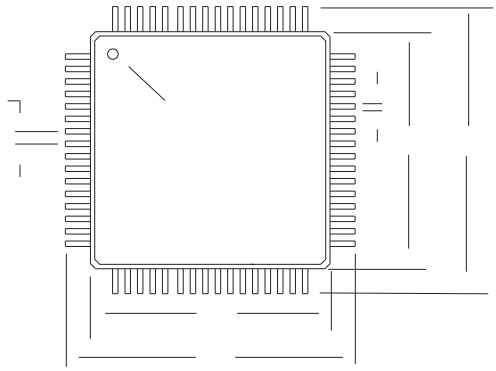
ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
A_{REF}	Analog Reference input pin

31.1.4 Timer/Counter and AWEX Functions

OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

34. Packaging Information

34.1 64A



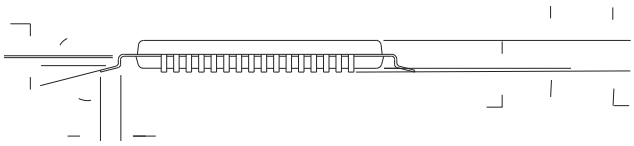


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Table 35-5. Current Consumption for Modules and Peripherals

Symbol	Parameter	Condition[1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				0.93		µA
	32.768kHz int. oscillator				27		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				240		
		DFLL enabled with 32.768kHz int. osc. as reference			430		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			300		
	Watchdog timer				1		
	BOD	Continuous mode			140		
		Sampled mode, includes ULP oscillator			1.3		
	Internal 1.0V reference				220		
	Temperature sensor				215		
	ADC	16ksps V_{REF} = Ext ref			1.12		mA
			CURRLIMIT = LOW		1.01		
			CURRLIMIT = MEDIUM		0.9		
			CURRLIMIT = HIGH		0.8		
		75ksps V_{REF} = Ext ref	CURRLIMIT = LOW		1.7		
		300ksps V_{REF} = Ext ref			3.1		
	DMA	615KBps between I/O registers and SRAM			115		µA
	USART	Rx and Tx enabled, 9600 BAUD			9.5		
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

Table 35-10. Accuracy Characteristics

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	12-bit resolution	Differential	8	12	12	Bits
			Single ended signed	7	11	11	
			Single ended unsigned	8	12	12	
INL[1]	Integral non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.5	1	lsb
			16ksps, all V_{REF}		0.8	2	
			300ksps, V_{REF} = 3V		0.6	1	
			300ksps, all V_{REF}		1	2	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.5	1	
			16ksps, all V_{REF}		1.3	2	
DNL[1]	Differential non-linearity	Differential mode	16ksps, V_{REF} = 3V		0.3	1	
			16ksps, all V_{REF}		0.5	1	
			300ksps, V_{REF} = 3V		0.35	1	
			300ksps, all V_{REF}		0.5	1	
		Single ended unsigned mode	16ksps, V_{REF} = 3.0V		0.6	1	
			16ksps, all V_{REF}		0.6	1	
	Offset error	Differential mode	300ksps, V_{REF}=3V		-7		mV
			Temperature drift, V_{REF}=3V		0.01		mV/K
			Operating voltage drift		0.16		mV/V
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

Table 35-11. Gain Stage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC}- 0.6	V
	Propagation delay	ADC conversion rate	1/2	1	3	Clk_{ADC} cycles
	Clock rate	Same as ADC	100		1800	kHz
	Gain error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		5		
	Offset error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		5		
		8x gain, normal mode		-20		
		64x gain, normal mode		-126		

35.7 Analog Comparator Characteristics

Table 35-12. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	Vcc=1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	Vcc=1.6V - 3.6V		15		
V_{hys3}	Hysteresis, large	Vcc=1.6V - 3.6V		30		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C		20	90	ns
		V_{CC} = 3.0V, T= 85°C		17		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb
	Current source accuracy after calibration			5		%
	current source calibration range		4		6	µA

35.13 Clock and Oscillator Characteristics

35.13.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 35-19. 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

35.13.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 35-20. 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.23		

35.13.3 Calibrated and Tunable 32MHz Internal Oscillator Characteristics

Table 35-21. 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	35	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.24		

35.13.4 32kHz Internal ULP Oscillator Characteristics

Table 35-22. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%
	Accuracy		-30		30	

Table 35-25. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF=Safety factor				min(RQ)/SF	Ω
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

Figure 36-35.DNL Error vs. Input Code

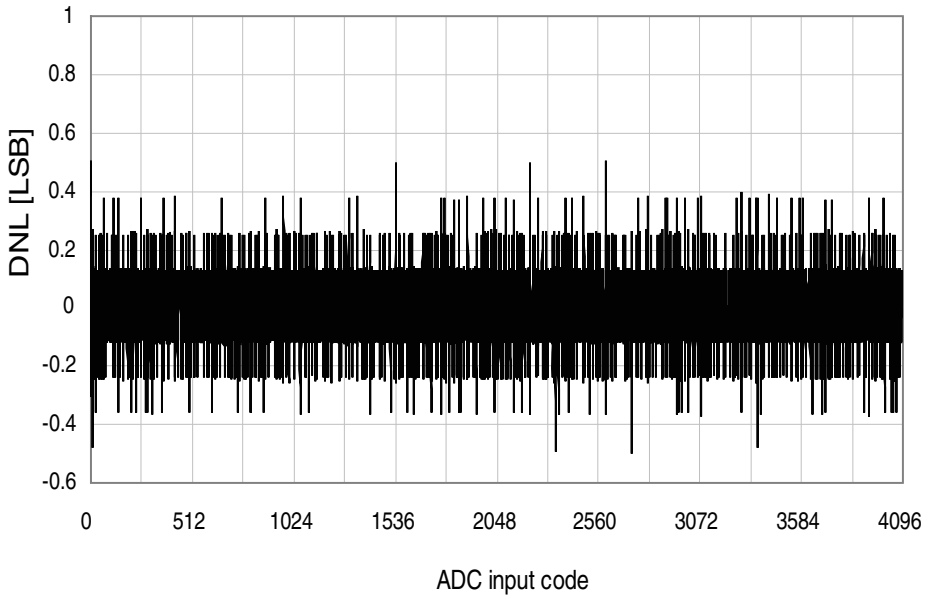


Figure 36-36.Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

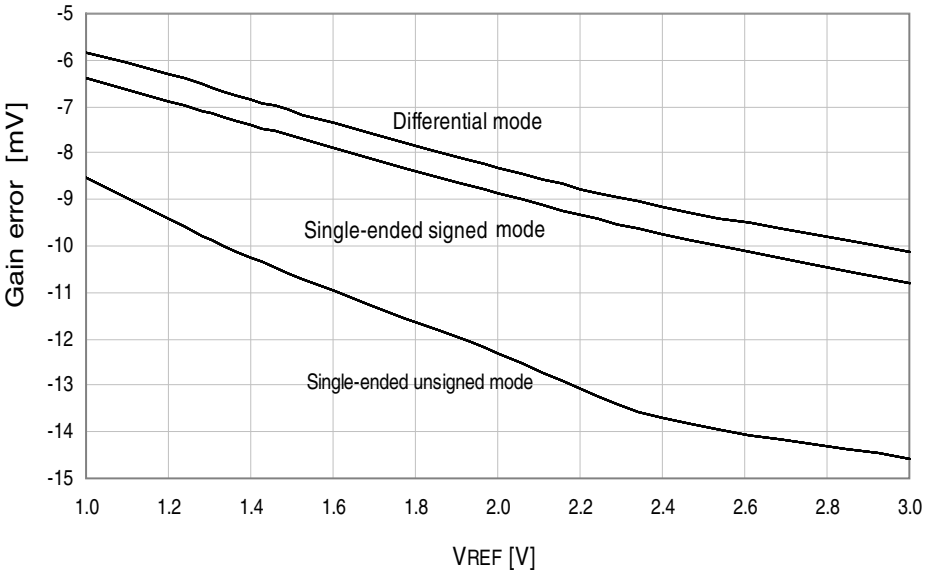


Figure 36-37.Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 300ksps

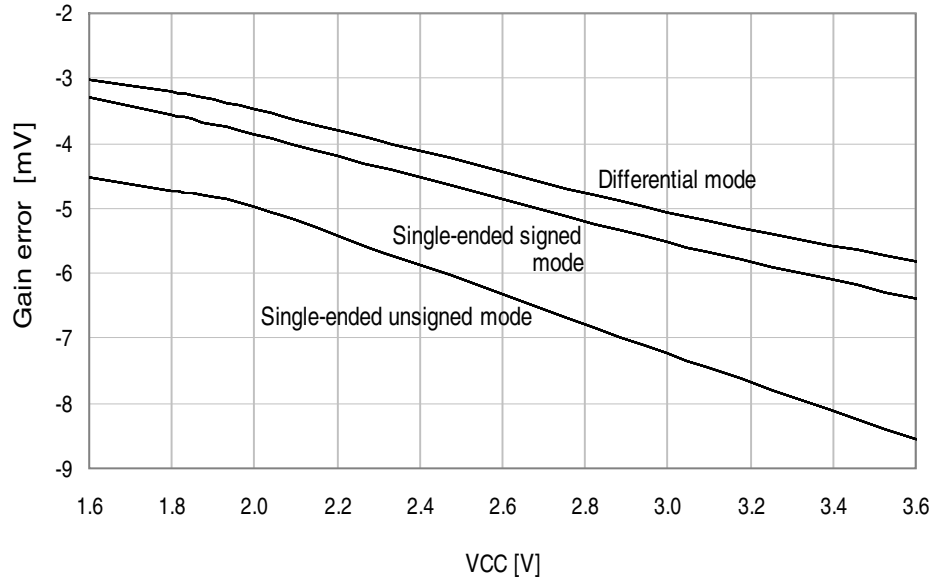


Figure 36-38.Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 300ksps

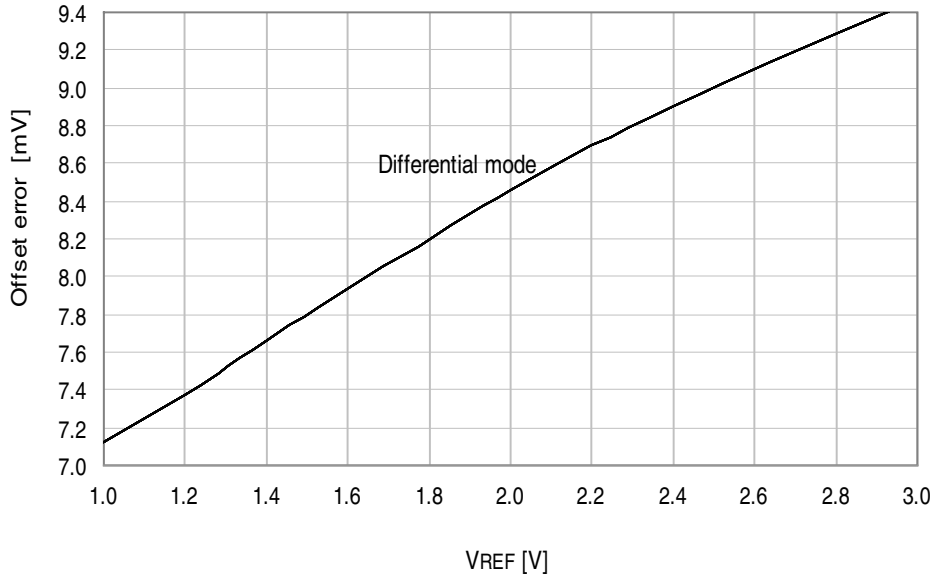


Figure 36-57. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

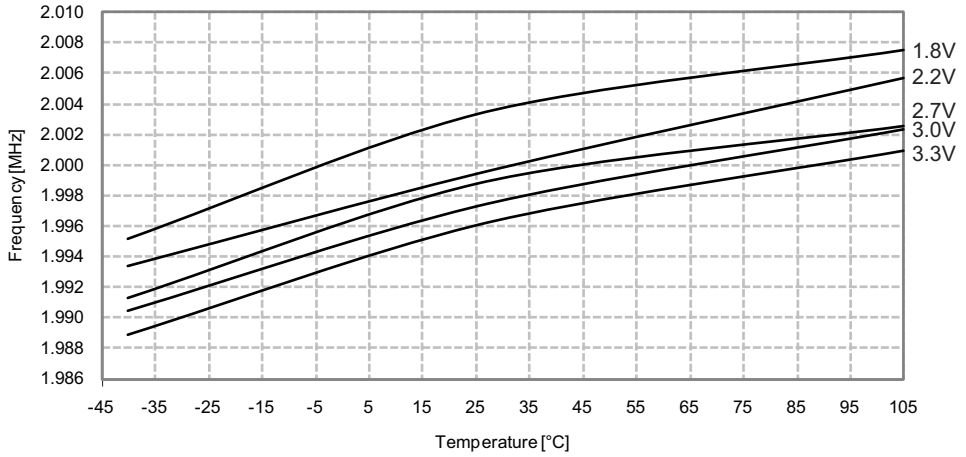
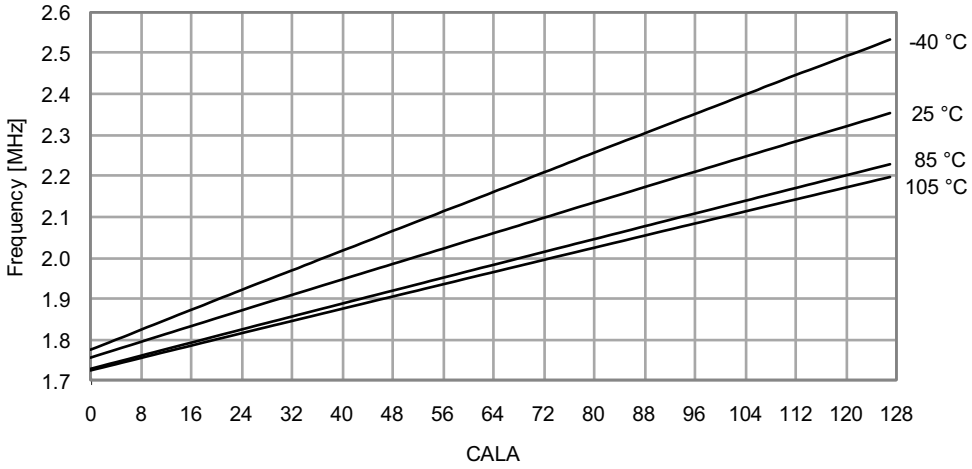


Figure 36-58. 2MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3V



38. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

38.1 8361G – 06/2015

1.	Updated “Packaging Information” on page 63. Replaced the “64Z3” on page 64 drawing by a correct drawing.

38.2 8361F – 11/2014

1.	Updated according to the template

38.3 8361E – 07/2014

1.	Updated “Ordering Information” on page 2. Ordering codes added for ATxmega384C3 @ 105°C
2.	Updated Table 35-4 on page 67. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled.
3.	Updated Table on page 75. Updated the table to include values for T=85°C and T=105°C. Removed T=55°C.
4.	TWI electrical characteristics: Units of Data setup time ($t_{SU;DAT}$) changed from µs to ns in Table 35-28 on page 83.
5.	“Typical Characteristics” on page 85: Added 105°C characteristics.
6.	Added info on ESR parameter for 16 MHz crystal oscillator and XOSC characteristics in Table on page 78.
7.	Changed Vcc to AV_{CC} in Section 28. “ADC – 12-bit Analog to Digital Converter” on page 46 and Section 29. “AC – Analog Comparator” on page 48.

38.4 8361D – 07/2013

1.	Errata **Temperature sensor not calibrated** added to “Rev. B” on page 119

38.5 8361C – 04/2012

1.	Updated four plots in typical characteristics: Figures 36-1 and Figure 36-2 on page 85; Figures 36-8 and Figure 36-3 on page 86.

38.6 8361B – 03/2012

1.	Editing update.
2.	Atmel new datasheet template used.