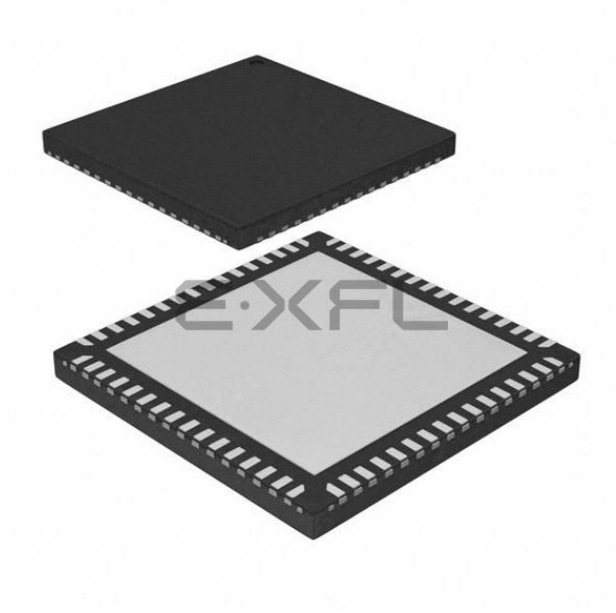

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What is "Embedded - Microcontrollers"?

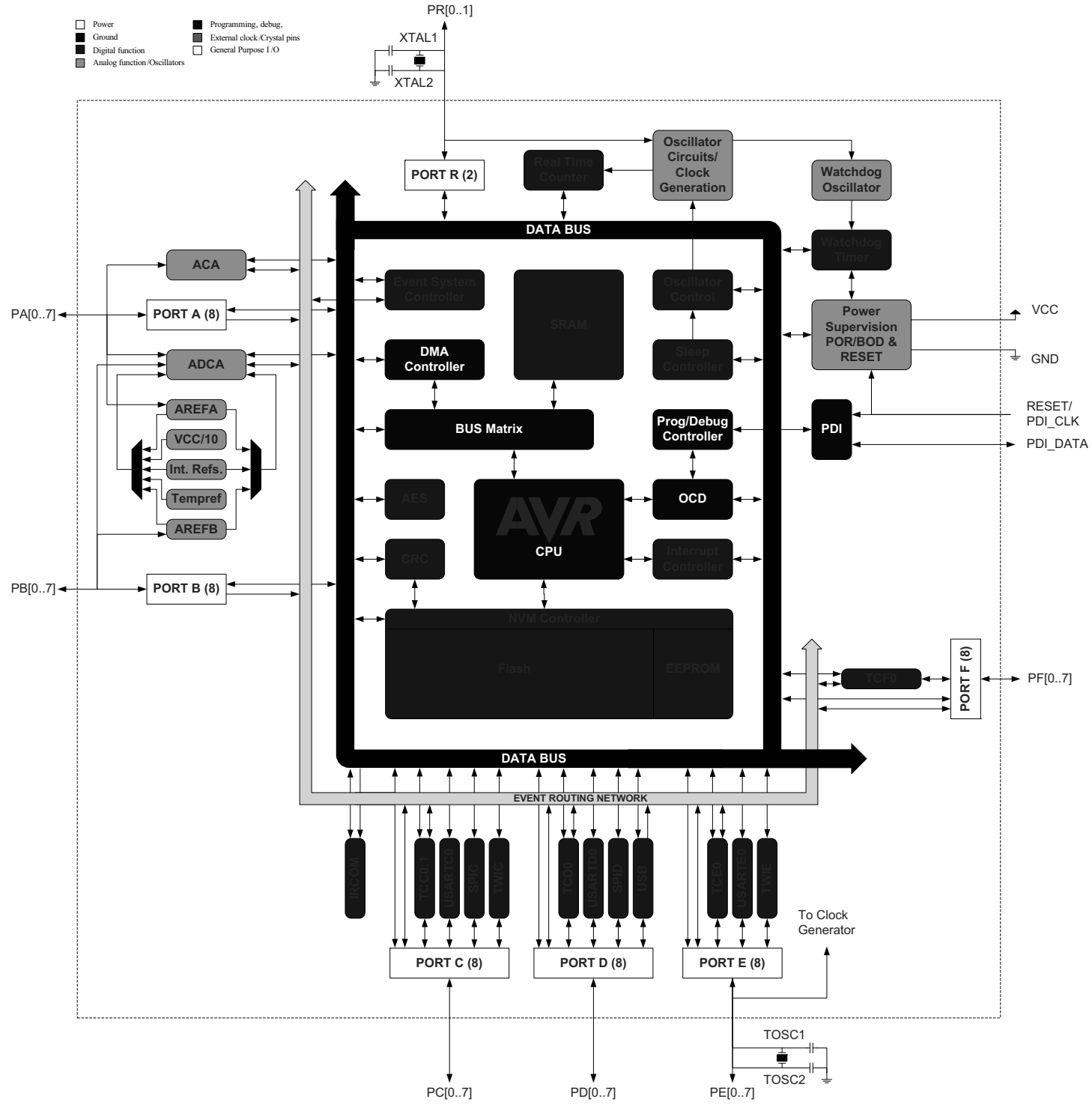
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega384c3-mn

3.1 Block Diagram

Figure 3-1. XMEGA C3 Block Diagram



4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on www.atmel.com/avr.

4.1 Recommended Reading

- Atmel AVR XMEGA C manual
- XMEGA application notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA C manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentation are available from www.atmel.com/avr.

10. System Clock and Clock Options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal oscillators:**
  - **32MHz run-time calibrated and tuneable oscillator**
  - **2MHz run-time calibrated oscillator**
  - **32.768kHz calibrated oscillator**
  - **32kHz ultra low power (ULP) oscillator with 1kHz output**
- **External clock options**
  - **0.4MHz - 16MHz crystal oscillator**
  - **32.768kHz crystal oscillator**
  - **External clock**
- **PLL with 20MHz - 128MHz output frequency**
  - **Internal and external clock options and 1x to 31x multiplication**
  - **Lock detector**
- **Clock prescalers with 1x to 2048x division**
- **Fast peripheral clocks running at two and four times the CPU clock**
- **Automatic run-time calibration of internal oscillators**
- **External oscillator and PLL lock failure detection with optional non-maskable interrupt**

10.2 Overview

Atmel AVR XMEGA C3 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 10-1 on page 19 presents the principal clock system. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 21.

12.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

12.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

12.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see “WDT – Watchdog Timer” on page 25.

12.4.5 Software Reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register. The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

12.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

15. I/O Ports

15.1 Features

- **50 general purpose input and output pins with individual configuration**
- **Output driver with configurable driver and pull settings:**
  - **Totem-pole**
  - **Wired-AND**
  - **Wired-OR**
  - **Bus-keeper**
  - **Inverted I/O**
- **Input with synchronous and/or asynchronous sensing with interrupts and events**
  - **Sense both edges**
  - **Sense rising edges**
  - **Sense falling edges**
  - **Sense low level**
- **Optional pull-up and pull-down resistor on input and Wired-OR/AND configurations**
- **Optional slew rate control**
- **Asynchronous pin change sensing that can wake the device from all sleep modes**
- **Two port interrupts with pin masking per I/O port**
- **Efficient and safe access to port pins**
  - **Hardware read-modify-write through dedicated toggle/clear/set registers**
  - **Configuration of multiple pins in a single operation**
  - **Mapping of port registers into bit-accessible I/O memory space**
- **Peripheral clocks output on port pin**
- **Real-time counter clock output to port pin**
- **Event channels can be output on port pin**
- **Remapping of digital peripheral pin functions**
  - **Selectable USART, SPI, and timer/counter input/output pin locations**

15.2 Overview

One port consists of up to eight port pins: pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement synchronous and asynchronous input sensing with interrupts and events for selectable pin change conditions. Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, included the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in a single operation. The pins have hardware read-modify-write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

The port pin configuration also controls input and output selection of other device functions. It is possible to have both the peripheral clock and the real-time clock output to a port pin, and available for external use. The same applies to events from the event system that can be used to synchronize and control external functions. Other digital peripherals, such as USART, SPI, and timer/counters, can be remapped to selectable pin locations in order to optimize pin-out versus application needs.

The notation of the ports are PORTA, PORTB, PORTC, PORTD, PORTE, PORTF, and PORTR.

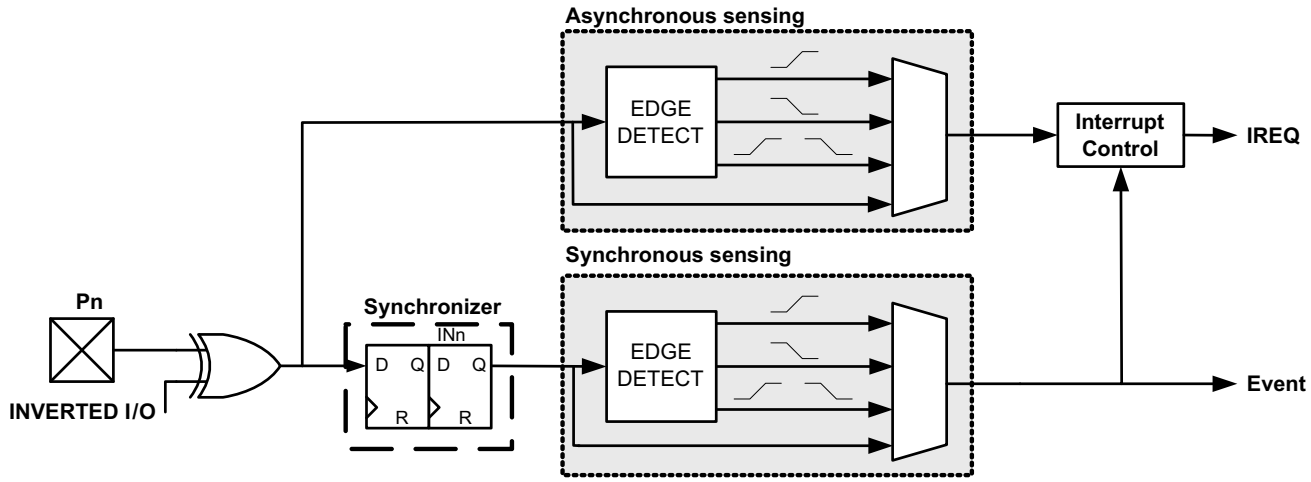
15.3 Output Driver

All port pins (Pn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

15.4 Input Sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7.

Figure 15-7. Input Sensing System Overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

15.5 Alternate Port Functions

Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. “Pinout and Pin Functions” on page 51 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

20. RTC – 16-bit Real-Time Counter

20.1 Features

- **16-bit resolution**
- **Selectable clock source**
  - **32.768kHz external crystal**
  - **External clock**
  - **32.768kHz internal oscillator**
  - **32kHz internal ULP oscillator**
- **Programmable 10-bit clock prescaling**
- **One compare register**
- **One period register**
- **Clear counter on period overflow**
- **Optional interrupt/event on overflow and compare match**

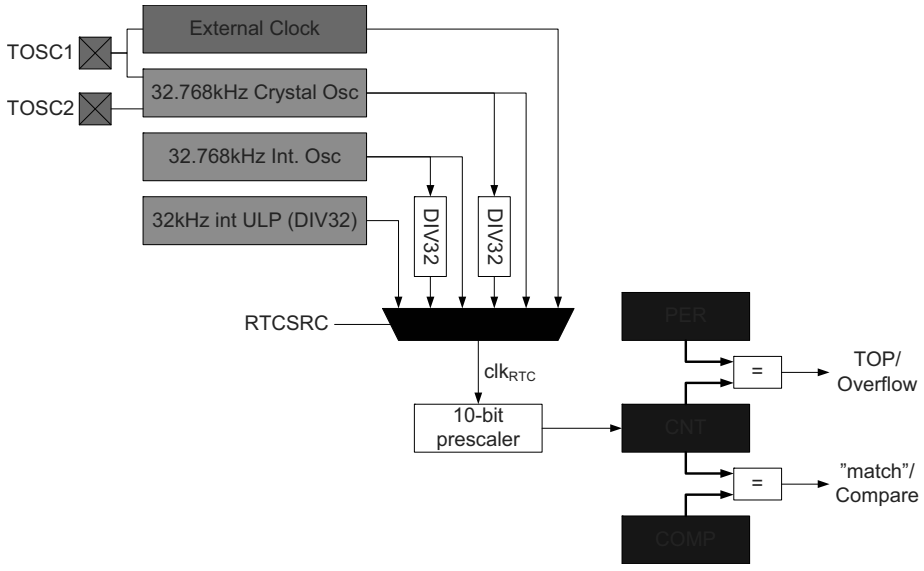
20.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 20-1. Real-time Counter Overview



For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

31.1.5 Communication Functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI
D-	Data- for USB
D+	Data+ for USB

31.1.6 Oscillators, Clock, and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel Output
RTCOUT	RTC Clock Source Output

31.1.7 Debug/System Functions

RESET	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

35.11 Power-on Reset Characteristics

Table 35-16. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled $V_{POT-} = V_{POT+}$.

35.12 Flash and EEPROM Memory Characteristics

Table 35-17. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 35-18. Programming Time

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip erase(2)	384KB Flash, EEPROM		130		ms
	Flash	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

35.15 Two-Wire Interface Characteristics

Table 35-28 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 35-7.

Figure 35-7. Two-wire Interface Bus Timing

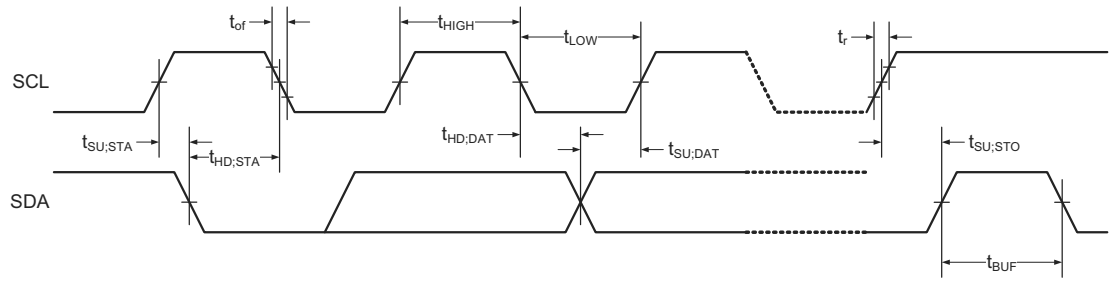


Table 35-28. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		0.5		$0.3V_{CC}$	
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	0.6			

36.1.3 Power-down Mode Supply Current

Figure 36-15.Power-down Mode Supply Current vs. V_{CC}

All functions disabled

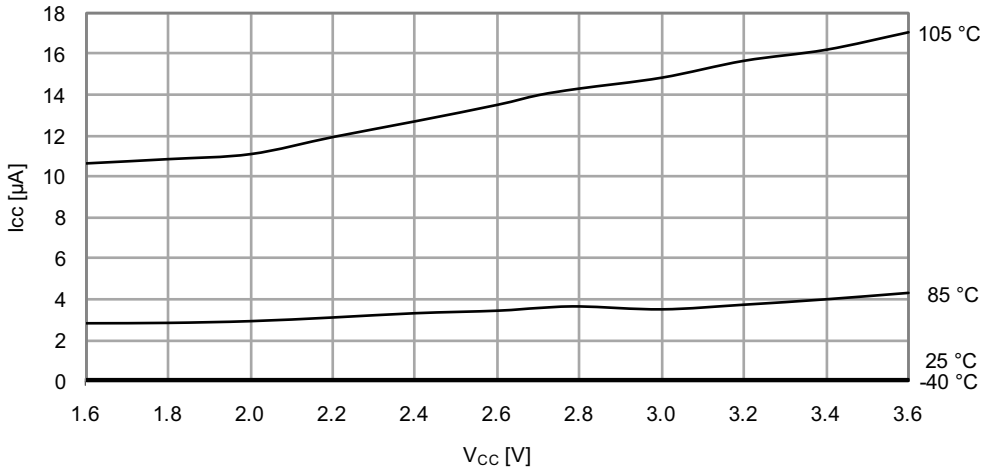


Figure 36-16.Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled

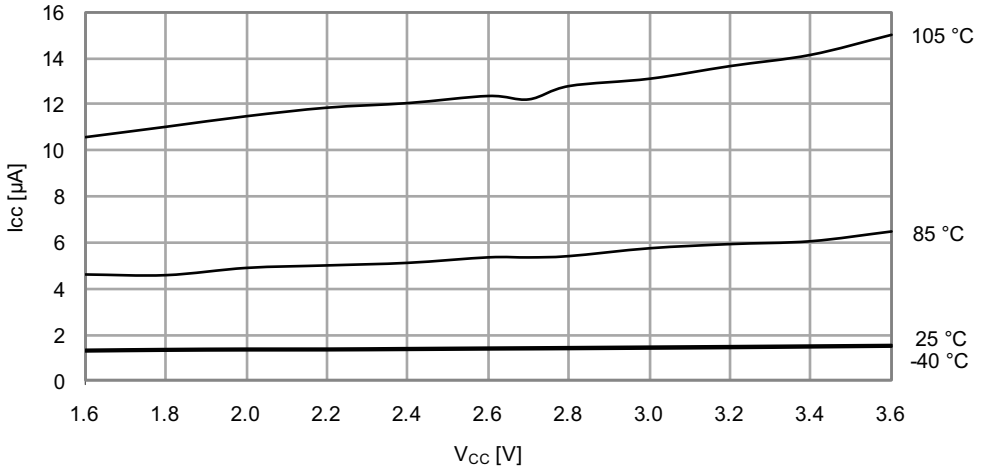


Figure 36-25.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V

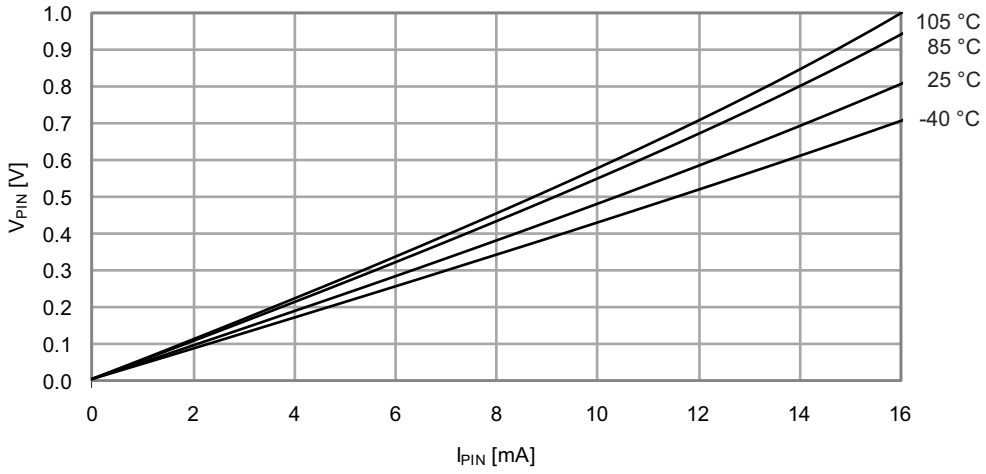


Figure 36-26.I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V

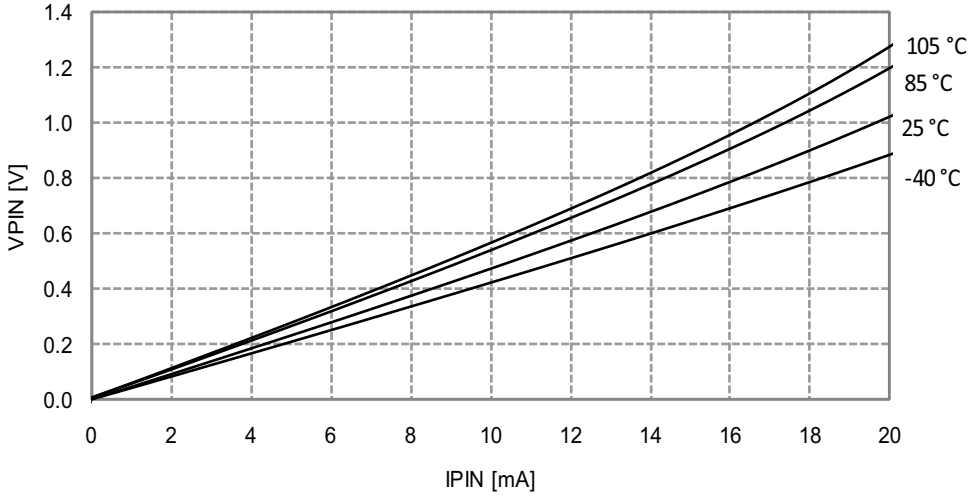


Figure 36-49.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 1.8V

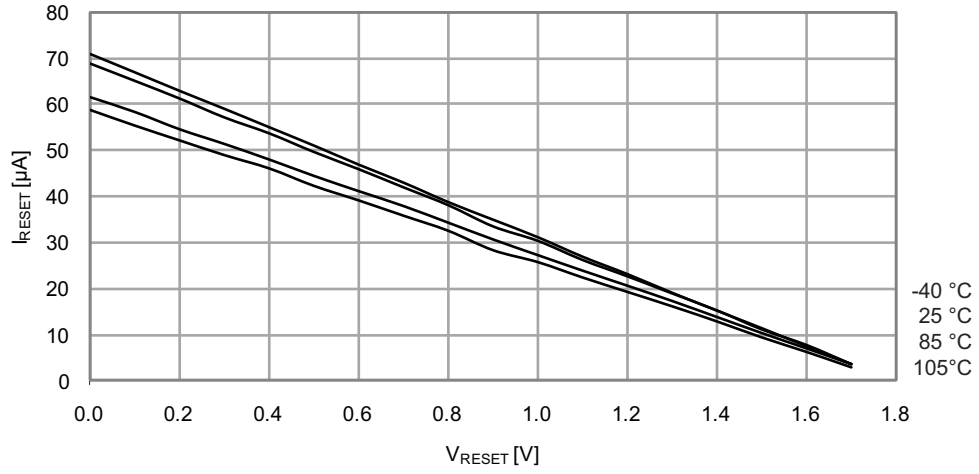
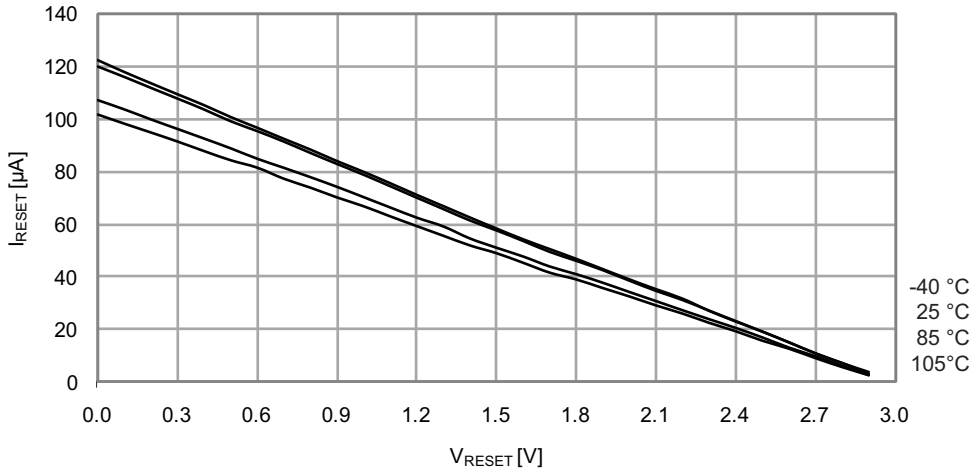


Figure 36-50.Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

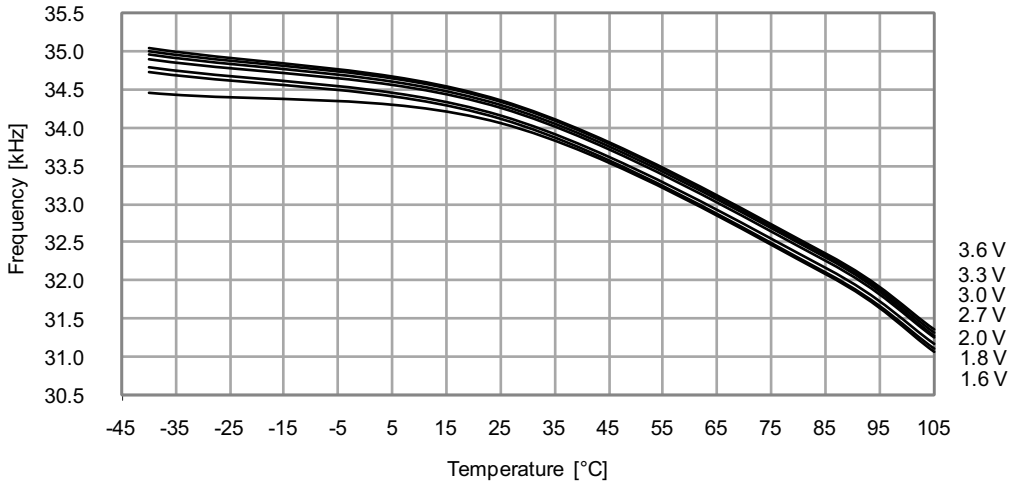
V_{CC} = 3.0V



36.8 Oscillator Characteristics

36.8.1 Ultra Low-Power Internal Oscillator

Figure 36-53. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



36.8.2 32.768kHz Internal Oscillator

Figure 36-54. 32.768kHz Internal Oscillator Frequency vs. Temperature

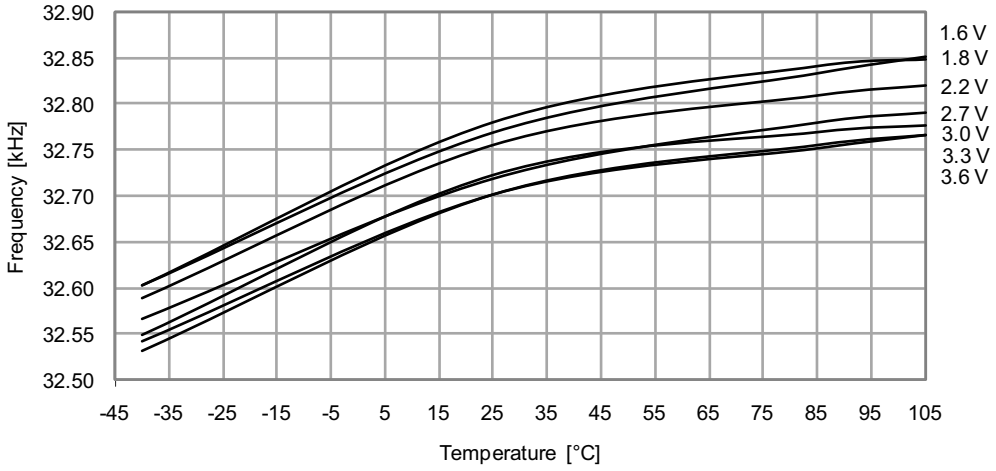
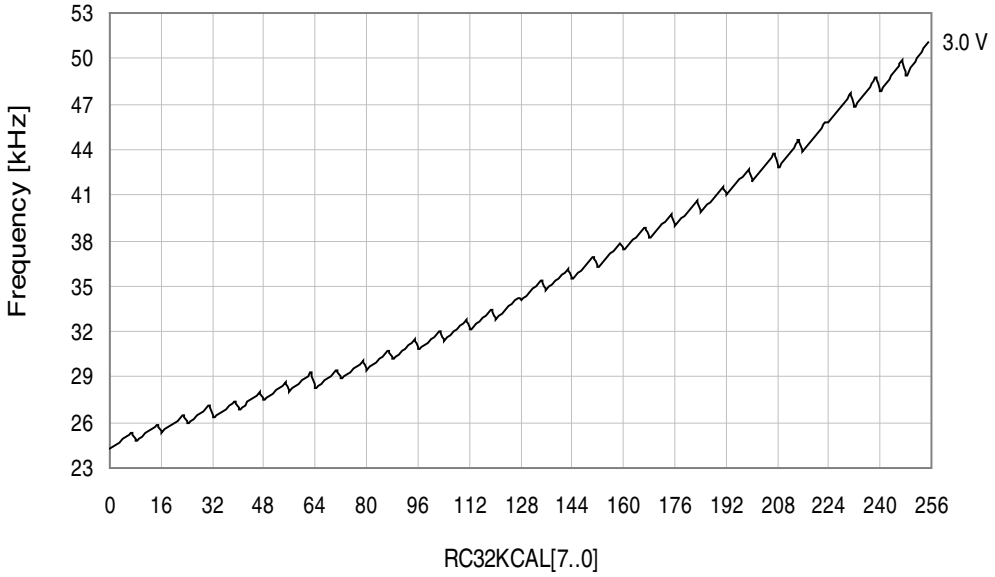


Figure 36-55. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

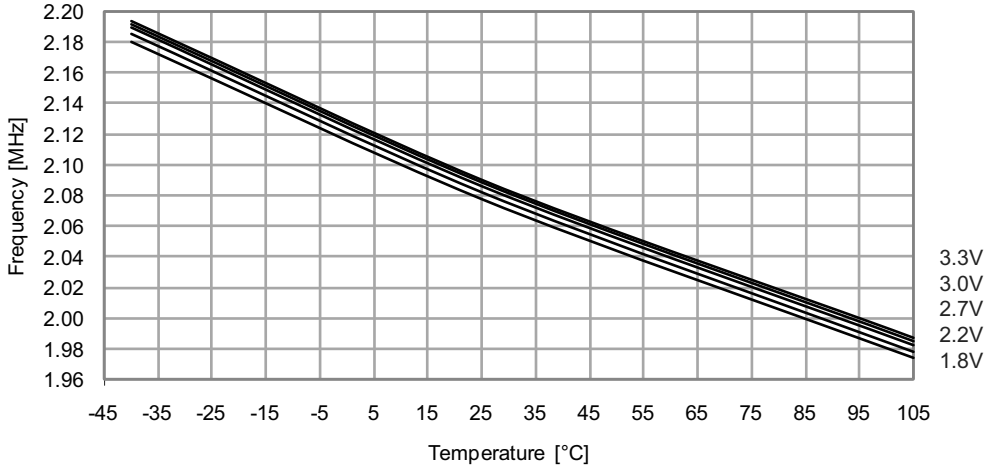
V_{CC} = 3.0V, T = 25°C



36.8.3 2MHz Internal Oscillator

Figure 36-56. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



36.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 36-63. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

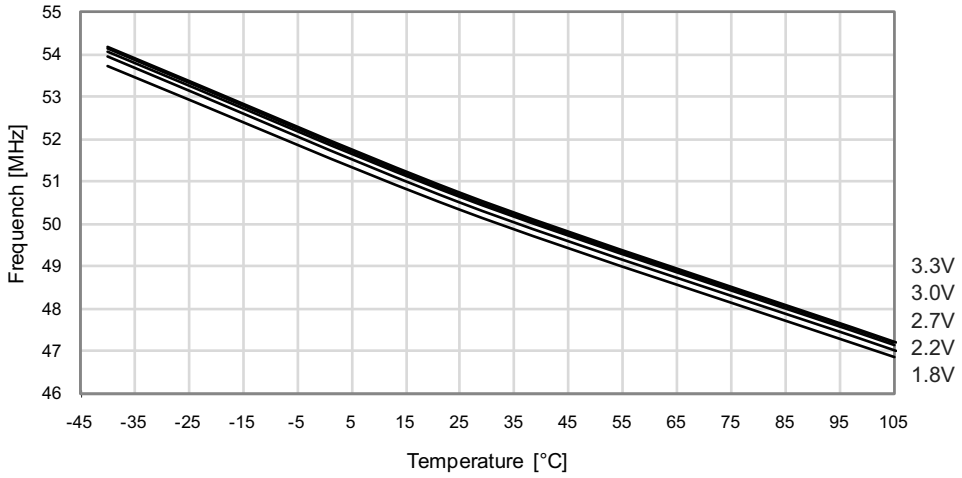
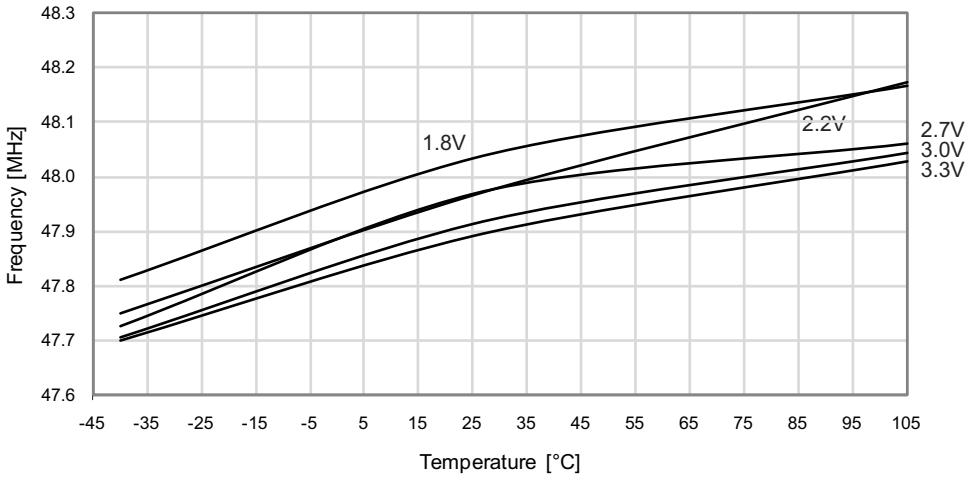


Figure 36-64. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator



38. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

38.1 8361G – 06/2015

1.	Updated “Packaging Information” on page 63. Replaced the “64Z3” on page 64 drawing by a correct drawing.

38.2 8361F – 11/2014

1.	Updated according to the template

38.3 8361E – 07/2014

1.	Updated “Ordering Information” on page 2. Ordering codes added for ATxmega384C3 @ 105°C
2.	Updated Table 35-4 on page 67. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled.
3.	Updated Table on page 75. Updated the table to include values for T=85°C and T=105°C. Removed T=55°C.
4.	TWI electrical characteristics: Units of Data setup time ($t_{SU;DAT}$) changed from µs to ns in Table 35-28 on page 83.
5.	“Typical Characteristics” on page 85: Added 105°C characteristics.
6.	Added info on ESR parameter for 16 MHz crystal oscillator and XOSC characteristics in Table on page 78.
7.	Changed Vcc to AV_{CC} in Section 28. “ADC – 12-bit Analog to Digital Converter” on page 46 and Section 29. “AC – Analog Comparator” on page 48.

38.4 8361D – 07/2013

1.	Errata **Temperature sensor not calibrated** added to “Rev. B” on page 119

38.5 8361C – 04/2012

1.	Updated four plots in typical characteristics: Figures 36-1 and Figure 36-2 on page 85; Figures 36-8 and Figure 36-3 on page 86.

38.6 8361B – 03/2012

1.	Editing update.
2.	Atmel new datasheet template used.

38.7 8361A – 02/2012

1. Initial revision.