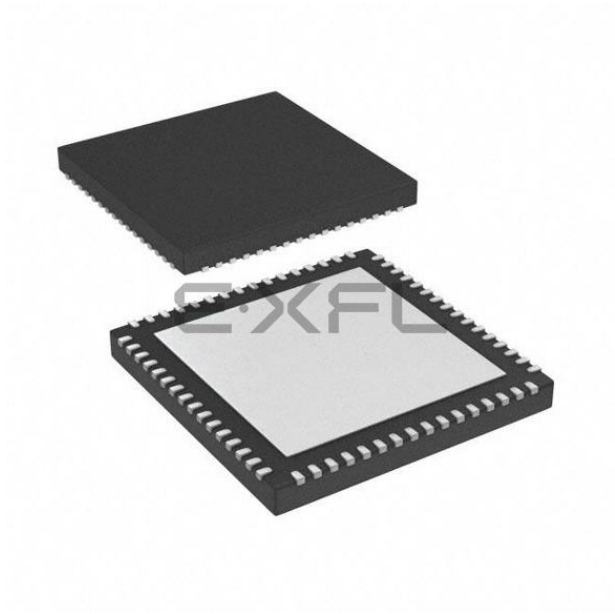

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 45x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19195-i-mr

4.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of an FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that read the program memory via the FSR require one extra instruction cycle to complete. Example 4-2 demonstrates reading the program memory via an FSR.

The HIGH directive will set bit 7 if a label points to a location in the program memory. This applies to the assembly code Example 4-2 shown below.

EXAMPLE 4-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0        ;Index0 data
    RETLW DATA1        ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

4.2 Memory Access Partition (MAP)

User Flash is partitioned into:
- Application Block
- Boot Block, and
- Storage Area Flash (SAF) Block

The user can allocate the memory usage by setting the $\overline{\text{BBEN}}$ bit, selecting the size of the partition defined by BBSIZE<2:0> bits and enabling the Storage Area Flash by the $\overline{\text{SAFEN}}$ bit of the Configuration Word (see Register 5-4). Refer to Table 4-2 for the different user Flash memory partitions.

4.2.1 APPLICATION BLOCK

Default settings of the Configuration bits ($\overline{\text{BBEN}}$ = 1 and $\overline{\text{SAFEN}}$ = 1) assign all memory in the user Flash area to the Application Block.

4.2.2 BOOT BLOCK

If $\overline{\text{BBEN}}$ = 1, the Boot Block is enabled and a specific address range is alloted as the Boot Block based on the value of the BBSIZE bits of Configuration Word (Register 5-4) and the sizes provided in Table 5-1.

4.2.3 STORAGE AREA FLASH

Storage Area Flash (SAF) is enabled by clearing the $\overline{\text{SAFEN}}$ bit of the Configuration Word in Register 5-4. If enabled, the SAF block is placed at the end of memory and spans 128 words. If the Storage Area Flash (SAF) is enabled, the SAF area is not available for program execution.

4.2.4 MEMORY WRITE PROTECTION

All the memory blocks have corresponding write protection fuses WRTAPP and WRTB bits in the Configuration Word (Register 5-4). If write-protected locations are written from NVMCON registers, memory is not changed and the WRERR bit defined in Register 12-5 is set as explained in **Section 13.4.9 “WRERR Bit”**.

4.2.5 MEMORY VIOLATION

A Memory Execution Violation Reset occurs while executing an instruction that has been fetched from outside a valid execution area, clearing the $\overline{\text{MEMV}}$ bit. Refer to **Section 8.13 “Memory Execution Violation”** for the available valid program execution areas and the PCON1 register definition (Register 8-3) for $\overline{\text{MEMV}}$ bit conditions.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19195/6/7 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 63 (Continued)											
1FD0h	—	Unimplemented								---- ----	---- ----
1FD1h	—	Unimplemented								---- ----	---- ----
1FD2h	—	Unimplemented								---- ----	---- ----
1FD3h	—	Unimplemented								---- ----	---- ----
1FD4h	—	Unimplemented								---- ----	---- ----
1FD5h	—	Unimplemented								---- ----	---- ----
1FD6h	—	Unimplemented								---- ----	---- ----
1FD7h	—	Unimplemented								---- ----	---- ----
1FD8h	—	Unimplemented								---- ----	---- ----
1FD9h	—	Unimplemented								---- ----	---- ----
1FDAh	—	Unimplemented								---- ----	---- ----
1FDBh	—	Unimplemented								---- ----	---- ----
1FDCh	—	Unimplemented								---- ----	---- ----
1FDDh	—	Unimplemented								---- ----	---- ----
1FDEh	—	Unimplemented								---- ----	---- ----
1FDFh	—	Unimplemented								---- ----	---- ----
1FE0h	—	Unimplemented								---- ----	---- ----
1FE1h	—	Unimplemented								---- ----	---- ----
1FE2h	—	Unimplemented								---- ----	---- ----
1FE3h	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

5.0 DEVICE CONFIGURATION

Device configuration consists of the Configuration Words, User ID, Device ID, Device Information Area (DIA), (see **Section 6.0 "Device Information Area"**), and the Device Configuration Information (DCI) regions, (see **Section 7.0 "Device Configuration Information"**).

5.1 Configuration Words

The devices have several Configuration Words starting at address 8007h. The Configuration bits establish configuration values prior to the execution of any software; Configuration bits enable or disable device-specific features.

In terms of programming, these important Configuration bits should be considered:

1. LVP: Low-Voltage Programming Enable bit

- 1 = ON – Low-Voltage Programming is enabled. $\overline{MCLR}$/V_{PP} pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
- 0 = OFF – HV on $\overline{MCLR}$/V_{PP} must be used for programming.

2. CP: User Nonvolatile Memory (NVM) Program Memory Code Protection bit

- 1 = OFF – User NVM code protection disabled
- 0 = ON – User NVM code protection enabled

13.4.9 WRERR BIT

The WRERR bit can be used to determine if a write error occurred.

WRERR will be set if one of the following conditions occurs:

- If WR is set while the NVMADRH:NMVADRL points to a write-protected address
- A Reset occurs while a self-write operation was in progress
- An unlock sequence was interrupted

The WRERR bit is normally set by hardware, but can be set by the user for test purposes. Once set, WRERR must be cleared in software.

TABLE 13-4: ACTIONS FOR PFM WHEN WR = 1

Free	LWLO	Actions for PFM when WR = 1	Comments
1	x	Erase the 32-word row of NVMADRH:NVMADRL location. See **Section 13.4.4 "NVMREG Erase of PFM"**	• If WP is enabled, WR is cleared and WRERR is set • All 32 words are erased • NVMDATH:NVMDATL is ignored
0	1	Copy NVMDATH:NVMDATL to the write latch corresponding to NVMADR LSBs. See **Section 13.4.4 "NVMREG Erase of PFM"**	• Write protection is ignored • No memory access occurs
0	0	Write the write-latch data to PFM row. See **Section 13.4.4 "NVMREG Erase of PFM"**	• If WP is enabled, WR is cleared and WRERR is set • Write latches are reset to 3FFh • NVMDATH:NVMDATL is ignored

REGISTER 13-6: NVMCON2: NONVOLATILE MEMORY CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
NVMCON2<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **NVMCON2<7:0>:** Flash Memory Unlock Pattern bits

To unlock writes, a 55h must be written first followed by an AAh before setting the WR bit of the NVMCON1 register. The value written to this register is used to unlock the writes.

TABLE 13-5: SUMMARY OF REGISTERS ASSOCIATED WITH NONVOLATILE MEMORY (NVM)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	147
PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	155
PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	164
NVMCON1	—	NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD	200
NVMCON2	NVMCON2<7:0>								201
NVMADRL	NVMADR<7:0>								199
NVMADRH	—(1)	NVMADR<14:8>							199
NVMDATL	NVMDAT<7:0>								199
NVMDATH	—	—	NVMDAT<13:8>						199

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by NVM.

Note 1: Unimplemented, read as '1'.

REGISTER 14-20: WPUC: WEAK PULL-UP PORTC REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUC<7:0>**: Weak Pull-up Register bits(1)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 14-21: ODCONC: PORTC OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODCC<7:0>:** PORTC Open-Drain Enable bits
For RC<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 14-22: SLRCONC: PORTC SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SLRC<7:0>:** PORTC Slew Rate Enable bits
For RC<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

20.0 TEMPERATURE INDICATOR MODULE (TIM)

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The main purpose of the temperature indicator module is to provide temperature-dependent voltage that can be measured by the Analog-to-Digital Converter.

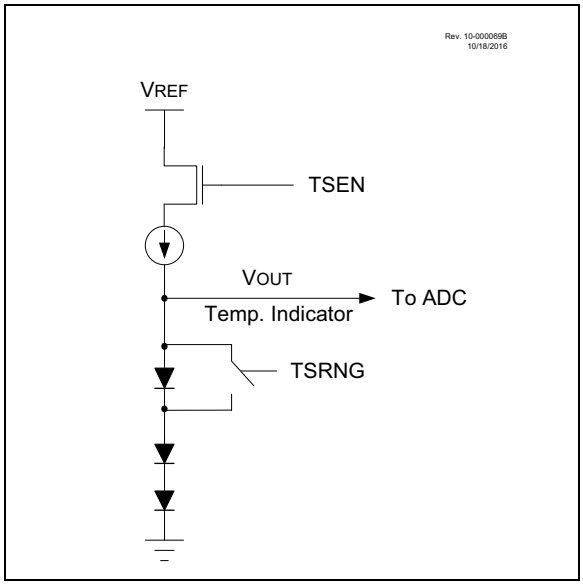
The circuit's range of operating temperature falls between -40°C and +125°C. The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately.

20.1 Module Operation

The temperature indicator module consists of a temperature-sensing circuit that provides a voltage to the device ADC. The analog voltage output, VTSENSE, varies inversely to the device temperature. The output of the temperature indicator is referred to as VOUT.

Figure 20-1 shows a simplified block diagram of the temperature indicator module.

FIGURE 20-1: TEMPERATURE CIRCUIT DIAGRAM



The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 19.0 "Analog-to-Digital Converter with Computation (ADC2) Module"** for detailed information.

The ON/OFF bit for the module is located in the FVRCON register. See **Section 18.0 "Fixed Voltage Reference (FVR)"** for more information. The circuit is enabled by setting the TSEN bit of the FVRCON register. When the module is disabled, the circuit draws no current.

The circuit operates in either High or Low range. Refer to **Section 20.5 "Temperature Indicator Range"** for more details on the range settings.

20.2 Estimation of Temperature

This section describes how the sensor voltage can be used to estimate the temperature of the module. To use the sensor, the output voltage, VTSENSE, is measured and the corresponding temperature is determined. Equation 20-1 provides an estimate for the die temperature based on the VTSENSE value.

EQUATION 20-1: SENSOR TEMPERATURE

$$T_{SENSE} = V_{TSENSE} \times (-Mt) + T_{OFFSET}$$

Where:
Mt = 1/Mv, where Mv = sensor voltage sensitivity (V/°C).
TOFFSET is the temperature difference between the theoretical temperature and the actual temperature.

20.4 Minimum Operating VDD

When the temperature circuit is operated in Low range, the device may be operated at any operating voltage that is within specifications. When the temperature circuit is operated in High range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 20-1 shows the recommended minimum VDD vs. Range setting.

TABLE 20-1: RECOMMENDED VDD vs. RANGE

Min.VDD, TSRNG = 1 (High Range)	Min. VDD, TSRNG = 0 (Low Range)
≥ 2.5	≥ 1.8

20.5 Temperature Indicator Range

The temperature indicator circuit operates in either High or Low range. The High range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range. High range requires a higher-bias voltage to operate and thus, a higher VDD is needed. The Low range is selected by clearing the TSRNG bit of the FVRCON register. The Low range generates a lower sensor voltage and thus, a lower VDD voltage is needed to operate the circuit.

The output voltage of the sensor is the highest value at -40°C and the lowest value at +125°C.

- **High Range:** The High range is used in applications with the reference for the ADC, VREF = 2.048V. This range may not be suitable for battery-powered applications.
- **Low Range:** This mode is useful in applications in which the VDD is too low for high-range operation. The VDD in this mode can be as low as 1.8V. VDD must, however, be at least 0.5V higher than the maximum sensor voltage depending on the expected low operating temperature.

20.6 DIA Information

DIA data provide ADC readings at one operating temperature. DIA data is taken during factory testing and stored within the device. The 90°C reading alone allows single-point calibration as described in Section 20.2.1, Calibration, by solving Equation 20-1 for TOFFSET.

Refer to **Section 6.0 "Device Information Area"** for more information on the data stored in the DIA and how to access them.

Note:	The lower temperature range (e.g., - 40°C) will suffer in accuracy because temperature conversion must extrapolate below the reference points, amplifying any measurement errors.

TABLE 20-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		279

Legend: — = Unimplemented location, read as '0'. Shaded cells are unused by the temperature indicator module.

REGISTER 24-8: MINUTES(1): MINUTE VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINH<2:0>			MINL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINH<2:0>:** Binary Coded Decimal value of minutes '10' digit; valid values from 0 to 5

bit 3-0 **MINL<3:0>:** Binary Coded Decimal value of minutes '1' digit; valid values from 0 to 9

Note 1: Writes to the MINUTE registers are only allowed when RTCWREN = 1.

REGISTER 24-9: SECONDS(1): SECOND VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECH<2:0>			SECL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECH<2:0>:** Binary Coded Decimal value of seconds '10' digit; valid values from 0 to 5

bit 3-0 **SECL<3:0>:** Binary Coded Decimal value of seconds '1' digit; valid values from 0 to 9

Note 1: Writes to the SECOND registers are only allowed when RTCWREN = 1.

27.6 Timer2/4 Operation During Sleep

When PSYNC = 1, Timer2/4 cannot be operated while the processor is in Sleep mode. The contents of the TMR2 and T2PR registers will remain unchanged while processor is in Sleep mode.

When PSYNC = 0, Timer2/4 will operate in Sleep as long as the clock source selected is also still running. Selecting the LFINTOSC, MFINTOSC, or HFINTOSC oscillator as the timer clock source will keep the selected oscillator running during Sleep.

REGISTER 28-4: SMTxCLK: SMT CLOCK SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	CSEL<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **CSEL<2:0>:** SMT Clock Selection bits

111 = Reserved
110 = SOSC
101 = MFINTOSC/16 (31.25 kHz)
100 = MFINTOSC (500 kHz)
011 = LFINTOSC
010 = HFINTOSC
001 = FOSC
000 = FOSC/4

34.1.2.3 Receive Interrupts

The RXxIF interrupt flag bit of the PIR3 register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RXxIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RXxIF interrupts are enabled by setting all of the following bits:

- RXxIE, Interrupt Enable bit of the PIE3 register
- PEIE, Peripheral Interrupt Enable bit of the INTCON register
- GIE, Global Interrupt Enable bit of the INTCON register

The RXxIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

34.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCxSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCxREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCxSTA register which resets the EUSART. Clearing the CREN bit of the RCxSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive FIFO have framing errors, repeated reads of the RCxREG will not clear the FERR bit.

34.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCxSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCxSTA register or by resetting the EUSART by clearing the SPEN bit of the RCxSTA register.

34.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

34.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCxSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RXxIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

34.4.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

Note:	If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

34.4.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCxREG is read to access the FIFO. When this happens the OERR bit of the RCxSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCxREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

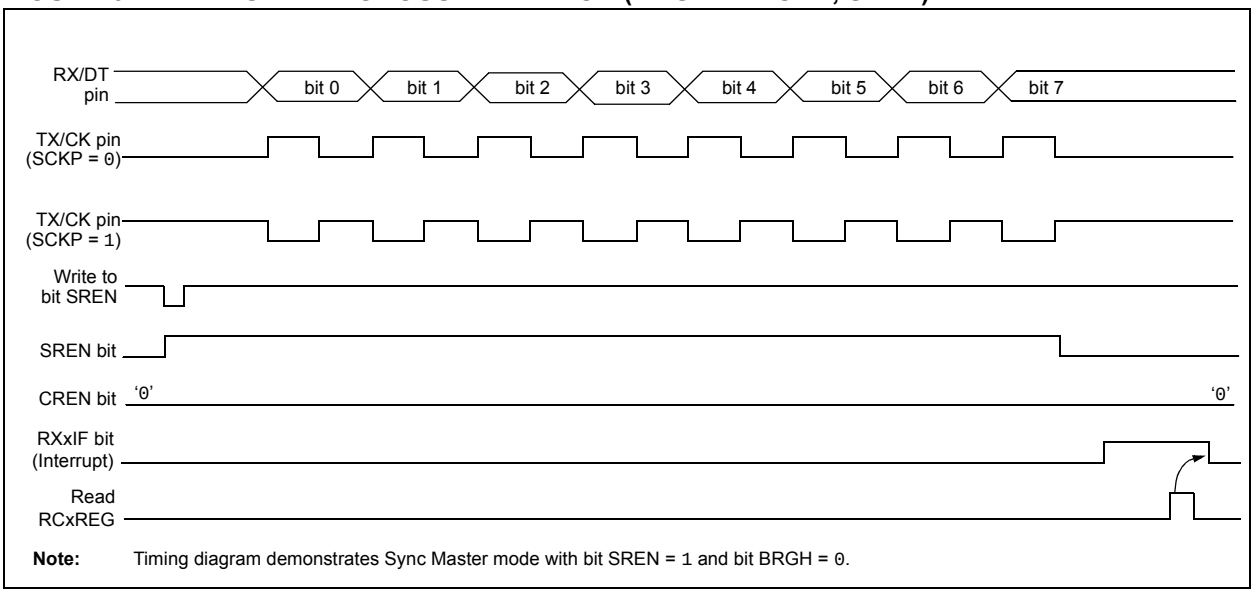
34.4.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

34.4.1.9 Synchronous Master Reception Set-up:

1. Initialize the SPxBRGH, SPxBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RXxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RXxIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RXxIE was set.
9. Read the RCxSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCxREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

FIGURE 34-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

35.8 LCD Multiplex Types

The LCD driver module can be configured into four multiplex types:

- Static (only COM0 used)
- 1/2 multiplex (COM0 and COM1 are used)
- 1/3 multiplex (COM0, COM1 and COM2 are used)
- 1/4 multiplex (COM0, COM1, COM2 and COM3 are used)
- 1/5 multiplex (COM0, COM1, COM2, COM3 and COM4 are used)
- 1/6 multiplex (COM0, COM1, COM2, COM3, COM4 and COM5 are used)
- 1/7 multiplex (COM0, COM1, COM2, COM3, COM4, COM5 and COM6 are used)
- 1/8 multiplex (COM0, COM1, COM2, COM3, COM4, COM5, COM6 and COM7 are used)

The LMUX<3:0> setting (LCDCON<3:0>) decides the function of the COM pins. (For details, see Table 35-6).

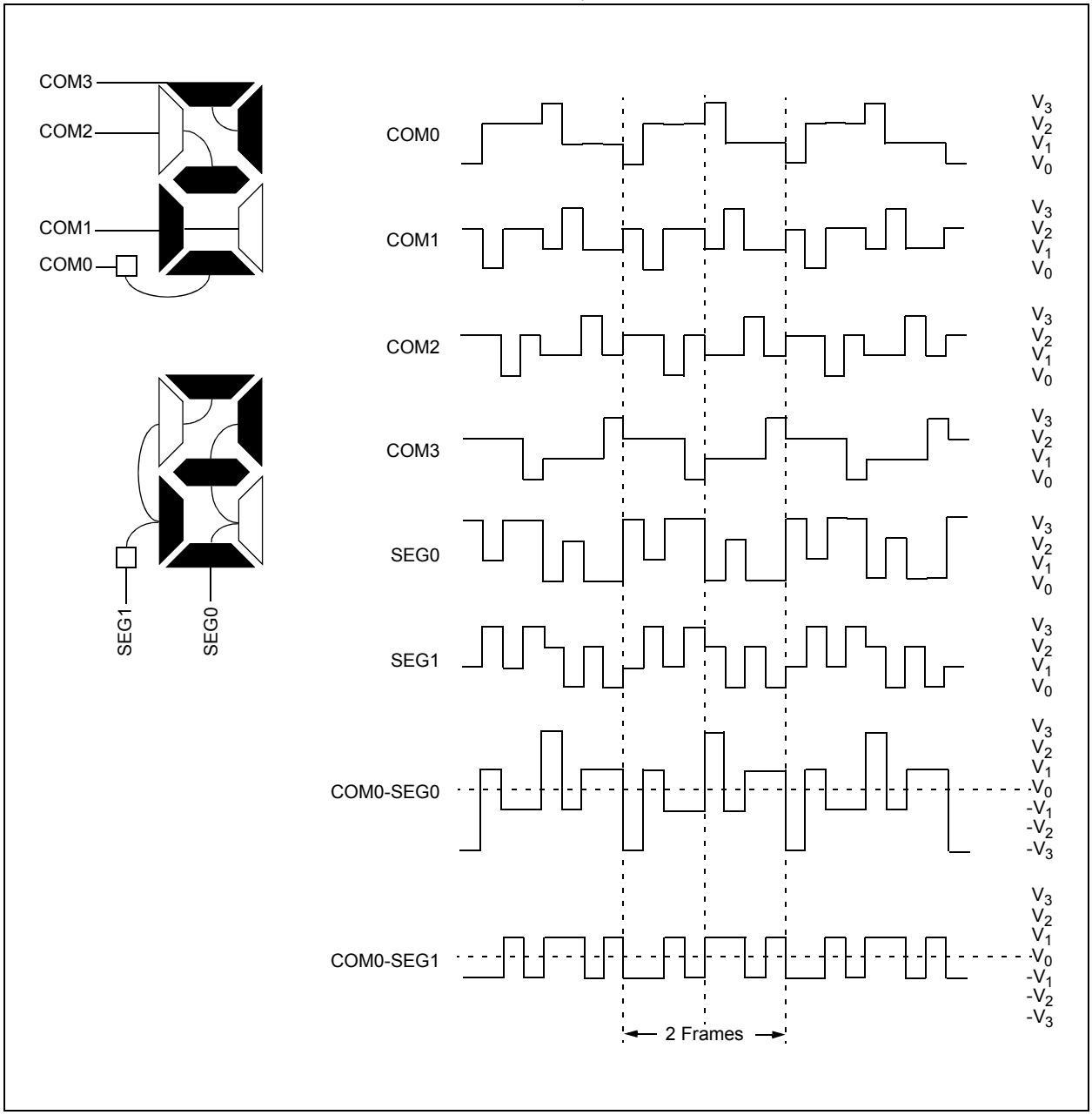
If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, the TRIS setting of that pin is overridden.

Note:	On a Power-on Reset, the LMUX<3:0> bits are '0000'.

TABLE 35-6: COM<7:0> PIN FUNCTIONS

LMUX<3:0>	COM7 Pin	COM6 Pin	COM5 Pin	COM4 Pin	COM3 Pin	COM2 Pin	COM1 Pin	COM0 Pin
1000	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
0111	I/O Pin	COM6	COM5	COM4	COM3	COM2	COM1	COM0
0110	I/O Pin	I/O Pin	COM5	COM4	COM3	COM2	COM1	COM0
0101	I/O Pin	I/O Pin	I/O Pin	COM4	COM3	COM2	COM1	COM0
0100	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM3	COM2	COM1	COM0
0011	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM2	COM1	COM0
0010	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM1	COM0
0001	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM0
0000	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin

FIGURE 35-18: TYPE-B WAVEFORMS IN 1/4 MUX, 1/3 BIAS DRIVE



REGISTER 35-1: LCDCON: LCD CONTROL REGISTER

R/W-0	R/W-0	HS/C-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDEN	SLPEN	WERR	CS	LMUX3	LMUX2	LMUX1	LMUX0
bit 7							bit 0

Legend:	C = Clearable bit	HS = Bit is set by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **LCDEN**: LCD Enable bit
1 = LCD module is enabled
0 = LCD module is disabled

bit 6 **SLPEN**: LCD Display Sleep-Enabled bit
1 = Module will stop driving in Sleep
0 = Module will continue driving in Sleep

bit 5 **WERR**: LCD Write Failed Error bit(1)
1 = Write failure to LCDDATA register occurred (must be reset in software)
0 = No LCD write error

bit 4 **CS**: Clock Source Select bit
1 = SOSC Selected
0 = LFINTOSC Selected

bit 3-0 **LMUX<3:0>**: Common Selection bits. Specifies the number of commons(2)

LMUX<3:0>	Multiplex	Bias
0000	All COMs off	—
0001	Static (COM0)	Static
0010	1/2 MUX (COM<1:0>)	1/2
0011	1/3 MUX (COM<2:0>)	1/3
0100	1/4 MUX (COM<3:0>)	1/3
0101	1/5 MUX (COM<4:0>)	1/3
0110	1/6 MUX (COM<5:0>)	1/3
0111	1/7 MUX (COM<6:0>)	1/3
1000	1/8 MUX (COM<7:0>)	1/3

Note 1: Bit can only be set by hardware and only cleared in software by writing to zero.
2: Cannot be changed when LCDEN = 1.

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19195/6/7 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
30Ch	CCPR1L	RL								454
30Dh	CCPR1H	RH								455
30Eh	CCP1CON	CCP1EN	—	CCP1OUT	CCP1FMT	CCP1MODE<3:0>				452
		—		—	—	CCP1-MODE3	CCP1-MODE2	CCP1-MODE1	CCP1MODE0	452
30Fh	CCP1CAP	CCP1CTS								454
		—	—	—	—	—	CCP1CTS2	CCP1CTS1	CCP1CTS0	454
310h	CCPR2L	RL								454
311h	CCPR2H	RH								455
312h	CCP2CON	CCP2EN	—	CCP2OUT	CCP2FMT	CCP2MODE<3:0>				452
		—		—	—	CCP2-MODE3	CCP2-MODE2	CCP2-MODE1	CCP2MODE0	452
313h	CCP2CAP	CCP2CTS								454
		—	—	—	—	—	CCP2CTS2	CCP2CTS1	CCP2CTS0	454
314h	PWM3DCL	PWM3DC<1:0>		—	—	—	—	—	—	462
		PWM3DC1	PWM3DC0	—	—	—	—	—	—	462
315h	PWM3DCH	PWM3DC								462
		PWM3DC9	PWM3DC8	PWM3DC7	PWM3DC6	PWM3DC5	PWM3DC4	PWM3DC3	PWM3DC2	462
316h	PWM3CON	PWM3EN	—	PWM3OUT	PWM3POL	—	—	—	—	461
317h	—	Unimplemented								461
318h	PWM4DCL	PWM4DC<1:0>		—	—	—	—	—	—	462
		PWM4DC1	PWM4DC0	—	—	—	—	—	—	462
319h	PWM4DCH	PWM4DC								462
		PWM4DC9	PWM4DC8	PWM4DC7	PWM4DC6	PWM4DC5	PWM4DC4	PWM4DC3	PWM4DC2	462
31Ah	PWM4CON	PWM4EN	—	PWM4OUT	PWM4POL	—	—	—	—	461
31Bh 31Fh	—	Unimplemented								
38Ch	—	Unimplemented								
38Dh	—	Unimplemented								
38Eh	—	Unimplemented								
38Fh	—	Unimplemented								
390h	—	Unimplemented								
391h	—	Unimplemented								
392h	—	Unimplemented								
393h	—	Unimplemented								
394h	—	Unimplemented								
395h	—	Unimplemented								
396h	—	Unimplemented								
397h	—	Unimplemented								
398h	—	Unimplemented								
399h	—	Unimplemented								
39Ah	—	Unimplemented								
39Bh	—	Unimplemented								
39Ch	—	Unimplemented								
39Dh	—	Unimplemented								
39Eh	—	Unimplemented								
39Fh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 39-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C

Param. No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	θJA	Thermal Resistance Junction to Ambient	48.3	°C/W	64-pin TQFP package
			28	°C/W	64-pin QFN package
TH02	θJC	Thermal Resistance Junction to Case	26.1	°C/W	64-pin TQFP package
			0.24	°C/W	64-pin QFN package
TH03	TJMAX	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD(1)
TH06	PI/O	I/O Power Dissipation	—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power	—	W	PDER = PDMAX (TJ - TA)/θJA(2)

Note 1: IDD is current to run the chip alone without driving any load on the output pins.
2: TA = Ambient Temperature, TJ = Junction Temperature

FIGURE 39-12: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

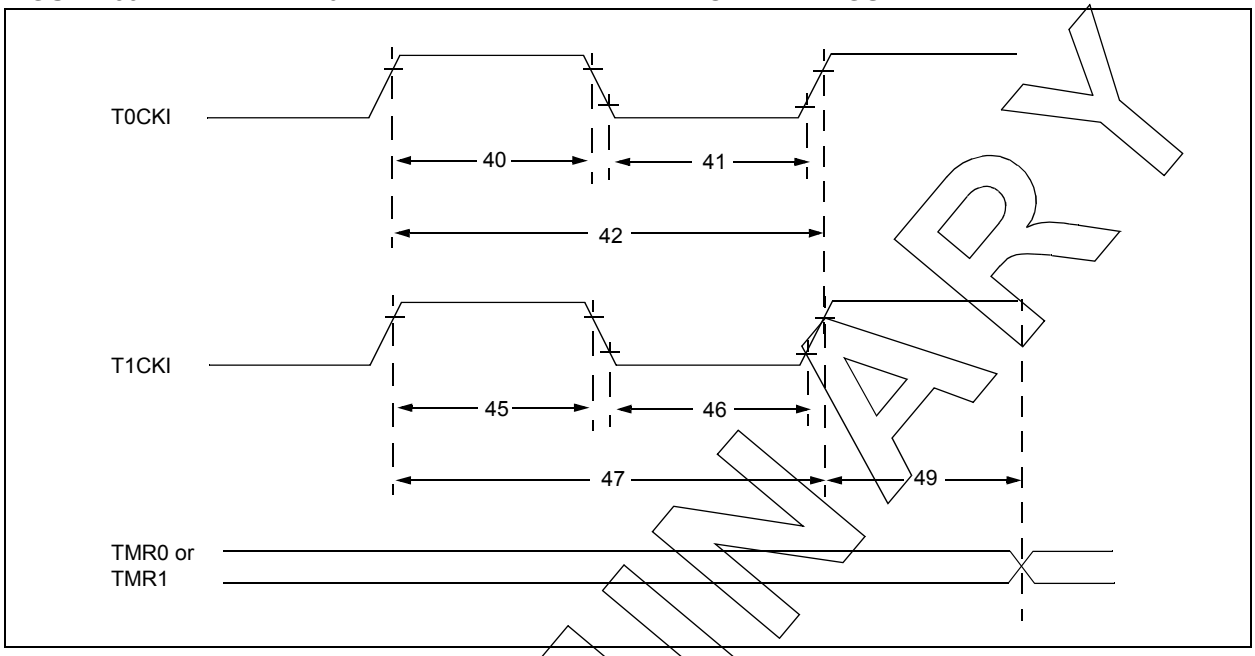


TABLE 39-19: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or TCY + 40 / N	—	—	ns	N = prescale value
			Asynchronous	60	—	—	ns	
48	FT1	Secondary Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		32.4	32.768	33.1	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 TOSC	—	7 TOSC	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 39-24: SPI MODE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
SP70*	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input	2.25*Tcy	—	—	ns	
SP71*	TscH	SCK input high time (Slave mode)	Tcy + 20	—	—	ns	
SP72*	TscL	SCK input low time (Slave mode)	Tcy + 20	—	—	ns	
SP73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	—	ns	
SP74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
SP75*	TdoR	SDO data output rise time	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP76*	TdoF	SDO data output fall time	—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}$↑ to SDO output high-impedance	10	—	50	ns	
SP78*	TscR	SCK output rise time (Master mode)	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP79*	TscF	SCK output fall time (Master mode)	—	10	25	ns	
SP80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	3.0V ≤ VDD ≤ 5.5V
			—	—	145	ns	1.8V ≤ VDD ≤ 5.5V
SP81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	1 Tcy	—	—	ns	
SP82*	TssL2doV	SDO data output valid after $\overline{SS}$↓ edge	—	—	50	ns	
SP83*	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK edge	1.5 Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.