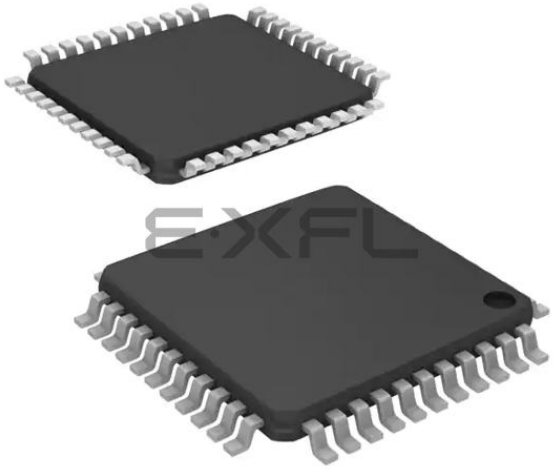

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 45x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19195-i-pt

TABLE 4-10: PIC16(L)F19195/6/7 MEMORY MAP, BANKS 58-63

	Bank 58		Bank 59		Bank 60		Bank 61		Bank 62		Bank 63
1D00h	Core Registers (Table 4-3)	1D80h	Core Registers (Table 4-3)	1E00h	Core Registers (Table 4-3)	1E80h	Core Registers (Table 4-3)	1F00h	Core Registers (Table 4-3)	1F80h	Core Registers (Table 4-3)
1D0Ch	LCDCON	1D8Ch	—	1E0Ch	—	1E8Ch	—	1F0Ch	—	1F8Ch	—
1D0Dh	LCDPS	1D8Dh	—	1E0Dh	—	1E8Dh	—	1F0Dh	—	1F8Dh	—
1D0Eh	LCDSE0	1D8Eh	—	1E0Eh	—	1E8Eh	—	1F0Eh	—	1F8Eh	—
1D0Fh	LCDSE1	1D8Fh	—	1E0Fh	CLCDATA	1E8Fh	PPSLOCK	1F0Fh	—	1F8Fh	—
1D10h	LCDSE2	1D90h	—	1E10h	CLC1CON	1E90h	INTPPS	1F10h	RA0PPS	1F90h	—
1D11h	LCDSE3	1D91h	—	1E11h	CLC1POL	1E91h	T0CKIPPS	1F11h	RA1PPS	1F91h	—
1D12h	LCDSE4	1D92h	—	1E12h	CLC1SEL0	1E92h	T1CKIPPS	1F12h	RA2PPS	1F92h	—
1D13h	LCDSE5	1D93h	—	1E13h	CLC1SEL1	1E93h	T1GPPS	1F13h	RA3PPS	1F93h	—
1D14h	LCDVCON1	1D94h	—	1E14h	CLC1SEL2	1E94h	—	1F14h	RA4PPS	1F94h	—
1D15h	LCDVCON2	1D95h	—	1E15h	CLC1SEL3	1E95h	—	1F15h	RA5PPS	1F95h	—
1D16h	LCDREF	1D96h	—	1E16h	CLC1GLS0	1E96h	—	1F16h	RA6PPS	1F96h	—
1D17h	LCDRL	1D97h	—	1E17h	CLC1GLS1	1E97h	—	1F17h	RA7PPS	1F97h	—
1D18h	LCDDATA0	1D98h	—	1E18h	CLC1GLS2	1E98h	—	1F18h	RB0PPS	1F98h	—
1D19h	LCDDATA1	1D99h	—	1E19h	CLC1GLS3	1E99h	—	1F19h	RB1PPS	1F99h	—
1D1Ah	LCDDATA2	1D9Ah	—	1E1Ah	CLC2CON	1E9Ah	—	1F1Ah	RB2PPS	1F9Ah	—
1D1Bh	LCDDATA3	1D9Bh	—	1E1Bh	CLC2POL	1E9Bh	—	1F1Bh	RB3PPS	1F9Bh	—
1D1Ch	LCDDATA4	1D9Ch	—	1E1Ch	CLC2SEL0	1E9Ch	T2AINPPS	1F1Ch	RB4PPS	1F9Ch	—
1D1Dh	LCDDATA5	1D9Dh	—	1E1Dh	CLC2SEL1	1E9Dh	T4AINPPS	1F1Dh	RB5PPS	1F9Dh	—
1D1Eh	LCDDATA6	1D9Eh	—	1E1Eh	CLC2SEL2	1E9Eh	—	1F1Eh	RB6PPS	1F9Eh	—
1D1Fh	LCDDATA7	1D9Fh	—	1E1Fh	CLC2SEL3	1E9Fh	—	1F1Fh	RB7PPS	1F9Fh	—
1D20h	LCDDATA8	1DA0h	—	1E20h	CLC2GLS0	1EA0h	—	1F20h	RC0PPS	1FA0h	—
1D21h	LCDDATA9	1DA1h	—	1E21h	CLC2GLS1	1EA1h	CCP1PPS	1F21h	RC1PPS	1FA1h	—
1D22h	LCDDATA10	1DA2h	—	1E22h	CLC2GLS2	1EA2h	CCP2PPS	1F22h	RC2PPS	1FA2h	—
1D23h	LCDDATA11	1DA3h	—	1E23h	CLC2GLS3	1EA3h	—	1F23h	RC3PPS	1FA3h	—
1D24h	LCDDATA12	1DA4h	—	1E24h	CLC3CON	1EA4h	—	1F24h	RC4PPS	1FA4h	—
1D25h	LCDDATA13	1DA5h	—	1E25h	CLC3POL	1EA5h	—	1F25h	RC5PPS	1FA5h	—
1D26h	LCDDATA14	1DA6h	—	1E26h	CLC3SEL0	1EA6h	—	1F26h	RC6PPS	1FA6h	—
1D27h	LCDDATA15	1DA7h	—	1E27h	CLC3SEL1	1EA7h	—	1F27h	RC7PPS	1FA7h	—
1D28h	LCDDATA16	1DA8h	—	1E28h	CLC3SEL2	1EA8h	—	1F28h	RD0PPS	1FA8h	—
1D29h	LCDDATA17	1DA9h	—	1E29h	CLC3SEL3	1EA9h	SMT1WINPPS	1F29h	RD1PPS	1FA9h	—
1D2Ah	LCDDATA18	1DAAh	—	1E2Ah	CLC3GLS0	1EAAh	SMT1SIGPPS	1F2Ah	RD2PPS	1FAAh	—
1D2Bh	LCDDATA19	1DABh	—	1E2Bh	CLC3GLS1	1EABh	—	1F2Bh	RD3PPS	1FABh	—
1D2Ch	LCDDATA20	1DACh	—	1E2Ch	CLC3GLS2	1EACh	—	1F2Ch	RD4PPS	1FACh	—
1D2Dh	LCDDATA21	1DADh	—	1E2Dh	CLC3GLS3	1EADh	—	1F2Dh	RD5PPS	1FADh	—
1D2Eh	LCDDATA22	1DAEh	—	1E2Eh	CLC4CON	1EAEh	—	1F2Eh	RD6PPS	1FAEh	—
1D2Fh	LCDDATA23	1DAFh	—	1E2Fh	CLC4POL	1EAFh	—	1F2Fh	RD7PPS	1FAFh	—
1D30h	LCDDATA24	1DB0h	—	1E30h	CLC4SEL0	1EB0h	—	1F30h	RE0PPS	1FB0h	—
1D31h	LCDDATA25	1DB1h	—	1E31h	CLC4SEL1	1EB1h	CWG1PPS	1F31h	RE1PPS	1FB1h	—
1D32h	LCDDATA26	1DB2h	—	1E32h	CLC4SEL2	1EB2h	—	1F32h	—	1FB2h	—
1D33h	LCDDATA27	1DB3h	—	1E33h	CLC4SEL3	1EB3h	—	1F33h	RE3PPS	1FB3h	—
1D34h	LCDDATA28	1DB4h	—	1E34h	CLC4GLS0	1EB4h	—	1F34h	RE4PPS	1FB4h	—
1D35h	LCDDATA29	1DB5h	—	1E35h	CLC4GLS1	1EB5h	—	1F35h	RE5PPS	1FB5h	—
1D36h	LCDDATA30	1DB6h	—	1E36h	CLC4GLS2	1EB6h	—	1F36h	RE6PPS	1FB6h	—
1D37h	LCDDATA31	1DB7h	—	1E37h	CLC4GLS3	1EB7h	—	1F37h	RE7PPS	1FB7h	—
1D38h	LCDDATA32	1DB8h	—	1E38h	RF0PPS	1EB8h	—	1F38h	ANSELA	1FB8h	—
1D39h	LCDDATA33	1DB9h	—	1E39h	RF1PPS	1EB9h	—	1F39h	WPUA	1FB9h	—
1D3Ah	LCDDATA34	1DBAh	—	1E3Ah	RF2PPS	1EBAh	—	1F3Ah	ODCONA	1FBAh	—
1D3Bh	LCDDATA35	1DBBh	—	1E3Bh	RF3PPS	1EBBh	CLCIN0PPS	1F3Bh	SLRCONA	1FBBh	—
1D3Ch	LCDDATA36	1DBCh	—	1E3Ch	RF4PPS	1EBCh	CLCIN1PPS	1F3Ch	INLVLA	1FBCh	—
1D3Dh	LCDDATA37	1DBDh	—	1E3Dh	RF5PPS	1EBDh	CLCIN2PPS	1F3Dh	IOCAP	1FBDh	—
1D3Eh	LCDDATA38	1DBEh	—	1E3Eh	RF6PPS	1EBEh	CLCIN3PPS	1F3Eh	IOCAN	1FBEh	—
1D3Fh	LCDDATA39	1DBFh	—	1E3Fh	RF7PPS	1EBFh	—	1F3Fh	IOCAF	1FBFh	—
1D40h	LCDDATA40	1DC0h	—	1E40h	RG0PPS	1EC0h	—	1F40h	—	1FC0h	—
1D41h	LCDDATA41	1DC1h	—	1E41h	RG1PPS	1EC1h	—	1F41h	—	1FC1h	—
1D42h	LCDDATA42	1DC2h	—	1E42h	RG2PPS	1EC2h	—	1F42h	—	1FC2h	—
1D43h	LCDDATA43	1DC3h	—	1E43h	RG3PPS	1EC3h	ADCACTPPS	1F43h	ANSELB	1FC3h	—
1D44h	LCDDATA44	1DC4h	—	1E44h	RG4PPS	1EC4h	—	1F44h	WPUB	1FC4h	—
1D45h	LCDDATA45	1DC5h	—	1E45h	—	1EC5h	SSP1CLKPPS	1F45h	ODCONB	1FC5h	—
1D46h	LCDDATA46	1DC6h	—	1E46h	RG6PPS	1EC6h	SSP1DATPPS	1F46h	SLRCONB	1FC6h	—
1D47h	LCDDATA47	1DC7h	—	1E47h	RG7PPS	1EC7h	SSP1SSPPS	1F47h	INLVLB	1FC7h	—
1D48h	—	1DC8h	—	1E48h	RH0PPS	1EC8h	—	1F48h	IOCBP	1FC8h	—
1D49h	—	1DC9h	—	1E49h	RH1PPS	1EC9h	—	1F49h	IOCBN	1FC9h	—
1D4Ah	—	1DCAh	—	1E4Ah	RH2PPS	1ECAh	—	1F4Ah	IOCBF	1FCAh	—
1D4Bh	—	1DCBh	—	1E4Bh	RH3PPS	1ECBh	RX1PPS	1F4Bh	—	1FCBh	—
1D4Ch	—	1DCCh	—	1E4Ch	—	1ECCh	TX1PPS	1F4Ch	—	1FCCh	—
1D4Dh	—	1DCDh	—	1E4Dh	—	1ECDh	RX2PPS	1F4Dh	—	1FCDh	—
1D4Eh	—	1DCEh	—	1E4Eh	—	1ECEh	TX2PPS	1F4Eh	ANSELC	1FCEh	—
1D4Fh	—	1DCFh	—	1E4Fh	—	1ECFh	—	1F4Fh	WPUC	1FCFh	—
1D50h	—	1DD0h	—	1E50h	ANSELF	1ED0h	—	1F50h	ODCONC	1FD0h	—
1D51h	—	1DD1h	—	1E51h	WPUF	1ED1h	—	1F51h	SLRCONC	1FD1h	—
1D52h	—	1DD2h	—	1E52h	ODCONF	1ED2h	—	1F52h	INLVLC	1FD2h	—
1D53h	—	1DD3h	—	1E53h	SLRCONF	1ED3h	—	1F53h	IOCCP	1FD3h	—
1D54h	—	1DD4h	—	1E54h	INLVLF	1ED4h	—	1F54h	IOCCN	1FD4h	—
1D55h	—	1DD5h	—	1E55h	HIDRVF	1ED5h	—	1F55h	IOCCF	1FD5h	—
1D56h	—	1DD6h	—	1E56h	—	1ED6h	—	1F56h	—	1FD6h	—
1D57h	—	1DD7h	—	1E57h	—	1ED7h	—	1F57h	—	1FD7h	—
1D58h	—	1DD8h	—	1E58h	—	1ED8h	—	1F58h	—	1FD8h	—
1D59h	—	1DD9h	—	1E59h	—	1ED9h	—	1F59h	ANSELD	1FD9h	—

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19195/6/7 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 58											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1D0Ch	LCDCON	LCDEN	SLPEN	WERR	CS	LMUX<3:0>				0000 0000	0000 0000
1D0Dh	LCDPS	WFT	—	LCDA	WA	LP<3:0>				0-00 0000	0-000000
1D0Eh	LCDSE0	SE07	SE06	SE05	SE04	SE03	SE02	SE01	SE00	0000 0000	0000 0000
1D0Fh	LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE09	SE08	0000 0000	0000 0000
1D10h	LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	0000 0000
1D11h	LCDSE3	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	0000 0000	0000 0000
1D12h	LCDSE4	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	0000 0000	0000 0000
1D13h	LCDSE5	SE47	SE46	SE45	SE44	SE43	SE42	SE41	SE40	0000 0000	0000 0000
1D14h	LCDVCON1	LPEN	EN5V	—	—	—	BIAS<2:0>			00---000	xx---000
1D15h	LCDVCON2	CPWDT	—	—	—	LCDVSRC3	LCDVSRC2	LCDVSRC1	LCDVSRC0	0----000	0----000
1D16h	LCDREF	—	—	—	—	—	LCDCST<2:0>			0000 0000	0000 0000
1D17h	LCDRL	LRLAP<1:0>		LRLBP<1:0>		LCDIRI	LRLAT<2:0>			0000 0000	0000 0000
1D18h	LCDDATA0	S07C0	S06C0	S05C0	S04C0	S03C0	S02C0	S01C0	S00C0	0000 0000	0000 0000
1D19h	LCDDATA1	S15C0	S14C0	S13C0	S12C0	S11C0	S10C0	S09C0	S08C0	0000 0000	0000 0000
1D1Ah	LCDDATA2	S23C0	S22C0	S21C0	S20C0	S19C0	S18C0	S17C0	S16C0	0000 0000	0000 0000
1D1Bh	LCDDATA3	S31C0	S30C0	S29C0	S28C0	S27C0	S26C0	S25C0	S24C0	0000 0000	0000 0000
1D1Ch	LCDDATA4	S39C0	S38C0	S37C0	S36C0	S35C0	S34C0	S33C0	S32C0	0000 0000	0000 0000
1D1Dh	LCDDATA5	—	—	S45C0	S44C0	S43C0	S42C0	S41C0	S40C0	0000 0000	0000 0000
1D1Eh	LCDDATA6	S07C1	S06C1	S05C1	S04C1	S03C1	S02C1	S01C1	S00C1	0000 0000	0000 0000
1D1Fh	LCDDATA7	S15C1	S14C1	S13C1	S12C1	S11C1	S10C1	S09C1	S08C1	0000 0000	0000 0000
1D20h	LCDDATA8	S23C1	S22C1	S21C1	S20C1	S19C1	S18C1	S17C1	S16C1	0000 0000	0000 0000
1D21h	LCDDATA9	S31C1	S30C1	S29C1	S28C1	S27C1	S26C1	S25C1	S24C1	0000 0000	0000 0000
1D22h	LCDDATA10	S39C1	S38C1	S37C1	S36C1	S35C1	S34C1	S33C1	S32C1	0000 0000	0000 0000
1D23h	LCDDATA11	—	—	S45C1	S44C1	S43C1	S42C1	S41C1	S40C1	0000 0000	0000 0000
1D24h	LCDDATA12	S07C2	S06C2	S05C2	S04C2	S03C2	S02C2	S01C2	S00C2	0000 0000	0000 0000
1D25h	LCDDATA13	S15C2	S14C2	S13C2	S12C2	S11C2	S10C2	S09C2	S08C2	0000 0000	0000 0000
1D26h	LCDDATA14	S23C2	S22C2	S21C2	S20C2	S19C2	S18C2	S17C2	S16C2	0000 0000	0000 0000
1D27h	LCDDATA15	S31C2	S30C2	S29C2	S28C2	S27C2	S26C2	S25C2	S24C2	0000 0000	0000 0000
1D28h	LCDDATA16	S39C2	S38C2	S37C2	S36C2	S35C2	S34C2	S33C2	S32C2	0000 0000	0000 0000
1D29h	LCDDATA17	—	—	S45C2	S44C2	S43C2	S42C2	S41C2	S40C2	0000 0000	0000 0000

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19195/6/7 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 61 (Continued)											
1EE5h	—	Unimplemented								---- ----	---- ----
1EE6h	—	Unimplemented								---- ----	---- ----
1EE7h	—	Unimplemented								---- ----	---- ----
1EE8h	—	Unimplemented								---- ----	---- ----
1EE9h	—	Unimplemented								---- ----	---- ----
1EEAh	—	Unimplemented								---- ----	---- ----
1EEBh	—	Unimplemented								---- ----	---- ----
1EECh	—	Unimplemented								---- ----	---- ----
1EEDh	—	Unimplemented								---- ----	---- ----
1EEEh	—	Unimplemented								---- ----	---- ----
1EEFh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

8.3.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

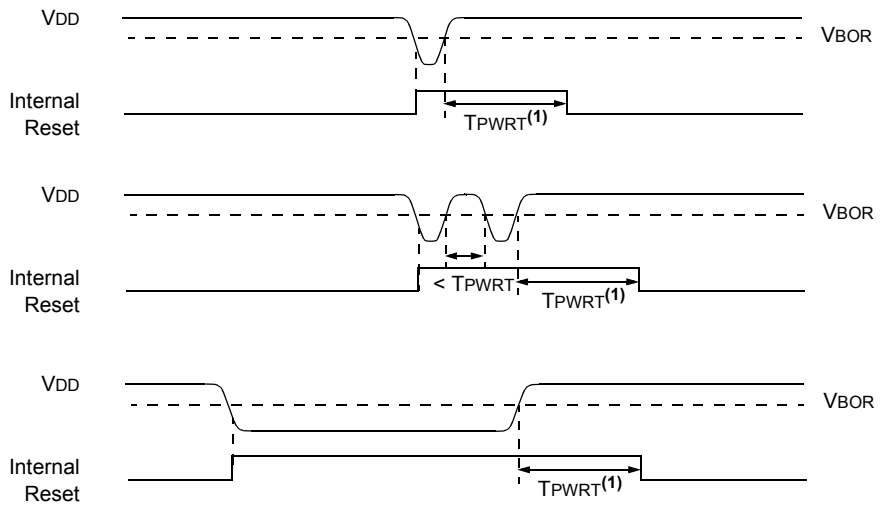
BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

8.3.4 BOR IS ALWAYS OFF

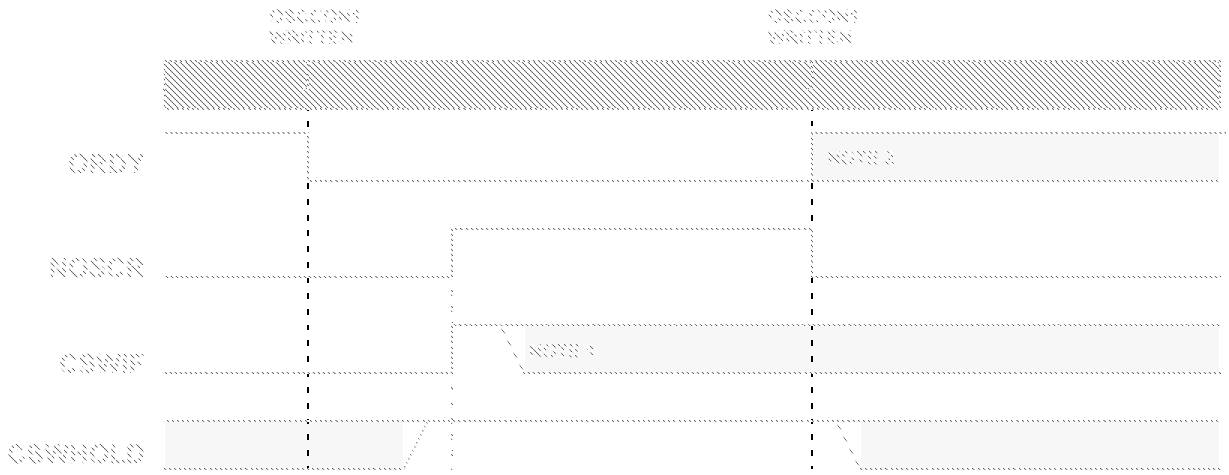
When the BOREN bits of the Configuration Words are programmed to '00', the BOR is off at all times. The device start-up is not delayed by the BOR ready condition or the VDD level.

FIGURE 8-2: BROWN-OUT SITUATIONS



Note 1: TPWRT delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

FIGURE 9-6: CLOCK SWITCH ABANDONED



Note 1: CSWIF may be cleared before or after rewriting OSCCON1; CSWIF is not automatically cleared.
2: ORDY = 0 if OSCCON1 does not match OSCCON2; a new switch will begin.

14.16 PORTH Registers

14.16.1 DATA REGISTER

PORTH is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISH (Register 14-2). Setting a TRISH bit (= 1) will make the corresponding PORTH pin an input (i.e., disable the output driver). Clearing a TRISH bit (= 0) will make the corresponding PORTH pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 14.2.8 shows how to initialize PORTH.

Reading the PORTH register (Register 14-1) reads the status of the pins, whereas writing to it will write to the PORT latch.

The PORT data latch LATH (Register 14-3) holds the output port data, and contains the latest value of a LATH or PORTH write.

EXAMPLE 14-7: INITIALIZING PORTH

```
; This code example illustrates
; initializing the PORTH register. The
; other ports are initialized in the same
; manner.

BANKSEL  PORTH        ;
CLRF     PORTH        ;Init PORTH
BANKSEL  LATH         ;Data Latch
CLRF     LATH         ;
BANKSEL  ANSELH       ;
CLRF     ANSELH       ;digital I/O
BANKSEL  TRISH        ;
MOVLW    B'00011100'  ;Set RH<4:2> as inputs
MOVWF    TRISH        ;and set RH<1:0> as
                      ;outputs
```

14.16.2 DIRECTION CONTROL

The TRISH register (Register 14-2) controls the PORTH pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISH register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

14.16.3 OPEN-DRAIN CONTROL

The ODCONH register (Register 14-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONH bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONH bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note:	It is not necessary to set open-drain control when using the pin for I^2C; the I^2C module controls the pin and makes the pin open-drain.

14.16.4 SLEW RATE CONTROL

The SLRCONH register (Register 14-7) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONH bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONH bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

14.16.5 INPUT THRESHOLD CONTROL

The INLVLH register (Register 14-8) controls the input voltage threshold for each of the available PORTH input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTH register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 39-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

15.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I^2C)

Note:	The I^2C SCLx and SDAx functions can be remapped through PPS. However, only the RB1, RB2, RC3 and RC4 pins have the I^2C and SMBus specific input buffers implemented (I^2C mode disables INLVL and sets thresholds that are specific for I^2C). If the SCLx or SDAx functions are mapped to some other pin (other than RB1, RB2, RC3 or RC4), the general purpose TTL or ST input buffers (as configured based on INLVL register setting) will be used instead. In most applications, it is therefore recommended only to map the SCLx and SDAx pin functions to the RB1, RB2, RC3 or RC4 pins.

15.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 15-1.

EXAMPLE 15-1: PPS LOCK/UNLOCK SEQUENCE

```
; suspend interrupts
    BCF     INTCON,GIE
;   BANKSEL PPSLOCK     ; set bank
; required sequence, next 5 instructions
    MOVLW   0x55
    MOVWF   PPSLOCK
    MOVLW   0xAA
    MOVWF   PPSLOCK
; Set PPSLOCKED bit to disable writes or
; Clear PPSLOCKED bit to enable writes
    BSF     PPSLOCK,PPSLOCKED
; restore interrupts
    BSF     INTCON,GIE
```

15.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

15.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

15.7 Effects of a Reset

A device Power-on-Reset (POR) clears all PPS input and output selections to their default values (Permanent Lock Removed). All other Resets leave the selections unchanged. Default input selections are shown in Table 15-1 and Table 15-2.

TABLE 19-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES(1,4)

ADC Clock Period (TAD)		Device Frequency (FOSC)					
ADC Clock Source	CS<5:0>	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
FOSC/2	000000	62.5 ns(2)	100 ns(2)	125 ns(2)	250 ns(2)	500 ns	2.0 μs
FOSC/4	000001	125 ns(2)	200 ns(2)	250 ns(2)	500 ns	1.0 μs	4.0 μs
FOSC/6	000010	187.5 ns(2)	300 ns(2)	375 ns(2)	750 ns	1.5 μs	6.0 μs
FOSC/8	000011	250 ns(2)	400 ns(2)	500 ns	1.0 μs	2.0 μs	8.0 μs
...	...	...	...	...	...	...	...
FOSC/16	000111	500 ns	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs(3)
...	...	...	...	...	...	...	...
FOSC/128	111111	4.0 μs	6.4 μs	8.0 μs	16.0 μs(3)	32.0 μs(2)	128.0 μs(2)
FRC	CS(ADCON0<4>) = 1	1.0-6.0 μs	1.0-6.0 μs	1.0-6.0 μs	1.0-6.0 μs	1.0-6.0 μs	1.0-6.0 μs

Legend: Shaded cells are outside of recommended range.

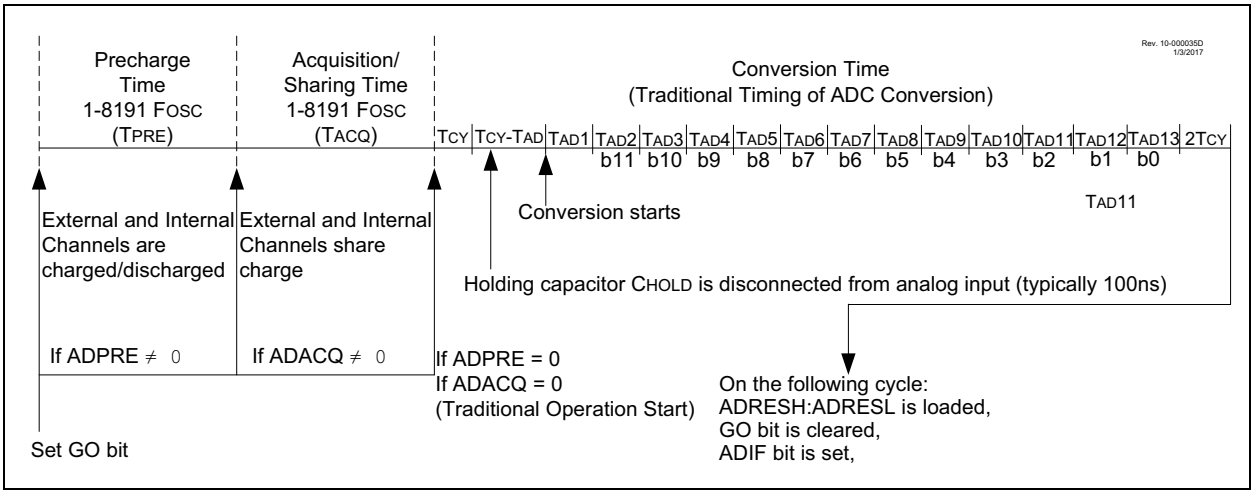
Note 1: See TAD parameter for FRC source typical TAD value.

2: These values violate the required TAD time.

3: Outside the recommended TAD time.

4: The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock FOSC. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 19-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



19.2 ADC Operation

19.2.1 STARTING A CONVERSION

To enable the ADC module, the ON bit of the ADCON0 register must be set to a '1'. A conversion may be started by any of the following:

- Software setting the GO bit of ADCON0 to '1'
- An external trigger (selected by Register 19-3)
- A continuous-mode retrigger (see section **Section 19.5.8 "Continuous Sampling mode"**)

Note:	The GO bit should not be set in the same instruction that turns on the ADC. Refer to **Section 19.2.6 "ADC Conversion Procedure (Basic Mode)"**.

19.2.2 COMPLETION OF A CONVERSION

When any individual conversion is complete, the value already in ADRES is written into PREV (if ADPSIS = 1) and the new conversion results appear in ADRES. When the conversion completes, the ADC module will:

- Clear the GO bit (unless the CONT bit of ADCON0 is set)
- Set the ADIF Interrupt Flag bit
- Set the ADMATH bit
- Update ACC

When ADDSEN = 0 then after every conversion, or when ADDSEN = 1 then after every other conversion, the following events occur:

- ERR is calculated
- ADTIF is set if ERR calculation meets threshold comparison

Importantly, filter and threshold computations occur after the conversion itself is complete. As such, interrupt handlers responding to ADIF should check ADTIF before reading filter and threshold results.

Note:	A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

19.2.3 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the ADCRC option. When the FRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ON bit remains set.

19.2.4 EXTERNAL TRIGGER DURING SLEEP

If the external trigger is received during sleep while ADC clock source is set to the FRC, ADC module will perform the conversion and set the ADIF bit upon completion.

If an external trigger is received when the ADC clock source is something other than FRC, the trigger will be recorded, but the conversion will not begin until the device exits Sleep.

REGISTER 19-2: ADCON1: ADC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0
PPOL	IPEN	GPOL	—	—	—	—	DSEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PPOL:** Precharge Polarity bit
If PRE>0x00:

PPOL	Action During 1st Precharge Stage	
	External (selected analog I/O pin)	Internal (AD sampling capacitor)
1	Connected to V_{DD}	C_{HOLD} connected to V_{SS}
0	Connected to V_{SS}	C_{HOLD} connected to V_{DD}

Otherwise:
The bit is ignored

bit 6 **IPEN:** A/D Inverted Precharge Enable bit
If DSEN = 1
1 = The precharge and guard signals in the second conversion cycle are the opposite polarity of the first cycle
0 = Both Conversion cycles use the precharge and guards specified by ADPPOL and ADGPOL
Otherwise:
The bit is ignored

bit 5 **GPOL:** Guard Ring Polarity Selection bit
1 = ADC guard Ring outputs start as digital high during Precharge stage
0 = ADC guard Ring outputs start as digital low during Precharge stage

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **DSEN:** Double-sample enable bit
1 = Two conversions are performed on each trigger. Data from the first conversion appears in PREV
0 = One conversion is performed for each trigger

25.0 TIMER0 MODULE

The Timer0 module is an 8/16-bit timer/counter with the following features:

- 16-bit timer/counter
- 8-bit timer/counter with programmable period
- Synchronous or asynchronous operation
- Selectable clock sources
- Programmable prescaler (independent of Watchdog Timer)
- Programmable postscaler
- Operation during Sleep mode
- Interrupt on match or overflow
- Output on I/O pin (via PPS) or to other peripherals

25.1 Timer0 Operation

Timer0 can operate as either an 8-bit timer/counter or a 16-bit timer/counter. The mode is selected with the T016BIT bit of the T0CON register.

25.1.1 16-BIT MODE

In normal operation, TMR0 increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

25.1.1.1 Timer0 Reads and Writes in 16-Bit Mode

TMR0H is not the actual high byte of Timer0 in 16-bit mode. It is actually a buffered version of the real high byte of Timer0, which is neither directly readable nor writable (see Figure 25-1). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte was valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

25.1.2 8-BIT MODE

In normal operation, TMR0 increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

The value of TMR0L is compared to that of the Period buffer, a copy of TMR0H, on each clock cycle. When the two values match, the following events happen:

- TMR0_out goes high for one prescaled clock period
- TMR0L is reset
- The contents of TMR0H are copied to the period buffer

In 8-bit mode, the TMR0L and TMR0H registers are both directly readable and writable. The TMR0L register is cleared on any device Reset, while the TMR0H register initializes at FFh.

Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset – Power-on Reset (POR), MCLR Reset, Watchdog Timer Reset (WDTR) or
- Brown-out Reset (BOR)

25.1.3 COUNTER MODE

In Counter mode, the prescaler is normally disabled by setting the T0CKPS bits of the T0CON1 register to '0000'. Each rising edge of the clock input (or the output of the prescaler if the prescaler is used) increments the counter by '1'.

25.1.4 TIMER MODE

In Timer mode, the Timer0 module will increment every instruction cycle as long as there is a valid clock signal and the T0CKPS bits of the T0CON1 register (Register 25-2) are set to '0000'. When a prescaler is added, the timer will increment at the rate based on the prescaler value.

25.1.5 ASYNCHRONOUS MODE

When the T0ASYNC bit of the T0CON1 register is set (T0ASYNC = '1'), the counter increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows the counter to continue operation during Sleep mode provided that the clock also continues to operate during Sleep.

25.1.6 SYNCHRONOUS MODE

When the T0ASYNC bit of the T0CON1 register is clear (T0ASYNC = 0), the counter clock is synchronized to the system oscillator (FOSC/4). When operating in Synchronous mode, the counter clock frequency cannot exceed FOSC/4.

REGISTER 25-1: T0CON0: TIMER0 CONTROL REGISTER 0

R/W-0/0	U-0	R-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **T0EN:** Timer0 Enable bit
1 = The module is enabled and operating
0 = The module is disabled and in the lowest power mode

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **T0OUT:** Timer0 Output bit (read-only)
Timer0 output bit

bit 4 **T016BIT:** Timer0 Operating as 16-bit Timer Select bit
1 = Timer0 is a 16-bit timer
0 = Timer0 is an 8-bit timer

bit 3-0 **T0OUTPS<3:0>:** Timer0 output postscaler (divider) select bits
1111 = 1:16 Postscaler
1110 = 1:15 Postscaler
1101 = 1:14 Postscaler
1100 = 1:13 Postscaler
1011 = 1:12 Postscaler
1010 = 1:11 Postscaler
1001 = 1:10 Postscaler
1000 = 1:9 Postscaler
0111 = 1:8 Postscaler
0110 = 1:7 Postscaler
0101 = 1:6 Postscaler
0100 = 1:5 Postscaler
0011 = 1:4 Postscaler
0010 = 1:3 Postscaler
0001 = 1:2 Postscaler
0000 = 1:1 Postscaler

29.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral that allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

The Capture/Compare/PWM modules available are shown in Table 29-1.

TABLE 29-1: AVAILABLE CCP MODULES

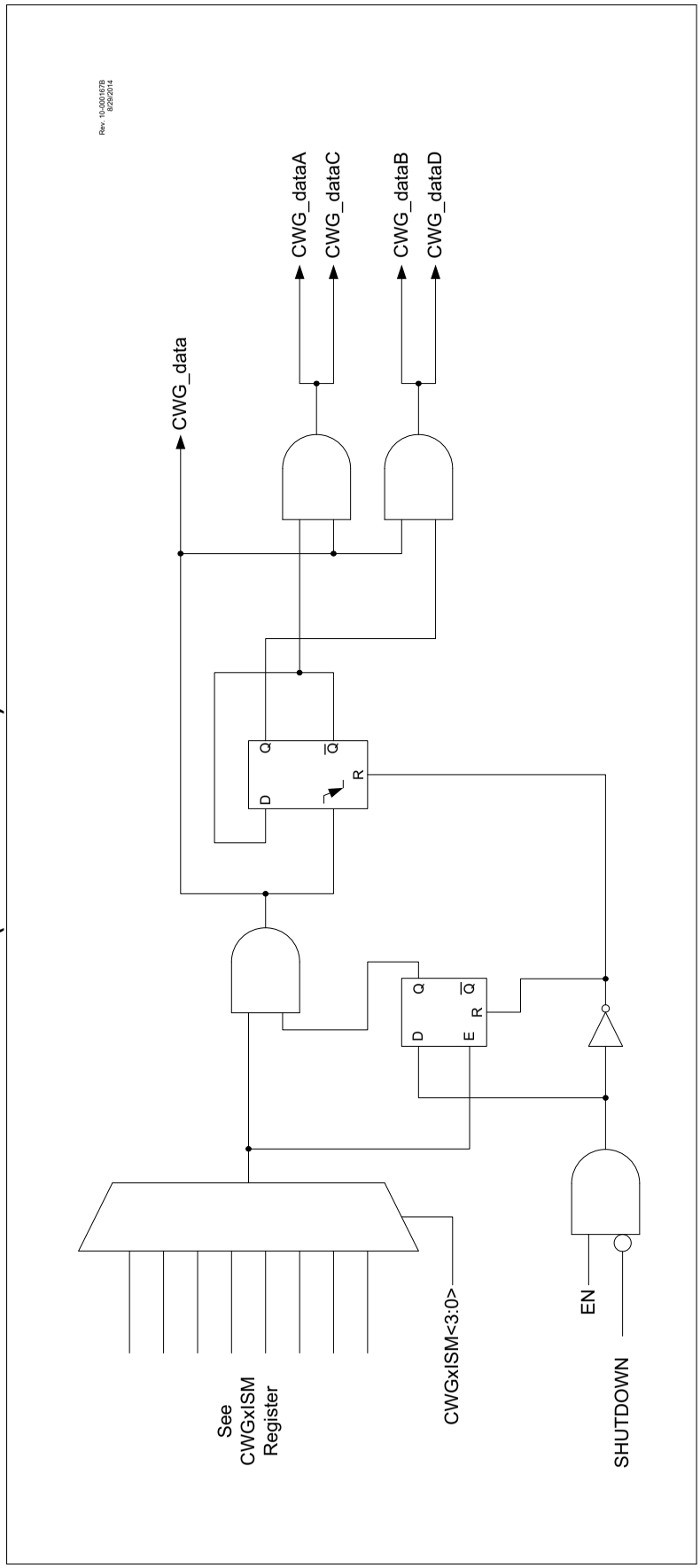
Device	CCP1	CCP2
PIC16(L)F19195/6/7	•	•

The Capture and Compare functions are identical for all CCP modules.

Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.

2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator ‘x’ to indicate the use of a numeral to distinguish a particular module, when required.

FIGURE 31-2: SIMPLIFIED CWG BLOCK DIAGRAM (PUSH-PULL MODE)



31.5 Dead-Band Control

The dead-band control provides non-overlapping PWM signals to prevent shoot-through current in PWM switches. Dead-band operation is employed for Half-Bridge and Full-Bridge modes. The CWG contains two 6-bit dead-band counters. One is used for the rising edge of the input source control in Half-Bridge mode or for reverse dead-band Full-Bridge mode. The other is used for the falling edge of the input source control in Half-Bridge mode or for forward dead band in Full-Bridge mode.

Dead band is timed by counting CWG clock periods from zero up to the value in the rising or falling dead-band counter registers. See CWG1DBR and CWG1DBF registers, respectively.

31.5.1 DEAD-BAND FUNCTIONALITY IN HALF-BRIDGE MODE

In Half-Bridge mode, the dead-band counters dictate the delay between the falling edge of the normal output and the rising edge of the inverted output. This can be seen in Figure 31-9.

31.5.2 DEAD-BAND FUNCTIONALITY IN FULL-BRIDGE MODE

In Full-Bridge mode, the dead-band counters are used when undergoing a direction change. The MODE<0> bit of the CWG1CON0 register can be set or cleared while the CWG is running, allowing for changes from Forward to Reverse mode. The CWG1A and CWG1C signals will change upon the first rising input edge following a direction change, but the modulated signals (CWG1B or CWG1D, depending on the direction of the change) will experience a delay dictated by the dead-band counters. This is demonstrated in Figure 31-3.

31.6 Rising Edge and Reverse Dead Band

CWG1DBR controls the rising edge dead-band time at the leading edge of CWG1A (Half-Bridge mode) or the leading edge of CWG1B (Full-Bridge mode). The CWG1DBR value is double-buffered. When EN = 0, the CWG1DBR register is loaded immediately when CWG1DBR is written. When EN = 1, then software must set the LD bit of the CWG1CON0 register, and the buffer will be loaded at the next falling edge of the CWG input signal. If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.

31.7 Falling Edge and Forward Dead Band

CWG1DBF controls the dead-band time at the leading edge of CWG1B (Half-Bridge mode) or the leading edge of CWG1D (Full-Bridge mode). The CWG1DBF value is double-buffered. When EN = 0, the CWG1DBF register is loaded immediately when CWG1DBF is written. When EN = 1 then software must set the LD bit of the CWG1CON0 register, and the buffer will be loaded at the next falling edge of the CWG input signal. If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.

Refer to Figure 31-6 and Figure 31-7 for examples.

FIGURE 35-11: TYPE-A WAVEFORMS IN 1/2 MUX, 1/3 BIAS DRIVE

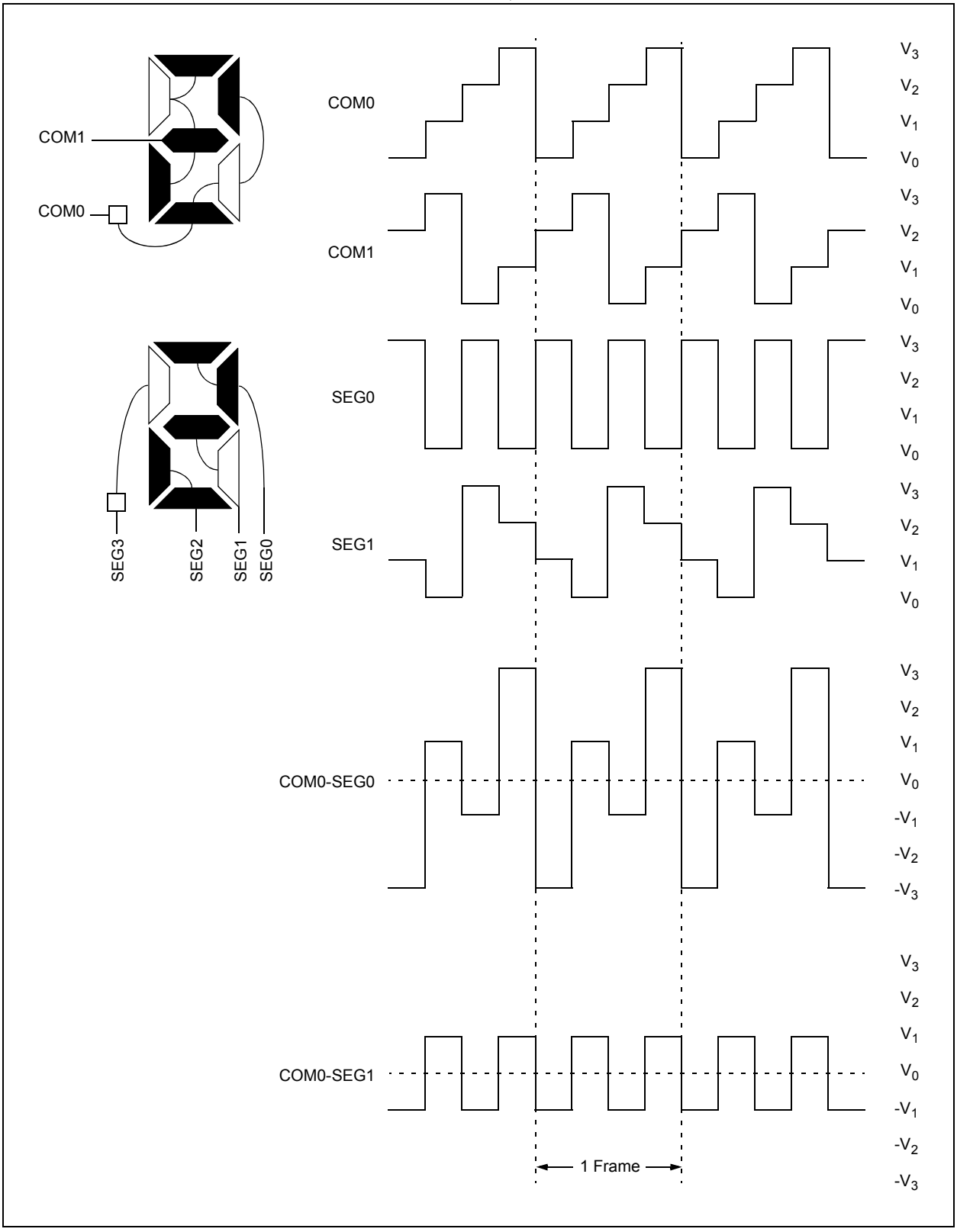
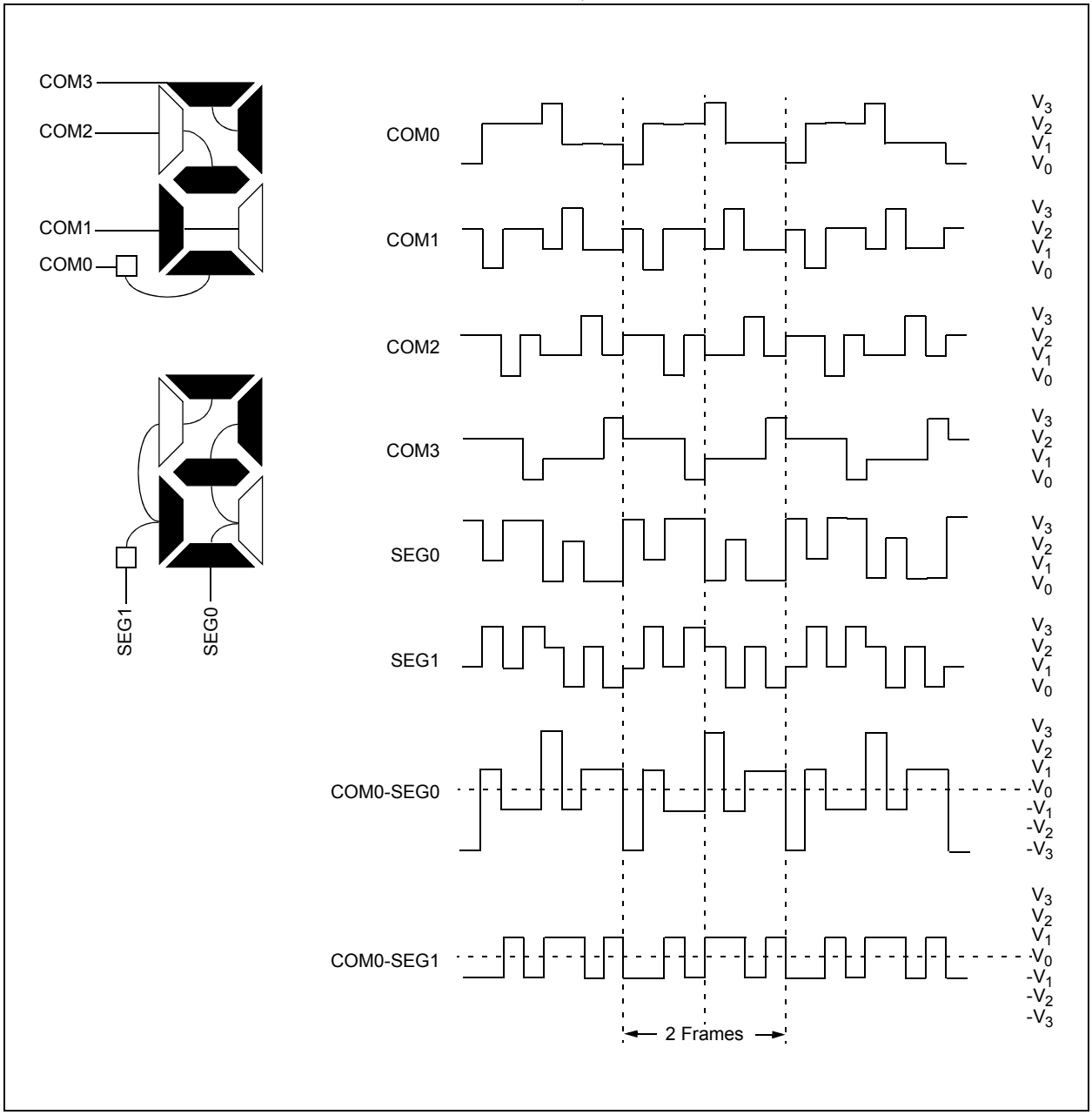


FIGURE 35-18: TYPE-B WAVEFORMS IN 1/4 MUX, 1/3 BIAS DRIVE



36.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $\overline{\text{MCLR}}$/VPP
- VDD
- VSS

In Program/Verify mode the program memory, data EEPROM, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the **"***PIC16(L)F153XX Memory Programming Specification***"** (DS40001838).

36.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on $\overline{\text{MCLR}}$/VPP to VIHH.

36.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Words is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

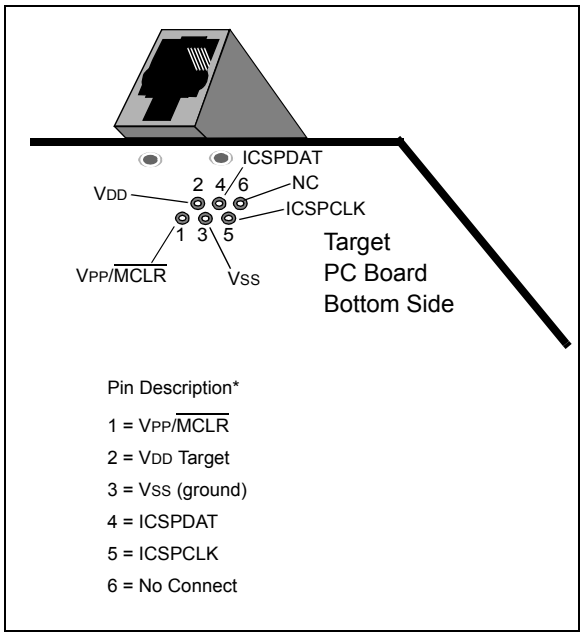
Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

If low-voltage programming is enabled (LVP = 1), the $\overline{\text{MCLR}}$ Reset function is automatically enabled and cannot be disabled. See **Section 8.6"MCLR"** for more information.

36.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 36-1.

FIGURE 36-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 36-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 36-3 for more information.

CALL **Call Subroutine**

Syntax:	[*label*] CALL k
Operands:	$0 \le k \le 2047$
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<6:3>) → PC<14:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a 2-cycle instruction.

CALLW **Subroutine Call With W**

Syntax:	[*label*] CALLW
Operands:	None
Operation:	(PC) +1 → TOS, (W) → PC<7:0>, (PCLATH<6:0>) → PC<14:8>
Status Affected:	None
Description:	Subroutine call with W. First, the return address (PC + 1) is pushed onto the return stack. Then, the contents of W is loaded into PC<7:0>, and the contents of PCLATH into PC<14:8>. CALLW is a 2-cycle instruction.

CLRF **Clear f**

Syntax:	[*label*] CLRF f
Operands:	$0 \le f \le 127$
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register ‘f’ are cleared and the Z bit is set.

CLRW **Clear W**

Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT **Clear Watchdog Timer**

Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF **Complement f**

Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	($\bar{f}$) → (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are complemented. If ‘d’ is ‘0’, the result is stored in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

DECF **Decrement f**

Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

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