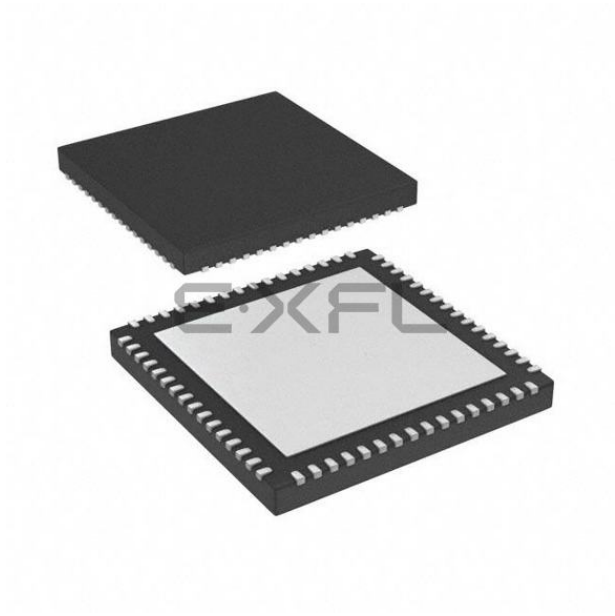

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 45x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19195t-i-mr

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19195/6/7 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 14											
CPU CORE REGISTERS; see Table 4-3 for specifics											
70Ch	PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	--00 ---1	00-- ---1
70Dh	PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	00-- --00	00-- --00
70Eh	PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	0000 0000	0000 0000
70Fh	PIR3	RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	0000 --00	0000 --00
710h	PIR4	—	—	—	—	TMR4IF	—	TMR2IF	TMR1IF	0000 0000	0000 0000
711h	PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	0000 ---0	0000 ---0
712h	PIR6	CRIF	—	—	—	—	—	CCP2IF	CCP1IF	0--- --00	0--- --00
713h	PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	0000 0000	0000 0000
714h	PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	00-- -000	00-- -000
715h	—	Unimplemented								---- ----	---- ----
716h	PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	0000 0000	0000 0000
717h	PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	00-- --00	00-- --00
718h	PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	0000 0000	0000 0000
719h	PIE3	RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	0000 --00	0000 --00
71Ah	PIE4	—	—	—	—	TMR4IF	—	TMR2IE	TMR1IE	0000 0000	0000 0000
71Bh	PIE5	CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	0000 ---0	0000 ---0
71Ch	PIE6	CRIE	—	—	—	—	—	CCP2IE	CCP1IE	0--- --00	0--- --00
71Dh	PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	0000 0000	0000 0000
71Eh	PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	00-- -000	00-- -000
71Fh	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19195/6/7 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 63											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1F8Ch	—	Unimplemented								---- ----	---- ----
1F8Dh	—	Unimplemented								---- ----	---- ----
1F8Eh	—	Unimplemented								---- ----	---- ----
1F8Fh	—	Unimplemented								---- ----	---- ----
1F90h	—	Unimplemented								---- ----	---- ----
1F91h	—	Unimplemented								---- ----	---- ----
1F92h	—	Unimplemented								---- ----	---- ----
1F93h	—	Unimplemented								---- ----	---- ----
1F94h	—	Unimplemented								---- ----	---- ----
1F95h	—	Unimplemented								---- ----	---- ----
1F96h	—	Unimplemented								---- ----	---- ----
1F97h	—	Unimplemented								---- ----	---- ----
1F98h	—	Unimplemented								---- ----	---- ----
1F99h	—	Unimplemented								---- ----	---- ----
1F9Ah	—	Unimplemented								---- ----	---- ----
1F9Bh	—	Unimplemented								---- ----	---- ----
1F9Ch	—	Unimplemented								---- ----	---- ----
1F9Dh	—	Unimplemented								---- ----	---- ----
1F9Eh	—	Unimplemented								---- ----	---- ----
1F9Fh	—	Unimplemented								---- ----	---- ----
1FA0h	—	Unimplemented								---- ----	---- ----

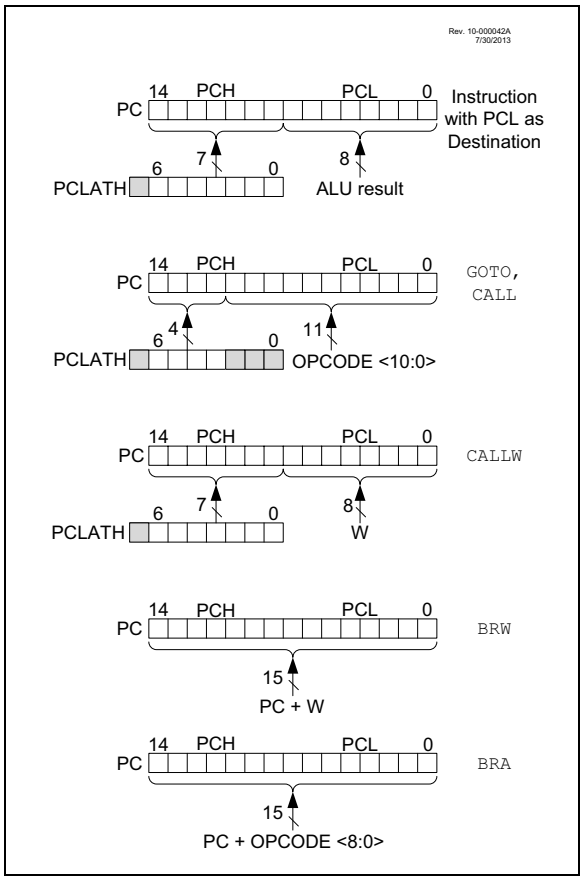
Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

4.4 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 4-3 shows the five situations for the loading of the PC.

FIGURE 4-3: LOADING OF PC IN DIFFERENT SITUATIONS



4.4.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

4.4.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

4.4.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

4.4.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 + the signed value of the operand of the BRA instruction.

10.6 Register Definitions: Interrupt Control

REGISTER 10-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	U-0	R/W-1/1
GIE	PEIE	—	—	—	—	—	INTEDG
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 10-16: PIR5: PERIPHERAL INTERRUPT REQUEST REGISTER 5

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	R/W/HS-0/0
CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **CLC4IF:** CLC4 Interrupt Flag bit
1 = A CLC4OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC4 interrupt event has occurred

bit 6 **CLC3IF:** CLC3 Interrupt Flag bit
1 = A CLC3OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC3 interrupt event has occurred

bit 5 **CLC2IF:** CLC2 Interrupt Flag bit
1 = A CLC2OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC2 interrupt event has occurred

bit 4 **CLC1IF:** CLC1 Interrupt Flag bit
1 = A CLC1OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC1 interrupt event has occurred

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = The Timer1 Gate has gone inactive (the acquisition is complete)
0 = The Timer1 Gate has not gone inactive

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

11.4 Register Definitions: Voltage Regulator and DOZE Control

REGISTER 11-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER (1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	U-0
—	—	—	—	—	—	VREGPM	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **VREGPM**: Voltage Regulator Power Mode Selection bit
- 1 = Low-Power Sleep mode enabled in Sleep(2)
  Draws lowest current in Sleep, slower wake-up
- 0 = Normal Power mode enabled in Sleep(2)
  Draws higher current in Sleep, faster wake-up

bit 0 **Unimplemented:** Read as '1'. Maintain this bit set

Note 1: PIC16F19195/6/7 only.

2: See **Section 39.0 "Electrical Specifications"**.

14.5 Register Definitions: PORTB

REGISTER 14-9: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RB<7:0>**: PORTB I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

REGISTER 14-10: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **TRISB<7:0>:** PORTB Tri-State Control bit
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

REGISTER 14-15: SLRCONB: PORTB SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SLRB<7:0>:** PORTB Slew Rate Enable bits
For RB<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 14-16: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLB<7:0>:** PORTB Input Level Select bits
For RB<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

TABLE 14-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTE	RE7	RE6	RE5	RE4	RE3	—	RE1	RE0	229
TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	—	TRISE1	TRISE0	229
LATE	LATE7	LATE6	LATE5	LATE4	LATE3	—	LATE1	LATE0	230
ANSELE	ANSE7	ANSE6	ANSE5	ANSE4	ANSE3	—	ANSE1	ANSE0	230
WPUE	WPUE7	WPUE6	WPUE5	WPUE4	WPUE3	—	WPUE1	WPUE0	231
ODCONE	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	—	ODCE1	ODCE0	231
SLRCONE	SLRE7	SLRE6	SLRE5	SLRE4	SLRE3	—	SLRE1	SLRE0	232
INLVLE	INLVLE7	INLVLE6	INLVLE5	INLVLE4	INLVLE3	—	INLVLE1	INLVLE0	232

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTE.

REGISTER 14-55: SLRCONG: PORTG SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRG7	SLRG6	—	SLRG4	SLRG3	SLRG2	SLRG1	SLRG0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **SLRG<7:6>:** PORTG Slew Rate Enable bits
For RG<7:6> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **SLRG<4:0>:** PORTG Slew Rate Enable bits
For RG<4:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 14-56: INLVLG: PORTG INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLG7	INLVLG6	INLVLG5	INLVLG4	INLVLG3	INLVLG2	INLVLG1	INLVLG0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLG<7:0>:** PORTG Input Level Select bits
For RG<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

REGISTER 19-35: ADACT: ADC AUTO CONVERSION TRIGGER CONTROL REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	ACT<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **Unimplemented**: Read as '0'

bit 4-0 **ACT<4:0>**: Auto-Conversion Trigger Select Bits
11111 = Software write to ADPCH
11110 = Reserved, do not use
11101 = Software read of ADRESH
11100 = Software read of ADERRH
11011 = CLC4_out
11010 = CLC3_out
11001 = CLC2_out
11000 = CLC1_out
10111 = Logical OR of all Interrupt-on-change Interrupt Flags
10110 = CMP2_out
10101 = CMP1_out
10100 = Reserved, do not use
10011 = Reserved, do not use
10010 = Reserved, do not use
10001 = Reserved, do not use
10000 = Reserved, do not use
01111 = PWM4_out
01110 = PWM3_out
01101 = Reserved, do not use
01100 = Reserved, do not use
01011 = CCP2_trigger
01010 = CCP1_trigger
01001 = SMT1_trigger
01000 = RTCC Seconds
00111 = Reserved, do not use
00110 = TMR4_postscaled
00101 = Reserved, do not use
00100 = TMR2_postscaled
00011 = TMR1_overflow
00010 = TMR0_overflow
00001 = Pin selected by ADCACTPPS
00000 = External Trigger Disabled

REGISTER 24-8: MINUTES(1): MINUTE VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINH<2:0>			MINL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINH<2:0>:** Binary Coded Decimal value of minutes '10' digit; valid values from 0 to 5

bit 3-0 **MINL<3:0>:** Binary Coded Decimal value of minutes '1' digit; valid values from 0 to 9

Note 1: Writes to the MINUTE registers are only allowed when RTCWREN = 1.

REGISTER 24-9: SECONDS(1): SECOND VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECH<2:0>			SECL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECH<2:0>:** Binary Coded Decimal value of seconds '10' digit; valid values from 0 to 5

bit 3-0 **SECL<3:0>:** Binary Coded Decimal value of seconds '1' digit; valid values from 0 to 9

Note 1: Writes to the SECOND registers are only allowed when RTCWREN = 1.

TABLE 30-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				398
T2TMR	Holding Register for the 8-bit TMR2 Register								378*
T2PR	TMR2 Period Register								378*
RxyPPS	—	—	—	RxyPPS<4:0>					259
CWG1ISM	—	—	—	—	IS<3:0>				486
CLCxSELy	—	—	LCxDyS<5:0>						497
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	205
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	218

Legend: - = Unimplemented locations, read as '0'. Shaded cells are not used by the PWMx module.

*Page provides register information.

TABLE 31-2: SUMMARY OF REGISTERS ASSOCIATED WITH CWG

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CWG1CLKCON	—	—	—	—	—	—	—	CS	486
CWG1ISM	—	—	—	—	IS<3:0>				486
CWG1DBR	—	—	DBR<5:0>						482
CWG1DBF	—	—	DBF<5:0>						482
CWG1CON0	EN	LD	—	—	—	MODE<2:0>			480
CWG1CON1	—	—	IN	—	POLD	POLC	POLB	POLA	481
CWG1AS0	SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	483
CWG1AS1	—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	484
CWG1STR	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	485

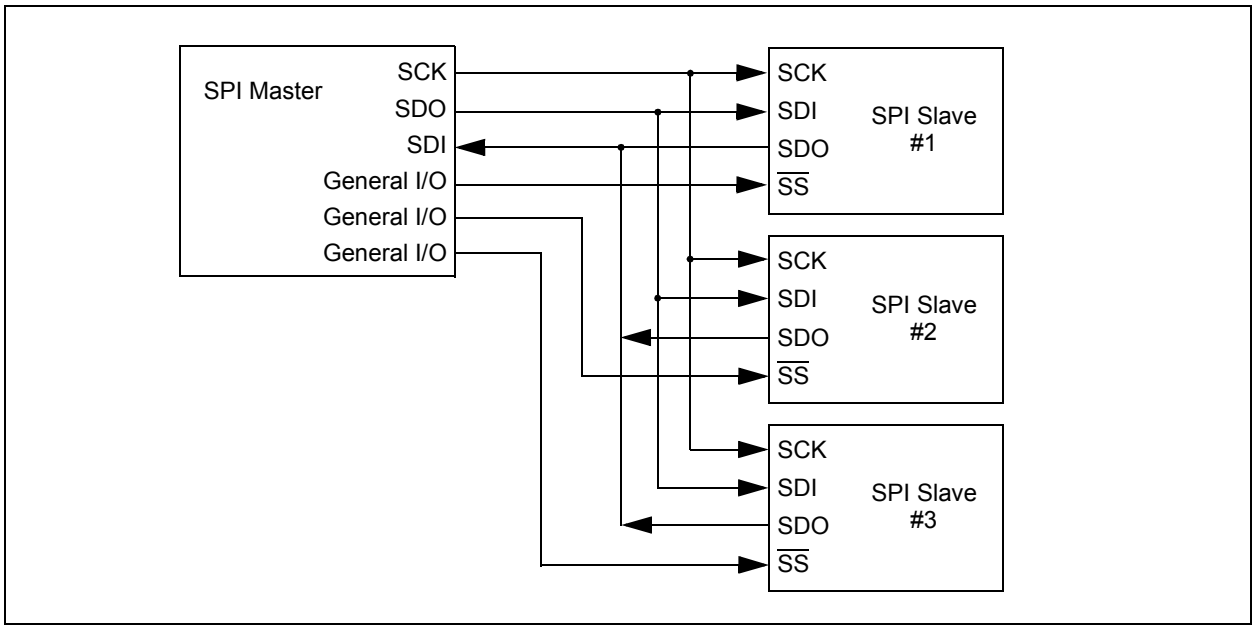
Legend: – = unimplemented locations read as '0'. Shaded cells are not used by CWG.

TABLE 32-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx (continued)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CLC4GLS1	LC4G2D4T	LC4G2D4N	LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	499
CLC4GLS2	LC4G3D4T	LC4G3D4N	LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	500
CLC4GLS3	LC4G4D4T	LC4G4D4N	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	501
CLCIN0PPS	—	—	—	CLCIN0PPS<4:0>					258
CLCIN1PPS	—	—	—	CLCIN1PPS<4:0>					258
CLCIN2PPS	—	—	—	CLCIN2PPS<4:0>					258
CLCIN3PPS	—	—	—	CLCIN3PPS<4:0>					258

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.

FIGURE 33-4: SPI MASTER AND MULTIPLE SLAVE CONNECTION



33.2.1 SPI MODE REGISTERS

The MSSP module has five registers for SPI mode operation. These are:

- MSSP STATUS register (SSPxSTAT)
- MSSP Control register 1 (SSPxCON1)
- MSSP Control register 3 (SSPxCON3)
- MSSP Data Buffer register (SSPxBUF)
- MSSP Address register (SSPxADD)
- MSSP Shift register (SSPxSR) (Not directly accessible)

SSPxCON1 and SSPxSTAT are the control and status registers in SPI mode operation. The SSPxCON1 register is readable and writable. The lower six bits of the SSPxSTAT are read-only. The upper two bits of the SSPxSTAT are read/write.

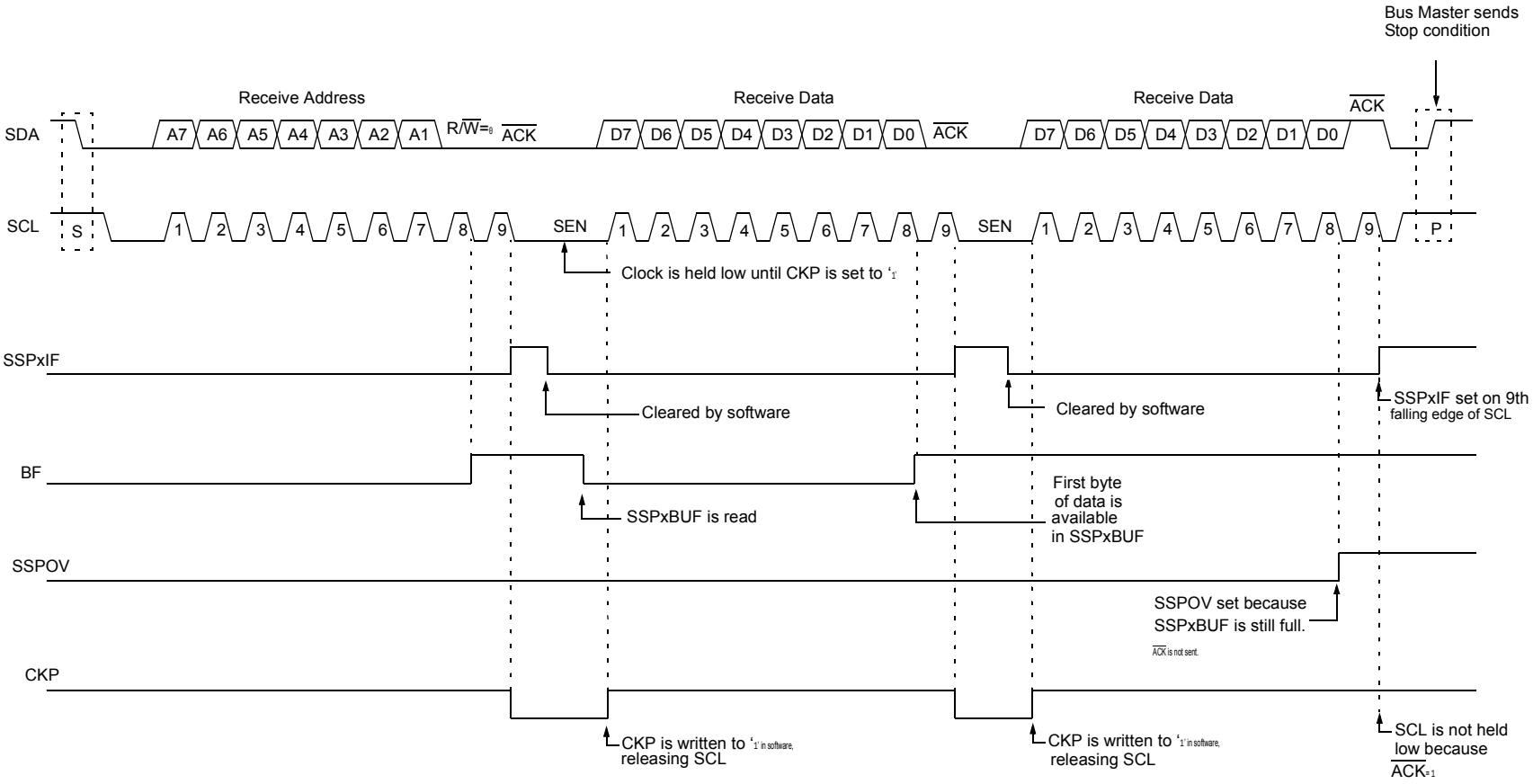
In one SPI master mode, SSPxADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in **Section 33.7 "Baud Rate Generator"**.

SSPxSR is the shift register used for shifting data in and out. SSPxBUF provides indirect access to the SSPxSR register. SSPxBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPxSR and SSPxBUF together create a buffered receiver. When SSPxSR receives a complete byte, it is transferred to SSPxBUF and the SSPxIF interrupt is set.

During transmission, the SSPxBUF is not buffered. A write to SSPxBUF will write to both SSPxBUF and SSPxSR.

FIGURE 33-15: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)



REGISTER 33-7: SSPxBUF: MSSPx BUFFER REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SSPxBUF<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SSPxBUF<7:0>:** MSSP Buffer bits

TABLE 33-3: SUMMARY OF REGISTERS ASSOCIATED WITH MSSPx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	147
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	158
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	149
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	550
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				551
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	552
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	553
SSP1MSK	SSPMSK<7:0>								554
SSP1ADD	SSPADD<7:0>								554
SSP1BUF	SSPBUF<7:0>								555
SSP2STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	550
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				551
SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	552
SSP2CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	553
SSP2MSK	SSPMSK<7:0>								554
SSP2ADD	SSPADD<7:0>								554
SSP2BUF	SSPBUF<7:0>								555
SSP1CLKPPS	—	—	—	SSP1CLKPPS<4:0>					258
SSP1DATPPS	—	—	—	SSP1DATPPS<4:0>					258
SSP1SSPPS	—	—	—	SSP1SSPPS<4:0>					258
SSP2CLKPPS	—	—	—	SSP2CLKPPS<4:0>					258
SSP2DATPPS	—	—	—	SSP2DATPPS<4:0>					258
SSP2SSPPS	—	—	—	SSP2SSPPS<4:0>					258
RxyPPS	—	—	—	RxyPPS<4:0>					259

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSPx module.

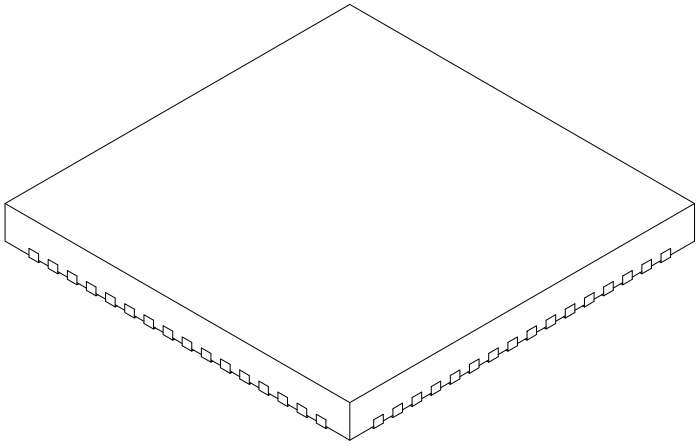
TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19195/6/7 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
68Dh	—	Unimplemented								
68Eh	—	Unimplemented								
68Fh	—	Unimplemented								
690h	—	Unimplemented								
691h	—	Unimplemented								
692h	—	Unimplemented								
693h	—	Unimplemented								
694h	—	Unimplemented								
695h	—	Unimplemented								
696h	—	Unimplemented								
697h	—	Unimplemented								
698h	—	Unimplemented								
699h	—	Unimplemented								
69Ah	—	Unimplemented								
69Bh	—	Unimplemented								
69Ch	—	Unimplemented								
69Dh	—	Unimplemented								
69Eh	—	Unimplemented								
69Fh	—	Unimplemented								
70Ch	PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	157
70Dh	PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	158
70Eh	PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	159
70Fh	PIR3	RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	160
710h	PIR4	—	—	—	—	TMR4IF	—	TMR2IF	TMR1IF	161
711h	PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	162
712h	PIR6	CRIF	—	—	—	—	—	CCP2IF	CCP1IF	163
713h	PIR7	—	—	NVMIF	—	—	—	—	CWG1IF	164
714h	PIR8	LCDIF	RTCCIF	—	—	—	SMT1PWAIF	SMT1PRAIF	SMT1IF	165
715h	—	Unimplemented								
716h	PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	148
717h	PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	149
718h	PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	150
719h	PIE3	RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	151
71Ah	PIE4	—	—	—	—	TMR4IF	—	TMR2IE	TMR1IE	152
71Bh	PIE5	CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	153
71Ch	PIE6	CRIE	—	—	—	—	—	CCP2IE	CCP1IE	154
71Dh	PIE7	—	—	NVMIE	—	—	—	—	CWG1IE	155
71Eh	PIE8	LCDIE	RTCCIE	—	—	—	SMT1PWAIE	SMT1PRAIE	SMT1IE	156
71Fh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2