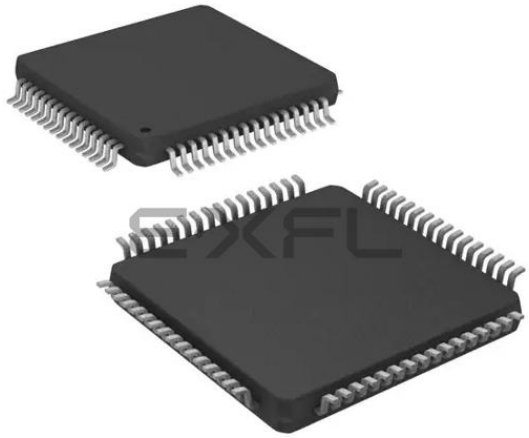

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 45x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f19196t-i-pt

TABLE 1-2: PIC16(L)F19195/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/C2IN4-/C1IN4-/ANA0/CLCIN0(1)/SEG33	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN4-	AN		Comparator negative input.
	C1IN4-	AN		Comparator negative input.
	ANA0	AN		ADC Channel input.
	CLCIN0(1)	—		Configurable Logic Cell source input.
	SEG33	AN		LCD Analog output.
RA1/ANA1/CLCIN1(1)/T2IN(1)/SEG18	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN		ADC Channel input.
	CLCIN1(1)	—		Configurable Logic Cell source input.
	T2IN(1)	—		Timer2 external input.
	SEG18	AN		LCD Analog output.
RA2/C2IN1+/C1IN1+/ANA2/SEG34	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	C2IN1+	AN		Comparator positive input.
	C1IN1+	AN		Comparator positive input.
	ANA2	AN		ADC Channel input.
	SEG34	AN		LCD Analog output.
RA3/ANA3/SEG35/VREF+ (ADC)/VREF+ (DAC1)	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	ANA3	AN		ADC Channel input.
	SEG35	AN		LCD Analog output.
	VREF+ (ADC)	AN		ADC positive reference.
	VREF+ (DAC1)	AN		DAC positive reference.
RA4/ANA4/T0CKI(1)/SEG14	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN		ADC Channel input.
	T0CKI(1)	—		Timer0 clock input.
	SEG14	AN		LCD Analog output.
RA5/VBAT	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	VBAT	AN		RTCC Back-up Battery.
RA6/ANA6/SEG36/CLKOUT	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN		ADC Channel input.
	SEG36	AN		LCD Analog output.
	CLKOUT	TTL/ST		FOSC/4 digital output.
RA7/ANA7/SEG37/CLKIN	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN		ADC Channel input.
	SEG37	AN		LCD Analog output.
	CLKIN	ST		External Clock input.
RB0/IOCB0/ANB0/SEG30/ZCD	RB0	TTL/ST	CMOS/OD	General purpose I/O.
	IOCB0	TTL/ST		Interrupt-on-change input.
	ANB0	AN		ADC Channel input.
	SEG30	AN		LCD Analog output.
	ZCD	—		Zero-cross detect input pin (with constant current sink/source).

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C; HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 14-2 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 14-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 4-12: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 PIC16(L)F19195/6/7 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 58											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1D0Ch	LCDCON	LCDEN	SLPEN	WERR	CS	LMUX<3:0>				0000 0000	0000 0000
1D0Dh	LCDPS	WFT	—	LCDA	WA	LP<3:0>				0-00 0000	0-000000
1D0Eh	LCDSE0	SE07	SE06	SE05	SE04	SE03	SE02	SE01	SE00	0000 0000	0000 0000
1D0Fh	LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE09	SE08	0000 0000	0000 0000
1D10h	LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	0000 0000
1D11h	LCDSE3	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	0000 0000	0000 0000
1D12h	LCDSE4	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	0000 0000	0000 0000
1D13h	LCDSE5	SE47	SE46	SE45	SE44	SE43	SE42	SE41	SE40	0000 0000	0000 0000
1D14h	LCDVCON1	LPEN	EN5V	—	—	—	BIAS<2:0>			00---000	xx---000
1D15h	LCDVCON2	CPWDT	—	—	—	LCDVSRC3	LCDVSRC2	LCDVSRC1	LCDVSRC0	0----000	0----000
1D16h	LCDREF	—	—	—	—	—	LCDCST<2:0>			0000 0000	0000 0000
1D17h	LCDRL	LRLAP<1:0>		LRLBP<1:0>		LCDIRI	LRLAT<2:0>			0000 0000	0000 0000
1D18h	LCDDATA0	S07C0	S06C0	S05C0	S04C0	S03C0	S02C0	S01C0	S00C0	0000 0000	0000 0000
1D19h	LCDDATA1	S15C0	S14C0	S13C0	S12C0	S11C0	S10C0	S09C0	S08C0	0000 0000	0000 0000
1D1Ah	LCDDATA2	S23C0	S22C0	S21C0	S20C0	S19C0	S18C0	S17C0	S16C0	0000 0000	0000 0000
1D1Bh	LCDDATA3	S31C0	S30C0	S29C0	S28C0	S27C0	S26C0	S25C0	S24C0	0000 0000	0000 0000
1D1Ch	LCDDATA4	S39C0	S38C0	S37C0	S36C0	S35C0	S34C0	S33C0	S32C0	0000 0000	0000 0000
1D1Dh	LCDDATA5	—	—	S45C0	S44C0	S43C0	S42C0	S41C0	S40C0	0000 0000	0000 0000
1D1Eh	LCDDATA6	S07C1	S06C1	S05C1	S04C1	S03C1	S02C1	S01C1	S00C1	0000 0000	0000 0000
1D1Fh	LCDDATA7	S15C1	S14C1	S13C1	S12C1	S11C1	S10C1	S09C1	S08C1	0000 0000	0000 0000
1D20h	LCDDATA8	S23C1	S22C1	S21C1	S20C1	S19C1	S18C1	S17C1	S16C1	0000 0000	0000 0000
1D21h	LCDDATA9	S31C1	S30C1	S29C1	S28C1	S27C1	S26C1	S25C1	S24C1	0000 0000	0000 0000
1D22h	LCDDATA10	S39C1	S38C1	S37C1	S36C1	S35C1	S34C1	S33C1	S32C1	0000 0000	0000 0000
1D23h	LCDDATA11	—	—	S45C1	S44C1	S43C1	S42C1	S41C1	S40C1	0000 0000	0000 0000
1D24h	LCDDATA12	S07C2	S06C2	S05C2	S04C2	S03C2	S02C2	S01C2	S00C2	0000 0000	0000 0000
1D25h	LCDDATA13	S15C2	S14C2	S13C2	S12C2	S11C2	S10C2	S09C2	S08C2	0000 0000	0000 0000
1D26h	LCDDATA14	S23C2	S22C2	S21C2	S20C2	S19C2	S18C2	S17C2	S16C2	0000 0000	0000 0000
1D27h	LCDDATA15	S31C2	S30C2	S29C2	S28C2	S27C2	S26C2	S25C2	S24C2	0000 0000	0000 0000
1D28h	LCDDATA16	S39C2	S38C2	S37C2	S36C2	S35C2	S34C2	S33C2	S32C2	0000 0000	0000 0000
1D29h	LCDDATA17	—	—	S45C2	S44C2	S43C2	S42C2	S41C2	S40C2	0000 0000	0000 0000

9.6 Register Definitions: Oscillator Control

REGISTER 9-1: OSCCON1: OSCILLATOR CONTROL REGISTER1

U-0	R/W-f/f(1)	R/W-f/f(1)	R/W-f/f(1)	R/W-q/q	R/W-q/q	R/W-q/q	R/W-q/q
—	NOSC<2:0>(2,3)			NDIV<3:0>(2,3,4)			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	f = determined by fuse setting

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **NOSC<2:0>:** New Oscillator Source Request bits
The setting requests a source oscillator and PLL combination per Table 9-1.
POR value = RSTOSC (Register 5-1).

bit 3-0 **NDIV<3:0>:** New Divider Selection Request bits
The setting determines the new postscaler division ratio per Table 9-1.

Note 1: The default value (f/f) is set equal to the RSTOSC Configuration bits.
2: If NOSC is written with a reserved value (Table 9-1), the operation is ignored and neither NOSC nor NDIV is written.
3: When CSWEN = 0, this register is read-only and cannot be changed from the POR value.
4: When NOSC = 110 (HFINTOSC 4 MHz), the NDIV bits will default to '0010' upon Reset; for all other NOSC settings the NDIV bits will default to '0000' upon Reset.

REGISTER 9-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2(1)

U-0	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)
—	COSC<2:0>			CDIV<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **COSC<2:0>:** Current Oscillator Source Select bits (read-only)
Indicates the current source oscillator and PLL combination per Table 9-1.

bit 3-0 **CDIV<3:0>:** Current Divider Select bits (read-only)
Indicates the current postscaler division ratio per Table 9-1.

Note 1: The POR value is the value present when user code execution begins.
2: The Reset value (n/n) is the same as the NOSC/NDIV bits.

REGISTER 10-15: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4

U-0	U-0	U-0	U-0	R/W/HS-0/0	U-0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	—	TMR4IF	—	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **TRM4IF:** Timer4 Interrupt Flag bit
1 = The TMR4 postscaler overflowed, or in 1:1 mode, a TMR4 to PR4 match occurred (must be cleared in software)
0 = No TMR4 event has occurred

bit 2 **Unimplemented:** Read as '0'

bit 1 **TRM2IF:** Timer2 Interrupt Flag bit
1 = The TMR2 postscaler overflowed, or in 1:1 mode, a TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 event has occurred

bit 0 **TRM1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 overflow occurred (must be cleared in software)
0 = No Timer1 overflow occurred

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- Current draw from pins with internal weak pull-ups
- Modules using any oscillator

I/O pins that are high-impedance inputs should be pulled to VDD or VSS externally to avoid switching currents caused by floating inputs.

Any module with a clock source that is not FOSC can be enabled. Examples of internal circuitry that might be sourcing current include modules such as the DAC and FVR modules. See **Section 21.0 "5-Bit Digital-to-Analog Converter (DAC1) Module"**, **Section 18.0 "Fixed Voltage Reference (FVR)"** for more information on these modules.

11.2.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on $\overline{\text{MCLR}}$ pin, if enabled.
2. BOR Reset, if enabled.
3. POR Reset.
4. Watchdog Timer, if enabled.
5. Any external interrupt.
6. Interrupts by peripherals capable of running during Sleep (see individual peripheral for more information).

The first three events will cause a device Reset. The last three events are considered a continuation of program execution. To determine whether a device Reset or wake-up event occurred, refer to **Section 8.14 "Determining the Cause of a Reset"**.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is enabled, the device executes the instruction after the SLEEP instruction, the device will then call the Interrupt Service Routine. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WWDT is cleared when the device wakes-up from Sleep, regardless of the source of wake-up.

12.6 Operation During Sleep

When the device enters Sleep, the WWDT is cleared. If the WWDT is enabled during Sleep, the WWDT resumes counting. When the device exits Sleep, the WWDT is cleared again.

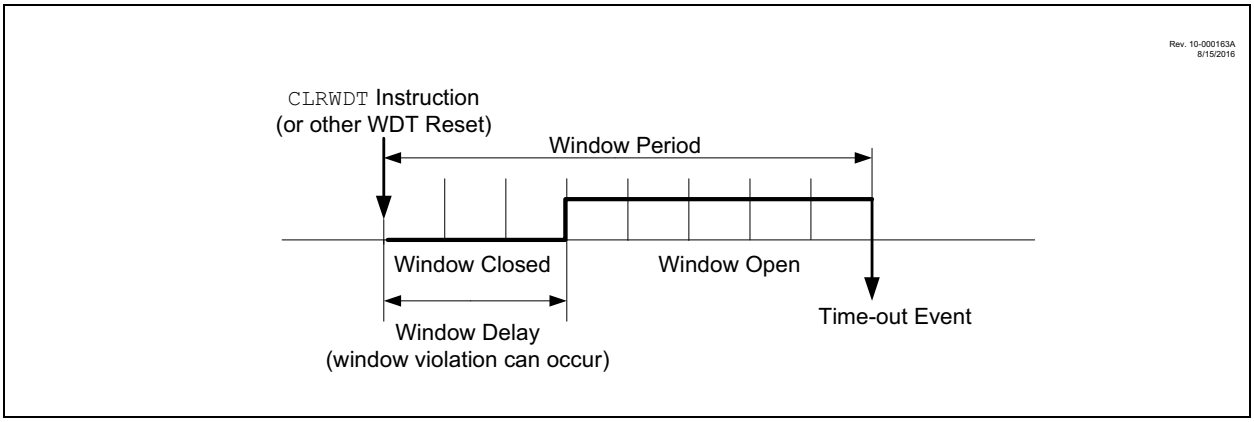
The WWDT remains clear until the OST, if enabled, completes. See **Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for more information on the OST.

When a WWDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register are changed to indicate the event. The $\overline{RWDT}$ bit in the PCON register can also be used. See **Section 4.3.2.1 "STATUS Register"** for more information.

TABLE 12-2: WWDT CLEARING CONDITIONS

Conditions	WWDT
WDTE<1:0> = 00	Cleared
WDTE<1:0> = 01 and SWDTEN = 0	
WDTE<1:0> = 10 and enter Sleep	
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = SOSC, EXTOSC, INTOSC	
Change INTOSC divider (IRCF bits)	Unaffected

FIGURE 12-2: WINDOW PERIOD AND DELAY



REGISTER 12-3: WDTPSL: WDT PRESCALE SELECT LOW BYTE REGISTER

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
PSCNT<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PSCNT<7:0>**: Prescale Select Low Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

REGISTER 12-4: WDTPSH: WDT PRESCALE SELECT HIGH BYTE REGISTER

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
PSCNT<15:8>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PSCNT<15:8>**: Prescale Select High Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

REGISTER 12-5: WDTTMR: WDT TIMER REGISTER

U-0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
—	WDTTMR<3:0>				STATE	PSCNT<17:16>(1)	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **WDTTMR<3:0>**: Watchdog Timer Value bits

bit 2 **STATE**: WDT Armed Status bit
1 = WDT is armed
0 = WDT is not armed

bit 1-0 **PSCNT<17:16>**: Prescale Select Upper Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

14.7 Register Definitions: PORTC

REGISTER 14-17: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RC<7:0>**: PORTC General Purpose I/O Pin bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.

REGISTER 14-18: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

REGISTER 14-19: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **LATC<7:0>**: PORTC Output Latch Value bits

14.15 Register Definitions: PORTG

REGISTER 14-49: PORTG: PORTG REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RG7	RG6	RG5	RG4	RG3	RG2	RG1	RG0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RG<7:0>**: PORTG I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTG are actually written to corresponding LATG register. Reads from PORTG register is return of actual I/O pin values.

REGISTER 14-50: TRISG: PORTG TRI-STATE REGISTER

R/W-1/1	R/W-1/1	U-1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISG7	TRISG6	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **TRISG<7:6>:** PORTG Tri-State Control bit(1)
1 = PORTG pin configured as an input (tri-stated)
0 = PORTG pin configured as an output

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **TRISG<4:0>:** PORTG Tri-State Control bit
1 = PORTG pin configured as an input (tri-stated)
0 = PORTG pin configured as an output

Note 1: TRISG is an input only function for VPP/$\overline{\text{MCLR}}$/RG5.

20.4 Minimum Operating VDD

When the temperature circuit is operated in Low range, the device may be operated at any operating voltage that is within specifications. When the temperature circuit is operated in High range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 20-1 shows the recommended minimum VDD vs. Range setting.

TABLE 20-1: RECOMMENDED VDD vs. RANGE

Min.VDD, TSRNG = 1 (High Range)	Min. VDD, TSRNG = 0 (Low Range)
≥ 2.5	≥ 1.8

20.5 Temperature Indicator Range

The temperature indicator circuit operates in either High or Low range. The High range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range. High range requires a higher-bias voltage to operate and thus, a higher VDD is needed. The Low range is selected by clearing the TSRNG bit of the FVRCON register. The Low range generates a lower sensor voltage and thus, a lower VDD voltage is needed to operate the circuit.

The output voltage of the sensor is the highest value at -40°C and the lowest value at +125°C.

- **High Range:** The High range is used in applications with the reference for the ADC, VREF = 2.048V. This range may not be suitable for battery-powered applications.
- **Low Range:** This mode is useful in applications in which the VDD is too low for high-range operation. The VDD in this mode can be as low as 1.8V. VDD must, however, be at least 0.5V higher than the maximum sensor voltage depending on the expected low operating temperature.

20.6 DIA Information

DIA data provide ADC readings at one operating temperature. DIA data is taken during factory testing and stored within the device. The 90°C reading alone allows single-point calibration as described in Section 20.2.1, Calibration, by solving Equation 20-1 for TOFFSET.

Refer to **Section 6.0 "Device Information Area"** for more information on the data stored in the DIA and how to access them.

Note:	The lower temperature range (e.g., - 40°C) will suffer in accuracy because temperature conversion must extrapolate below the reference points, amplifying any measurement errors.

TABLE 20-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		279

Legend: — = Unimplemented location, read as '0'. Shaded cells are unused by the temperature indicator module.

21.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC1) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DAC1OUT pin

The Digital-to-Analog Converter (DAC) is enabled by setting the DAC1EN bit of the DAC1CON0 register.

21.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DAC1R<4:0> bits of the DAC1CON1 register.

The DAC output voltage is determined by Equation 21-1:

EQUATION 21-1: DAC OUTPUT VOLTAGE

$$V_{OUT} = \left(V_{SOURCE+} - V_{SOURCE-}\right) \times \frac{DAC1R\langle 4:0\rangle}{2^5} + \left(V_{SOURCE-}\right)$$

$$V_{SOURCE+} = V_{DD} \text{ or } V_{REF+} \text{ or } FVR$$

$$V_{SOURCE-} = V_{SS} \text{ or } V_{REF-}$$

21.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in Table 39-16.

21.3 DAC Voltage Reference Output

The DAC voltage can be output to the DAC1OUT1/2 pins by setting the DAC1OE1/2 bits of the DAC1CON0 register, respectively. Selecting the DAC reference voltage for output on the DAC1OUT1/2 pins automatically overrides the digital output buffer and digital input threshold detector functions, disables the weak pull-up, and disables the current-controlled drive function of that pin. Reading the DAC1OUT1/2 pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to the DAC1OUT1/2 pins. Figure 21-2 shows an example buffering technique.

23.9 Register Definitions: ZCD Control

REGISTER 23-1: ZCDCON: ZERO-CROSS DETECTION CONTROL REGISTER

R/W-q/q	U-0	R-x/x	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
SEN	—	OUT	POL	—	—	INTP	INTN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on Configuration bits

bit 7 **SEN**: Zero-Cross Detection Enable bit
1 = Zero-cross detect is enabled. ZCD pin is forced to output to source and sink current.
0 = Zero-cross detect is disabled. ZCD pin operates according to PPS and TRIS controls.

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Zero-Cross Detection Logic Level bit
POL bit = 1:
1 = ZCD pin is sourcing current
0 = ZCD pin is sinking current
POL bit = 0:
1 = ZCD pin is sinking current
0 = ZCD pin is sourcing current

bit 4 **POL:** Zero-Cross Detection Logic Output Polarity bit
1 = ZCD logic output is inverted
0 = ZCD logic output is not inverted

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **INTP:** Zero-Cross Positive Edge Interrupt Enable bit
1 = ZCDIF bit is set on low-to-high ZCDx_output transition
0 = ZCDIF bit is unaffected by low-to-high ZCDx_output transition

bit 0 **INTN:** Zero-Cross Negative Edge Interrupt Enable bit
1 = ZCDIF bit is set on high-to-low ZCDx_output transition
0 = ZCDIF bit is unaffected by high-to-low ZCDx_output transition

TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE ZCD MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	151
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	160
ZCDxCON	SEN	—	OUT	POL	—	—	INTP	INTN	343

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the ZCD module.

TABLE 23-2: SUMMARY OF CONFIGURATION WORD WITH THE ZCD MODULE

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG2	13:8	—	—	$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	ZCDDIS	BORV	—	103
	7:0	BOREN <1:0>		$\overline{\text{LPBOREN}}$	—	—	—	$\overline{\text{PWRTE}}$	MCLRE	

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the ZCD module.

26.1 Timer1 Operation

The Timer1 modules are 16-bit incrementing counters which are accessed through the TMR1H:TMR1L register pairs. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

The timer is enabled by configuring the TMR1ON and GE bits in the T1CON and T1GCON registers, respectively. Table 26-1 displays the Timer1 enable selections.

TABLE 26-1: TIMER1 ENABLE SELECTIONS

TMR1ON	TMR1GE	Timer1 Operation
1	1	Count Enabled
1	0	Always On
0	1	Off
0	0	Off

26.2 Clock Source Selection

The T1CLK register is used to select the clock source for the timer. Register 26-3 shows the possible clock sources that may be selected to make the timer increment.

26.2.1 INTERNAL CLOCK SOURCE

When the internal clock source FOSC is selected, the TMR1H:TMR1L register pair will increment on multiples of FOSC as determined by the respective Timer1 prescaler.

When the FOSC internal clock source is selected, the timer register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the TMR1H:TMR1L value. To utilize the full resolution of the timer in this mode, an asynchronous input signal must be used to gate the timer clock input.

Out of the total timer gate signal sources, the following subset of sources can be asynchronous and may be useful for this purpose:

- CLC4 output
- CLC3 output
- CLC2 output
- CLC1 output
- Zero-Cross Detect output
- Comparator2 output
- Comparator1 output
- TxG PPS remappable input pin

26.2.2 EXTERNAL CLOCK SOURCE

When the timer is enabled and the external clock input source (ex: T1CKI PPS remappable input) is selected as the clock source, the timer will increment on the rising edge of the external clock input.

When using an external clock source, the timer can be configured to run synchronously or asynchronously, as described in **Section 26.5 "Timer Operation in Asynchronous Counter Mode"**.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used connected to the SOSCI/SOSCO pins.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- The timer is first enabled after POR
- Firmware writes to TMR1H or TMR1L
- The timer is disabled
- The timer is re-enabled (e.g., TMR1ON-->1) when the T1CKI signal is currently logic low.

27.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = 01110)
- High Reset level (MODE<4:0> = 01111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

REGISTER 28-16: SMTxPRL: SMT PERIOD REGISTER – LOW BYTE

R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1
SMTxPR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxPR<7:0>**: Significant bits of the SMT Timer Value for Period Match – Low Byte

REGISTER 28-17: SMTxPRH: SMT PERIOD REGISTER – HIGH BYTE

R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1
SMTxPR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxPR<15:8>**: Significant bits of the SMT Timer Value for Period Match – High Byte

REGISTER 28-18: SMTxPRU: SMT PERIOD REGISTER – UPPER BYTE

R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1
SMTxPR<23:16>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SMTxPR<23:16>**: Significant bits of the SMT Timer Value for Period Match – Upper Byte

32.7 Register Definitions: CLC Control

REGISTER 32-1: CLCxCON: CONFIGURABLE LOGIC CELL CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
LCxEN	—	LCxOUT	LCxINTP	LCxINTN	LCxMODE<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **LCxEN:** Configurable Logic Cell Enable bit
1 = Configurable logic cell is enabled and mixing input signals
0 = Configurable logic cell is disabled and has logic zero output

bit 6 **Unimplemented:** Read as '0'

bit 5 **LCxOUT:** Configurable Logic Cell Data Output bit
Read-only: logic cell output data, after LCPOL; sampled from CLCxOUT

bit 4 **LCxINTP:** Configurable Logic Cell Positive Edge Going Interrupt Enable bit
1 = CLCxIF will be set when a rising edge occurs on CLCxOUT
0 = CLCxIF will not be set

bit 3 **LCxINTN:** Configurable Logic Cell Negative Edge Going Interrupt Enable bit
1 = CLCxIF will be set when a falling edge occurs on CLCxOUT
0 = CLCxIF will not be set

bit 2-0 **LCxMODE<2:0>:** Configurable Logic Cell Functional Mode bits
111 = Cell is 1-input transparent latch with S and R
110 = Cell is J-K flip-flop with R
101 = Cell is 2-input D flip-flop with R
100 = Cell is 1-input D flip-flop with S and R
011 = Cell is S-R latch
010 = Cell is 4-input AND
001 = Cell is OR-XOR
000 = Cell is AND-OR

TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19195/6/7 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
30Ch	CCPR1L	RL								454
30Dh	CCPR1H	RH								455
30Eh	CCP1CON	CCP1EN	—	CCP1OUT	CCP1FMT	CCP1MODE<3:0>				452
		—		—	—	CCP1-MODE3	CCP1-MODE2	CCP1-MODE1	CCP1MODE0	452
30Fh	CCP1CAP	CCP1CTS								454
		—	—	—	—	—	CCP1CTS2	CCP1CTS1	CCP1CTS0	454
310h	CCPR2L	RL								454
311h	CCPR2H	RH								455
312h	CCP2CON	CCP2EN	—	CCP2OUT	CCP2FMT	CCP2MODE<3:0>				452
		—		—	—	CCP2-MODE3	CCP2-MODE2	CCP2-MODE1	CCP2MODE0	452
313h	CCP2CAP	CCP2CTS								454
		—	—	—	—	—	CCP2CTS2	CCP2CTS1	CCP2CTS0	454
314h	PWM3DCL	PWM3DC<1:0>		—	—	—	—	—	—	462
		PWM3DC1	PWM3DC0	—	—	—	—	—	—	462
315h	PWM3DCH	PWM3DC								462
		PWM3DC9	PWM3DC8	PWM3DC7	PWM3DC6	PWM3DC5	PWM3DC4	PWM3DC3	PWM3DC2	462
316h	PWM3CON	PWM3EN	—	PWM3OUT	PWM3POL	—	—	—	—	461
317h	—	Unimplemented								461
318h	PWM4DCL	PWM4DC<1:0>		—	—	—	—	—	—	462
		PWM4DC1	PWM4DC0	—	—	—	—	—	—	462
319h	PWM4DCH	PWM4DC								462
		PWM4DC9	PWM4DC8	PWM4DC7	PWM4DC6	PWM4DC5	PWM4DC4	PWM4DC3	PWM4DC2	462
31Ah	PWM4CON	PWM4EN	—	PWM4OUT	PWM4POL	—	—	—	—	461
31Bh 31Fh	—	Unimplemented								
38Ch	—	Unimplemented								
38Dh	—	Unimplemented								
38Eh	—	Unimplemented								
38Fh	—	Unimplemented								
390h	—	Unimplemented								
391h	—	Unimplemented								
392h	—	Unimplemented								
393h	—	Unimplemented								
394h	—	Unimplemented								
395h	—	Unimplemented								
396h	—	Unimplemented								
397h	—	Unimplemented								
398h	—	Unimplemented								
399h	—	Unimplemented								
39Ah	—	Unimplemented								
39Bh	—	Unimplemented								
39Ch	—	Unimplemented								
39Dh	—	Unimplemented								
39Eh	—	Unimplemented								
39Fh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

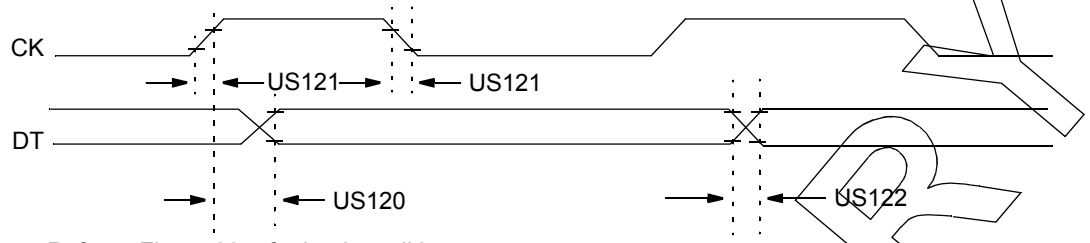
TABLE 38-1: REGISTER FILE SUMMARY FOR PIC16(L)F19195/6/7 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
1FA1h	—	Unimplemented								
1FA2h	—	Unimplemented								
1FA3h	—	Unimplemented								
1FA4h	—	Unimplemented								
1FA5h	—	Unimplemented								
1FA6h	—	Unimplemented								
1FA7h	—	Unimplemented								
1FA8h	—	Unimplemented								
1FA9h	—	Unimplemented								
1FAAh	—	Unimplemented								
1FABh	—	Unimplemented								
1FACh	—	Unimplemented								
1FADh	—	Unimplemented								
1FAEh	—	Unimplemented								
1FAFh	—	Unimplemented								
1FB0h	—	Unimplemented								
1FB1h	—	Unimplemented								
1FB2h	—	Unimplemented								
1FB3h	—	Unimplemented								
1FB4h	—	Unimplemented								
1FB5h	—	Unimplemented								
1FB6h	—	Unimplemented								
1FB7h	—	Unimplemented								
1FB8h	—	Unimplemented								
1FB9h	—	Unimplemented								
1FBAh	—	Unimplemented								
1FBBh	—	Unimplemented								
1FBCh	—	Unimplemented								
1FBDh	—	Unimplemented								
1FBEh	—	Unimplemented								
1FBFh	—	Unimplemented								
1FC0h	—	Unimplemented								
1FC1h	—	Unimplemented								
1FC2h	—	Unimplemented								
1FC3h	—	Unimplemented								
1FC4h	—	Unimplemented								
1FC5h	—	Unimplemented								
1FC6h	—	Unimplemented								
1FC7h	—	Unimplemented								
1FC8h	—	Unimplemented								
1FC9h	—	Unimplemented								
1FCAh	—	Unimplemented								
1FCBh	—	Unimplemented								
1FCCh	—	Unimplemented								
1FCDh	—	Unimplemented								
1FCEh	—	Unimplemented								
1FCFh	—	Unimplemented								

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Unimplemented data memory locations, read as '0'.

FIGURE 39-15: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

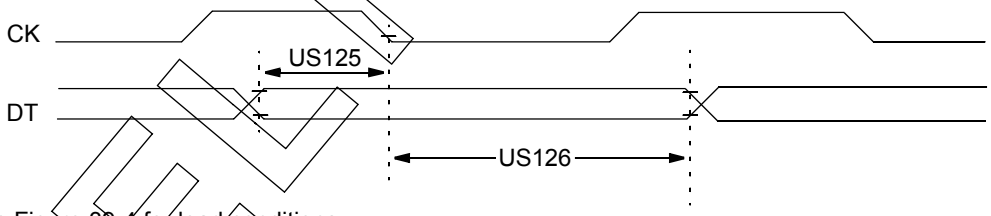


Note: Refer to Figure 39-4 for load conditions.

TABLE 39-22: EUSART SYNCHRONOUS TRANSMISSION CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US120	TCKH2DTV	SYNC XMIT (Master and Slave) Clock high to data-out valid	—	80	ns	3.0V ≤ VDD ≤ 5.5V
			—	100	ns	1.8V ≤ VDD ≤ 5.5V
US121	TCKRF	Clock out rise time and fall time (Master mode)	—	45	ns	3.0V ≤ VDD ≤ 5.5V
			—	50	ns	1.8V ≤ VDD ≤ 5.5V
US122	TDTRF	Data-out rise time and fall time	—	45	ns	3.0V ≤ VDD ≤ 5.5V
			—	50	ns	1.8V ≤ VDD ≤ 5.5V

FIGURE 39-16: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



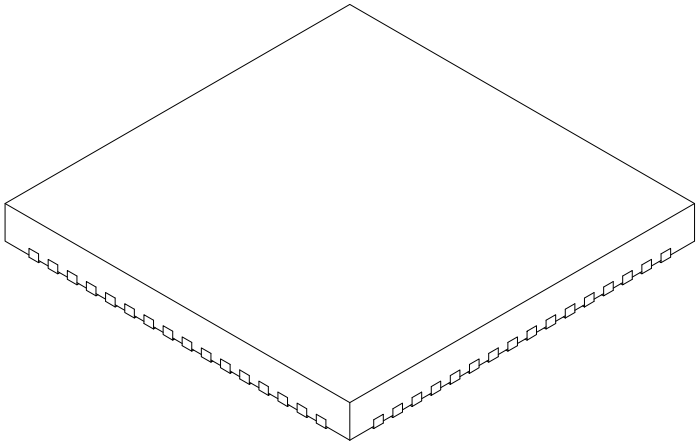
Note: Refer to Figure 39-4 for load conditions.

TABLE 39-23: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-setup before CK ↓ (DT hold time)	10	—	ns	
US126	TCKL2DTL	Data-hold after CK ↓ (DT hold time)	15	—	ns	

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2