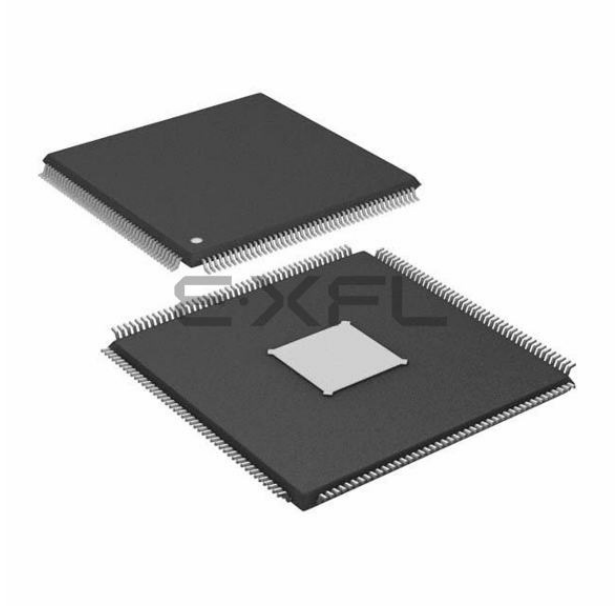
Renesas Electronics America Inc - R7S910001CFP#AA0 Datasheet



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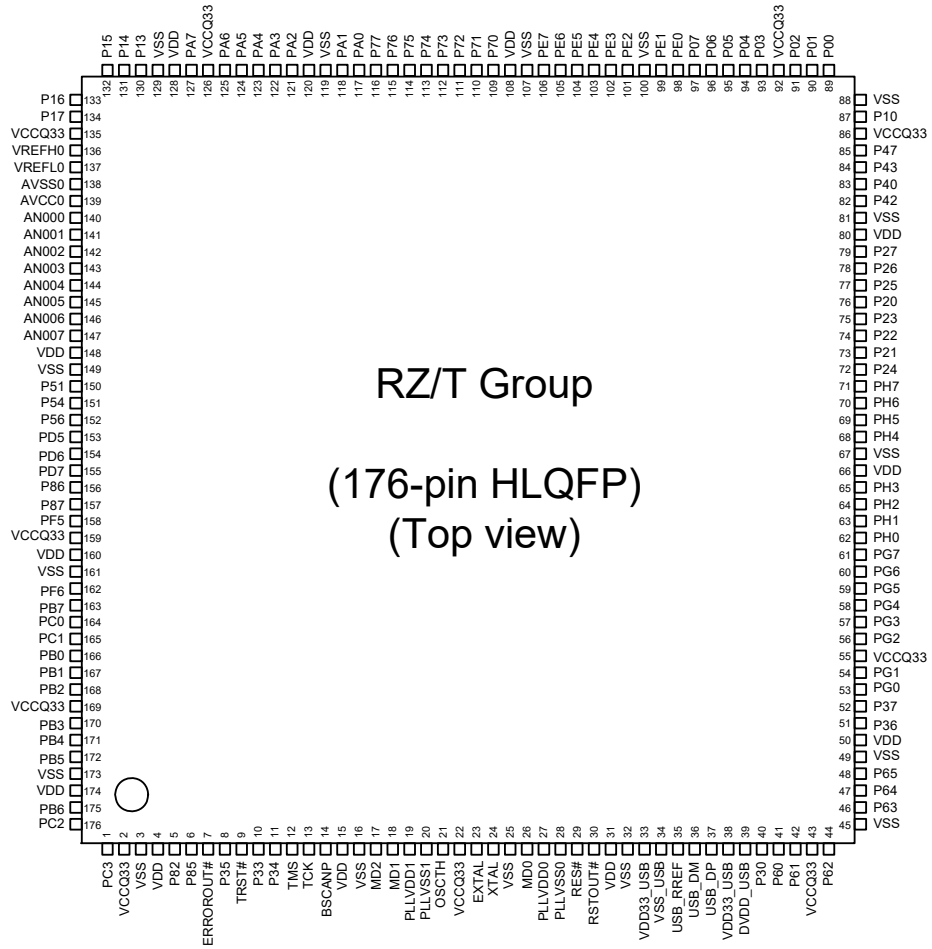
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R4F
Core Size	32-Bit Single-Core
Speed	450MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	97
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	544K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910001cfp-aa0

Table 1.1 Outline of Specifications (2 / 7)

Classification	Module/Function	Description
Low power	Low power consumption	• Standby mode (Cortex-R4) • Sleep mode (Cortex-M3) (for products incorporating an R-IN engine) • Module stop function
Interrupt	Cortex-R4 vector interrupt controller (VIC)	• Peripheral function interrupts: 273 sources / 276 sources (for products incorporating an R-IN engine) • External interrupts: 20 sources (NMI, IRQ0 to IRQ15, ETH0_INT, ETH1_INT, and ETH2_INT pins) • Software interrupts: 1 source • Non-maskable interrupts: 2 sources • Sixteen levels specifiable for the order of priority
	Cortex-M3 nested-type vector interrupt controller (NVIC) (only included in products incorporating an R-IN engine)	• Peripheral function interrupts: 82 sources • External interrupts: 19 sources (IRQ0 to IRQ15, ETH0_INT, ETH1_INT, and ETH2_INT pins) • Software interrupts: 1 source • Non-maskable interrupts: 1 source • Sixteen levels specifiable for the order of priority
External bus extension	Bus state controller (BSC)	• The external address space is divided into six areas (CS0 to CS5) for management. • The following features settable for each area independently. Bus size (8, 16, or 32 bits): Available sizes depend on the area. Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas) Idle wait cycle insertion (between same area access cycles or different area access cycles) Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. • Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing can be selected by software) • SDRAM refresh Auto refresh or self-refresh mode selectable • SDRAM burst access
Data transfer	Direct memory access controller (DMAC)	• 2 units (16 channels for unit 0, 16 channels for unit 1) • Transfer modes: Single transfer mode and block transfer mode • Transfer size Unit 0: 1/2/4/16/32/64 bytes Unit 1: 1/2/4/16 bytes • Activation sources: Software trigger, external DMA requests (DREQ0 to DREQ2), external interrupts, and interrupt requests from peripheral functions
I/O ports	General-purpose I/O ports	• 320-pin FBGA I/O pins: 209 Input pins: 9 Pull-up/pull-down resistors: 209 5-V tolerance: 9 • 176-pin HLQFP I/O pins: 97 Input pins: 5 Pull-up/pull-down resistors: 97 5-V tolerance: 5
Event link controller (ELC)		• 87 event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event-linked operation of signals of ports B and E is to be possible.
Multi-function pin controller (MPC)		The locations of input/output functions are selectable from among multiple pins.



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (176-Pin HLQFP).

Figure 1.3 Pin Arrangement (176-pin HLQFP)

Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8)

Pin Number	Pin Name
C5	PL5 / ETH2_RXD2 / TIOCA8
C6	PB6 / ETH_MDC / TCLKA / SCK3 / RTS4# / MISO3
C7	PB3 / IRQ3 / CS1# / ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1 / MCLK0
C8	PB1 / ETH1_RXER / MTCLKA / TCLKC / CTS4#
C9	PF5 / ETH1_TXEN / MTIOC4A / GTIOC1A / TIC2
C10	P87 / AN1_ANEX1 / A23 / ETH1_TXC / ETH0_RXD0 / MTIOC4C / GTIOC1B / MCLK1
C11	PD6 / AN114 / A22 / ETH1_TXD2 / ETH0_TXD1 / TIC1 / MISO2 / MCLK2
C12	P53 / ETH1_INT / MISO2
C13	P51 / IRQ1 / PHYLINK1 / RSPCK2
C14	AN004
C15	AN000
C16	VREFL0
C17	VREFH0
C18	PD2 / AN110 / WAIT#
C19	P14 / CAS# / MTIOC4A / GTIOC1A / ENCIF10
C20	P13 / RAS# / MTIOC4C / GTIOC1B
D1	P81 / ETH0_RXER / TIOCC0 / CTS4#
D2	P80 / IRQ8 / ETH0_RXDV / TIOCC3 / RTS4#
D3	PU3 / ETH2_COL / TIOCD6 / TXD3
D18	PD0 / AN108 / CS4#
D19	P96 / AN106 / POE0# / POE10# / ENCIF09
D20	P95 / AN105 / IRQ13 / MTCLKA / CTS2#
E1	P84 / ETH0_COL / CATLINKACT1 / RXD4
E2	P82 / ETH0_TXEN / ETH1_CRS / TIOCD3 / SCK4 / RTS3# / USB_OVRCUR
E3	PU1 / ETH2_RXC / TIOCA11 / SCK3
E5	PU0 / ETH2_RXER / TIOCA10
E6	PL6 / ETH2_RXD3 / TIOCA9
E7	PL4 / IRQ4 / ETH2_RXD1
E8	PL2 / ETH2_TXEN / TIOCA6 / ADTRG1
E9	PL0 / ETH2_TXD0 / TIOCB9
E10	PK7 / ETH2_TXD2 / TIOCB7
E11	PK6 / ETH2_TXD3 / TIOCB6
E12	PD5 / AN113 / A21 / ETH1_TXD3 / ETH0_TXD0 / TIC0 / SSL20 / MCLK3
E13	P56 / BS# / ETH1_TXER
E14	PD4 / AN112 / ETH2_INT
E15	VCCQ33
E16	PD1 / AN109 / CS1#
E18	P97 / AN107 / IRQ7 / A25 / ADTRG1
E19	P94 / AN104 / IRQ4 / MTCLKB / RTS2# / ENCIF08
E20	P93 / AN103 / MTIOC1A / TIC3 / SCK2 / ENCIF07
F1	PC4 / CATI2CCLK / TCLKH / SCL0
F2	P83 / IRQ11 / ETH0_CRS / CATLINKACT0 / TXD4
F3	P85 / IRQ5 / CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN
F5	PU4 / MII2_MDC / TIOCC9 / CTS3#
F6	VSS

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
V12		P20	A17	MTCLKD				
V13		P21	CS0#	MTIC5V / TIOCB1	CTS0#		IRQ1	
V14	VSS							
V15		P45	CS2#					
V16		P46	CKE					
V17		PS2		MTIOC7C		SSIWS0		
V18		P05	D5	MTIOC3A				
V19		P01	D1	MTIC5W / TIOCA2				
V20		P02	D2	MTIC5V / TIOCA3				
W1		P62			SPBCLK			
W2		P65	DREQ0		SPBIO2			
W3		PN5		MTIOC6A / TIOCD9		ENCIF10	IRQ5	
W4		PN6		MTIOC3C / TIOCC9		MCLK3 / ENCIF11		
W5		PP0	TEND0	POE8#		MCLK2		
W6		PP2		MTIOC0C / TCLKH		MCLK1		
W7		PP4		MTIOC0A		MCLK0		
W8	TRACECTL	PP6		TIOCA11	RXD1	ENCIF06		
W9	TRACECLK	PP7	DACK1	TCLKF / TCLKH	SCK1			
W10	TRACEDATA1	PR1	TEND1	POE4#	CTS1#	ENCIF08	IRQ9	
W11	TRACEDATA3	PR3		TIOCA10 / TIOCB10		ENCIF01		
W12	TRACEDATA5	PR5		TIOCA8 / TIOCB8		ENCIF03		
W13		P24	RD/WR#		RXD0		IRQ12	
W14		P22	RD#	MTIOC7B / TIOCD0	SCK0		IRQ2	
W15		P44	WAIT#	TCLKD	CTS0#		IRQ12	ADTRG0
W16		P43	WE2#/ DQMUL	MTIOC8B	USB_VBUSEN			
W17		PS1		MTIOC7B		SSISCK0	IRQ1	
W18		PS3		MTIOC7A		SSIRXD0		
W19		PS4		MTIOC6D		SSITXD0		
W20		PS5		MTIOC6B				
Y1	VSS							
Y2		P67	TEND0	GTIOC3B	CTXD0 / USB_OVRCUR		IRQ15	
Y3		P66	DACK0	GTIOC3A	CTXD1 / USB_VBUSEN		IRQ14	
Y4		PN7	DREQ0	MTIOC3A / TIOCD6		MDAT3 / ENCIF12		
Y5		PP1	DACK0	MTIOC0D		MDAT2		
Y6		PP3		MTIOC0B / TCLKC		MDAT1		
Y7		PP5		PO22		MDAT0		
Y8	VSS							
Y9	TRACEDATA0	PR0	DREQ1	TCLKE / TCLKG	TXD1	ENCIF07		
Y10	TRACEDATA2	PR2		TIOCA11 / TIOCB11	RTS1#	ENCIF00		

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V

Item	Symbol	Value	Unit
Power supply voltage (I/O)	VCCQ33	–0.3 to +4.2	V
Power supply voltage (internal)	VDD	–0.3 to +1.6	V
PLL power supply voltage	PLLVDD0, PLLVDD1	–0.3 to +1.6	V
Input voltage (except for ports for 5-V tolerant*1)	V_{in1}	–0.3 to VCCQ33 + 0.3*5	V
Input voltage (ports for 5-V tolerant*1)	V_{in2}	–0.3 to +5.5*3	V
Analog power supply voltage	AVCC0, AVCC1*2	–0.3 to +4.2	V
Reference power supply voltage	VREFH0, VREFH1	–0.3 to (AVCC0, AVCC1) + 0.3*5	V
USB digital power supply voltage	DVDD_USB	–0.3 to +1.6	V
USB power supply voltage	VDD33_USB*2	–0.3 to +4.2	V
Analog input voltage	V_{AN}	–0.3 to (AVCC0, AVCC1) + 0.3*5	V
Operating temperature (junction temperature)	Tj*4	–40 to +125	°C
Storage temperature	T_{stg}	–55 to +125	°C

[Usage Notes]

1. Do not directly connect output pins (I/O pins in output state) of IC products to other output pins (including I/O pins in output state) , power pins, or GND pins. However, output pins are directly connectable in an external circuit where timing design is provided to avoid conflict of outputs of high-impedance pins such as I/O pins.
2. If even a single item exceeds the absolute maximum rating for even a moment, it may degrade the product's quality. In other words, the absolute maximum rating is a rated value that potentially causes physical damage to products. Use products with a margin of the absolute maximum rating.
   Specified values and conditions shown in DC characteristics and AC characteristics are the range of normal operation and quality assurance of products.

Note 1. Ports PC0 to PC7 and P30 are 5-V tolerant.
Note 2. When the A/D converter unit 0 is not to be used, connect the AVCC0 and VREFH0 pins to VCCQ33 and the AVSS0 and VREFL0 pins to VSS, respectively. Do not leave these pins open. In the same way, when the A/D converter unit 1 is not to be used, connect the AVCC1 and VREFH1 pins to VCCQ33 and the AVSS1 and VREFL1 pins to VSS, respectively. Do not leave these pins open. When the USB is not to be used, connect the VDD33_USB pin to VCCQ33, the VSS_USB pin to VSS, and the DVDD_USB pin to VDD, respectively. Do not leave these pins open.
Note 3. When VCCQ33 is less than 3.0 V, the rated value of ports for 5-V tolerant is 3.6 V.
Note 4. For operations at the temperatures over 110°C (junction temperature), refer to the RZ/T1 Group Application Note: Precautions for High-Temperature Operations (R01AN3116).
Note 5. Do not exceed the absolute maximum rating, 4.2 V.

Table 2.12 CLKOUT25Mn Timing

Output load conditions: V_{OH} = 2.0 V, V_{OL1} = 0.8 Vn, C = 25 pF (RMII)
V_{OH} = VCCQ33 – 0.5 V, V_{OL1} = 0.4 V, C = 30 pF (MII)

Item		Symbol	min	max	Unit	Test Conditions
CLKOUT25Mn (RMII)	CLKOUT25Mn cycle time	T_{ck}	20	—	ns	Figure 2.3
	CLKOUT25Mn frequency Typ. 50 MHz	—	—	50 + 50 ppm	MHz	
	CLKOUT25Mn duty	—	35	65	%	
	CLKOUT25Mn output low pulse width 1	T_{ckl1}	$T_{ck}/2 - T_{ckf1}$	$T_{ck}/2 + T_{ckf1}$	ns	
	CLKOUT25Mn output high pulse width 1	T_{ckh1}	$T_{ck}/2 - T_{ckr1}$	$T_{ck}/2 + T_{ckr1}$	ns	
	CLKOUT25Mn rising/falling time 1	$T_{ckr1/ckf1}$	0.5	4	ns	
CLKOUT25Mn (MII)	CLKOUT25Mn cycle time	T_{ck}	40	—	ns	Figure 2.4
	CLKOUT25Mn frequency Typ. 25 MHz	—	—	25 + 50 ppm	MHz	
	CLKOUT25Mn duty	—	35	65	%	
	CLKOUT25Mn output low pulse width 2	T_{ckl2}	$T_{ck}/2 - T_{ckf2}$	$T_{ck}/2 + T_{ckf2}$	ns	
	CLKOUT25Mn output high pulse width 2	T_{ckh2}	$T_{ck}/2 - T_{ckr2}$	$T_{ck}/2 + T_{ckr2}$	ns	
	CLKOUT25Mn rising/falling time 2	$T_{ckr2/ckf2}$	0.5	9	ns	

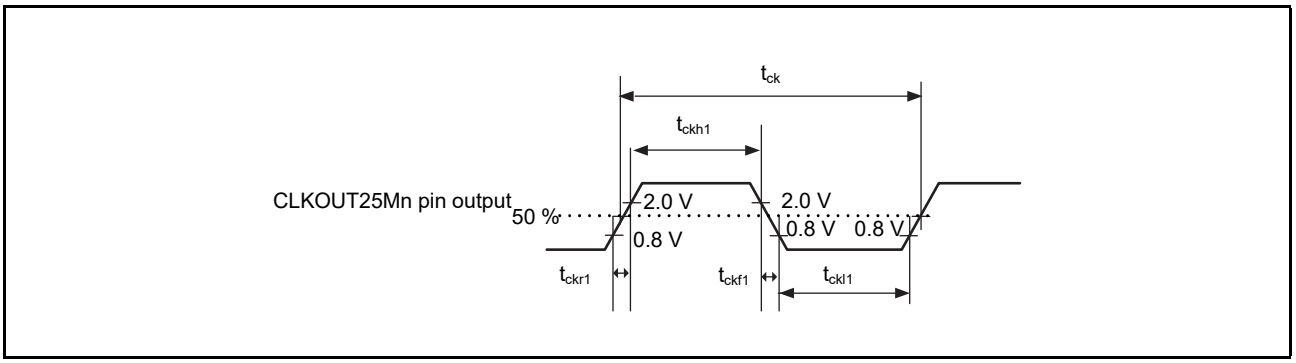


Figure 2.3 CLKOUT25Mn Pin Output Timing 1

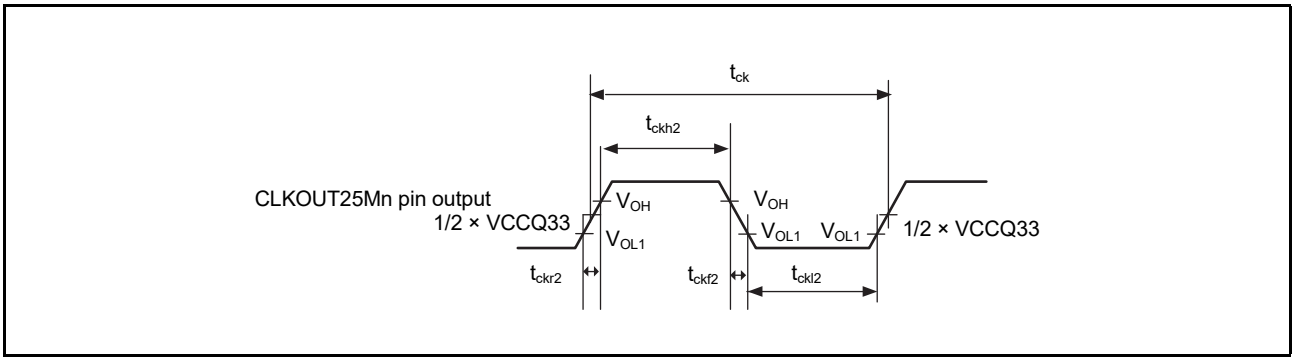


Figure 2.4 CLKOUT25Mn Pin Output Timing 2

Table 2.13 EXTAL Clock Timing

Item	Symbol	min	typ	max	Unit
EXTAL external clock input cycle time	t_{EXcyc}	40.00 + 50 ppm			ns
		25.00 ± 25ppm*1			MHz

Note 1. When EtherCAT is in use

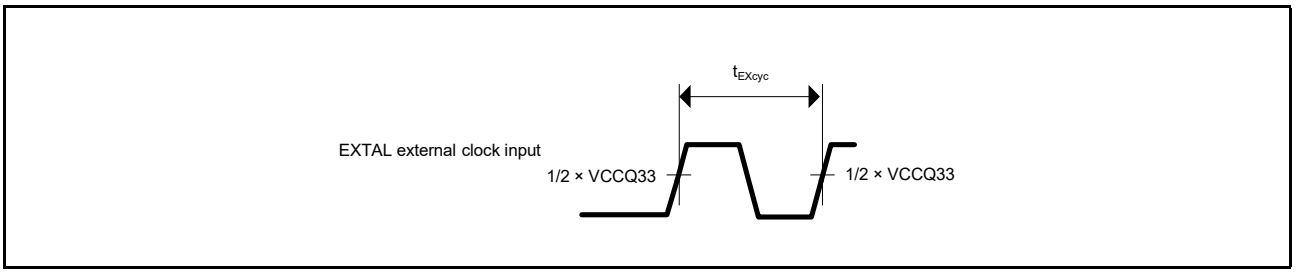


Figure 2.5 EXTAL External Clock Input Timing

Table 2.14 XTAL Clock Timing

Item	Symbol	min	typ	max	Unit
XTAL clock oscillator output cycle*1	$t_{XTALcyc}$		40.00 + 50 ppm*2		ns

Note 1. When using the XTAL clock, ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.
Note 2. When using the EtherCAT, make sure that the clock timing satisfies 25.00 MHz ± 25 ppm.

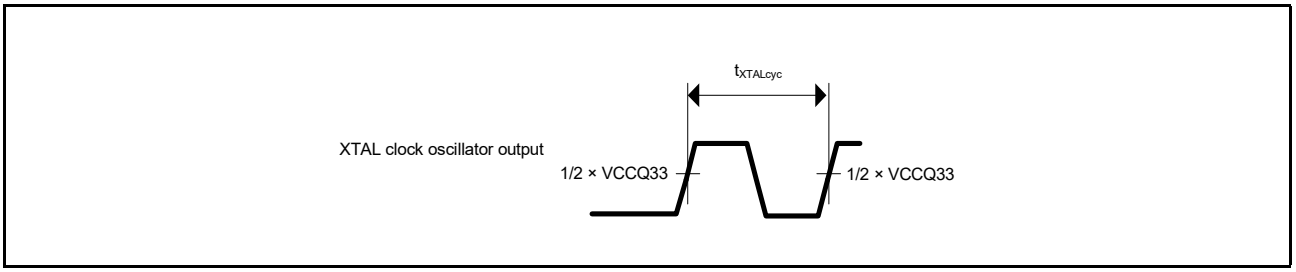


Figure 2.6 XTAL Clock Oscillator Output Timing

Table 2.15 LOCO Clock Timing

Item	Symbol	min	typ	max	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.62	4.17	3.79	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	40	µs	Figure 2.7

2.4.2 Reset Timing and Interrupt Timing

Table 2.16 Reset Timing and Interrupt Timing

Item		Symbol	Min*1	typ	max	Unit	Test Conditions
RES# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	Figure 2.8
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
RES# rising time		$T_{risereset}$	—	—	150	µs	
TRST# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
TRST# rising time		$T_{risereset}$	—	—	150	µs	
NMI pulse width		t_{NMIW}	t_{Icyc} × 2	—	—	ns	Figure 2.9
IRQ pulse width		t_{IRQW}	t_{Icyc} × 2	—	—	ns	Figure 2.10
ETH_INT pulse width		t_{EINTW}	t_{Icyc} × 2	—	—	ns	Figure 2.11

Note 1. t_{Icyc}: ICLK cycle

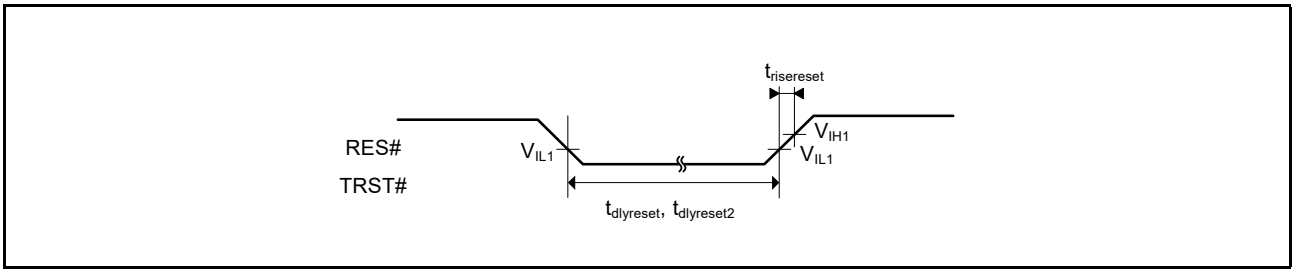


Figure 2.8 Reset Input Timing

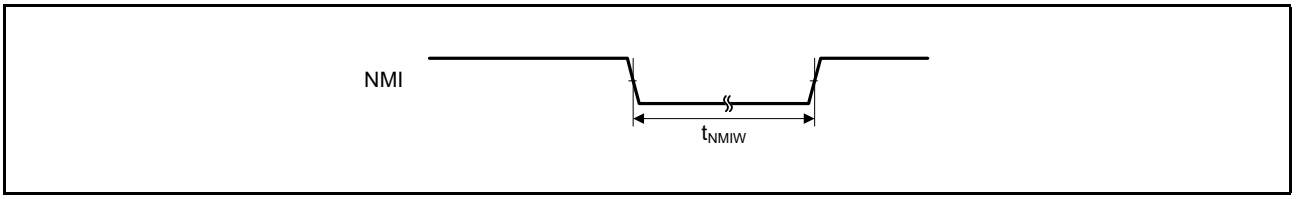


Figure 2.9 NMI Interrupt Input Timing

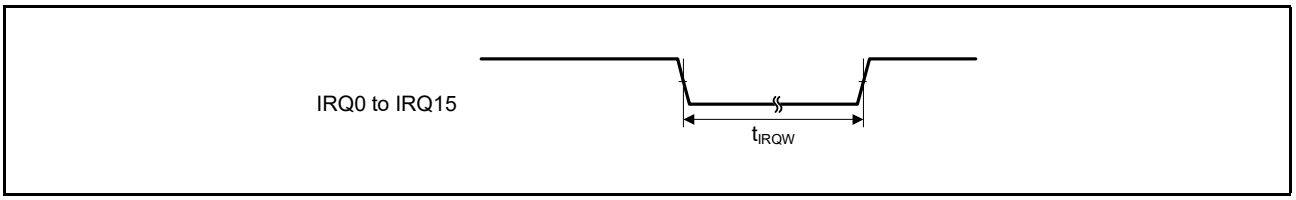
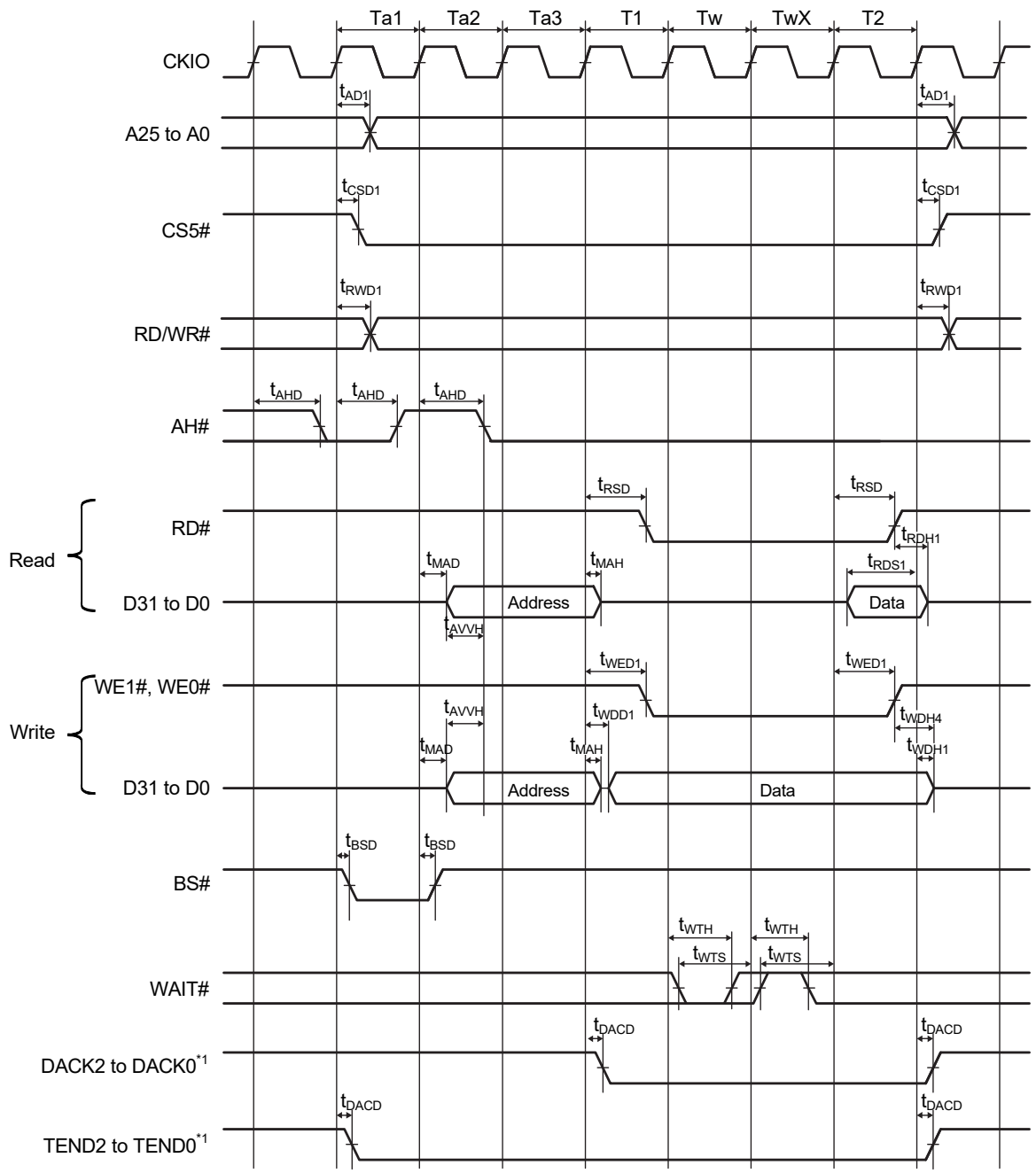
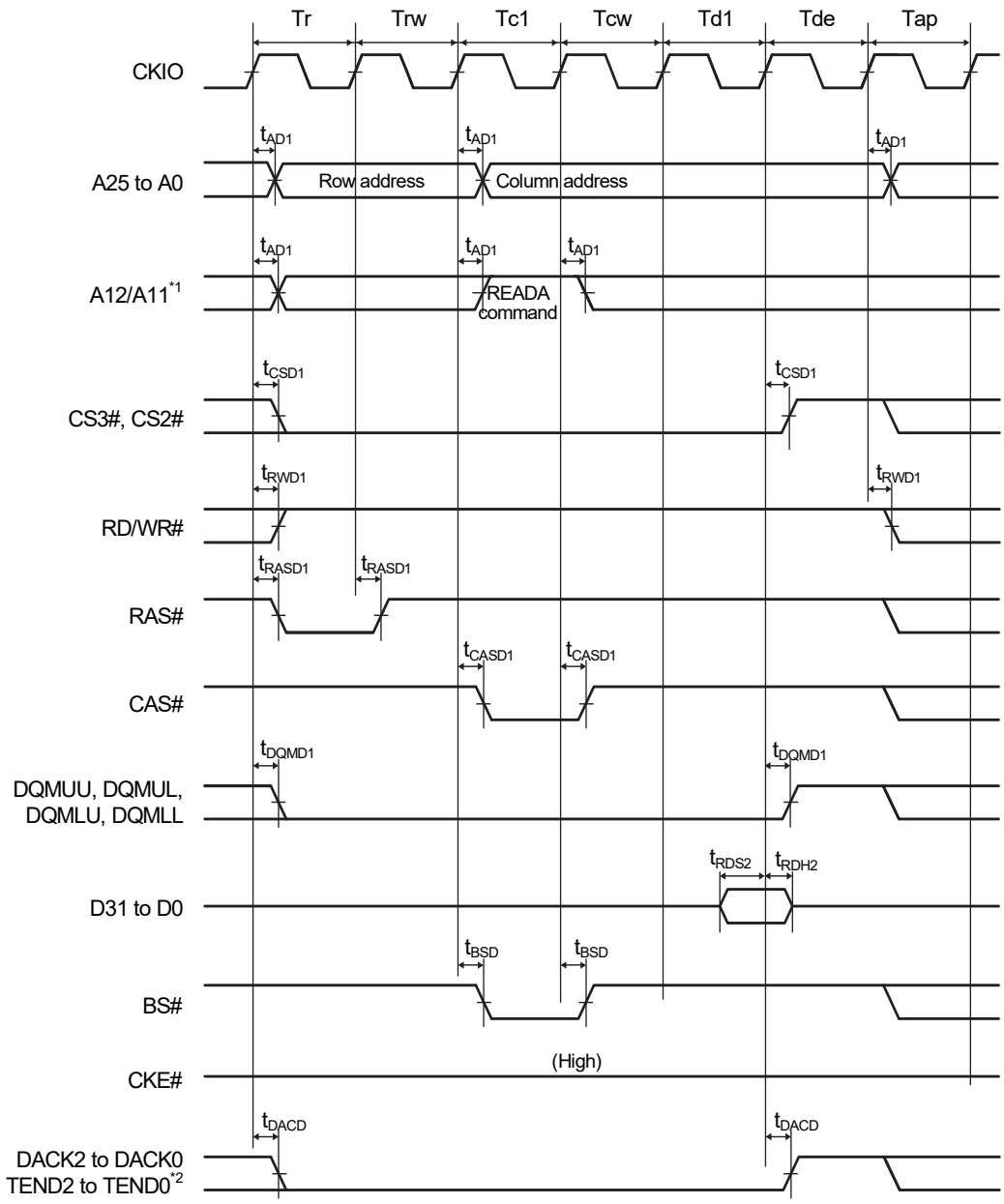


Figure 2.10 IRQ Interrupt Input Timing



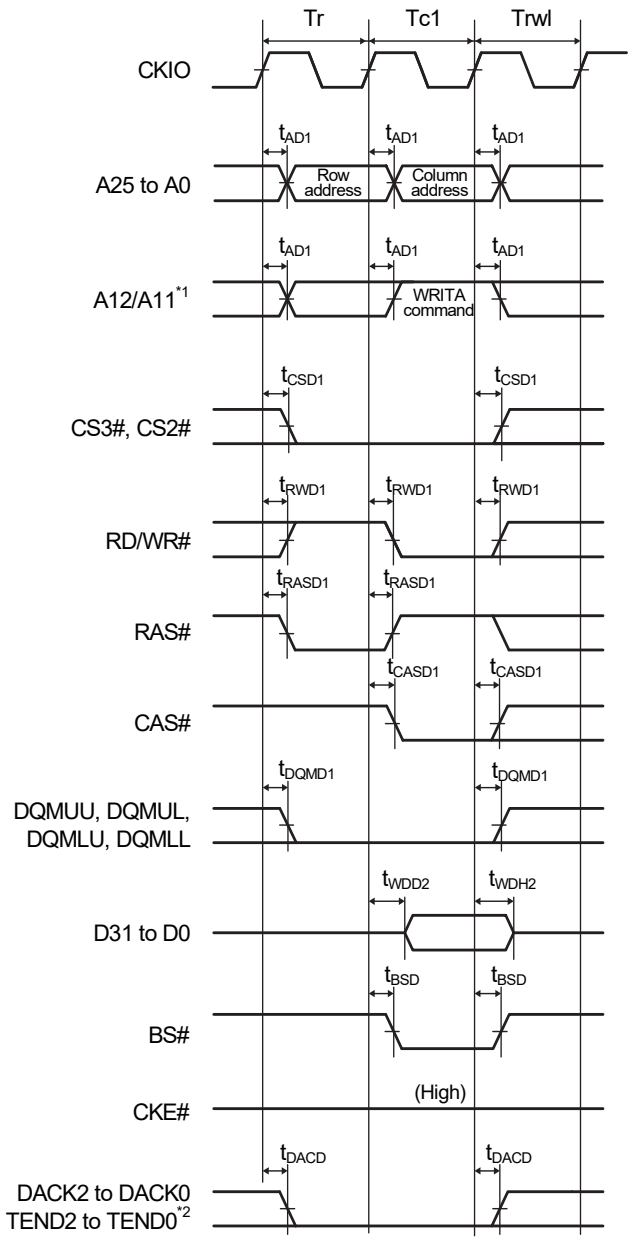
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.16 MPX-I/O Interface Bus Cycle (Address Cycle 3, Software Wait 1, External Wait 1 Inserted)



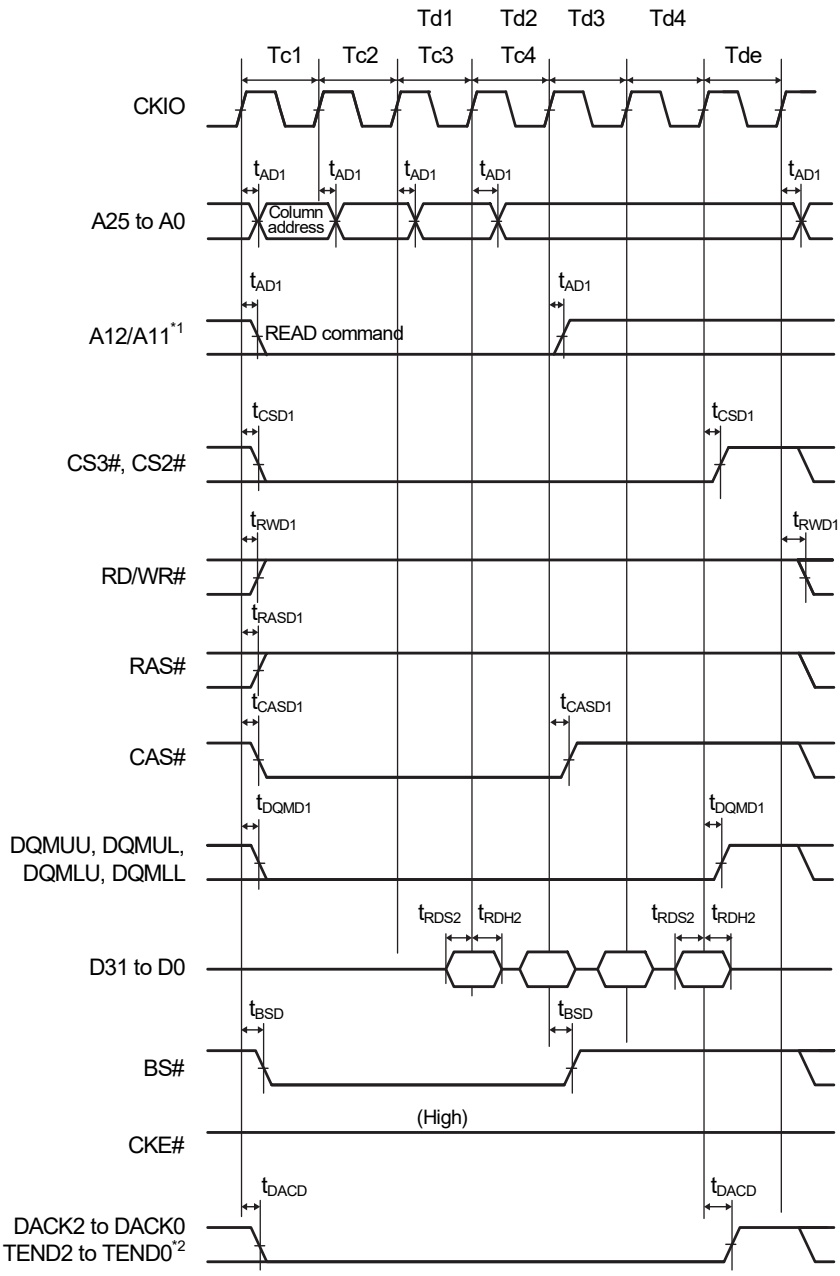
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.21 Synchronous DRAM Single-Read Bus Cycle (with Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 1 Cycle)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.24 Synchronous DRAM Single-Write Bus Cycle (with Auto Precharge, TRWL = 1 Cycle)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.29 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: READ Command, Same Row Address, CAS Latency 2, WTRCD = 0 Cycles)

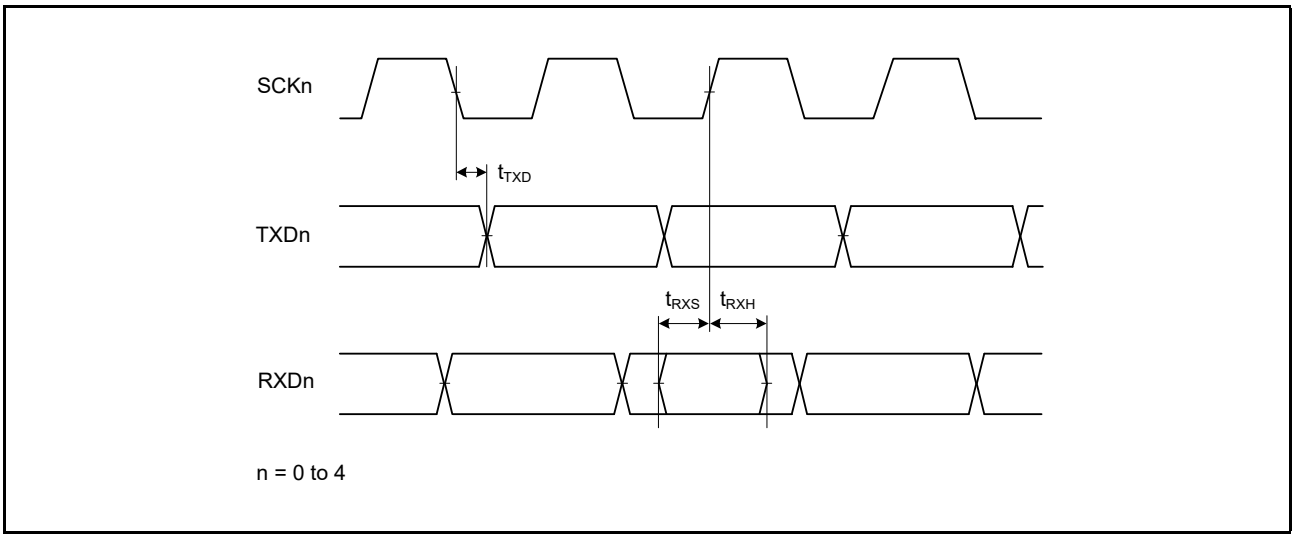


Figure 2.51 SCIFA Input/Output Timing/Clock Synchronous Mode

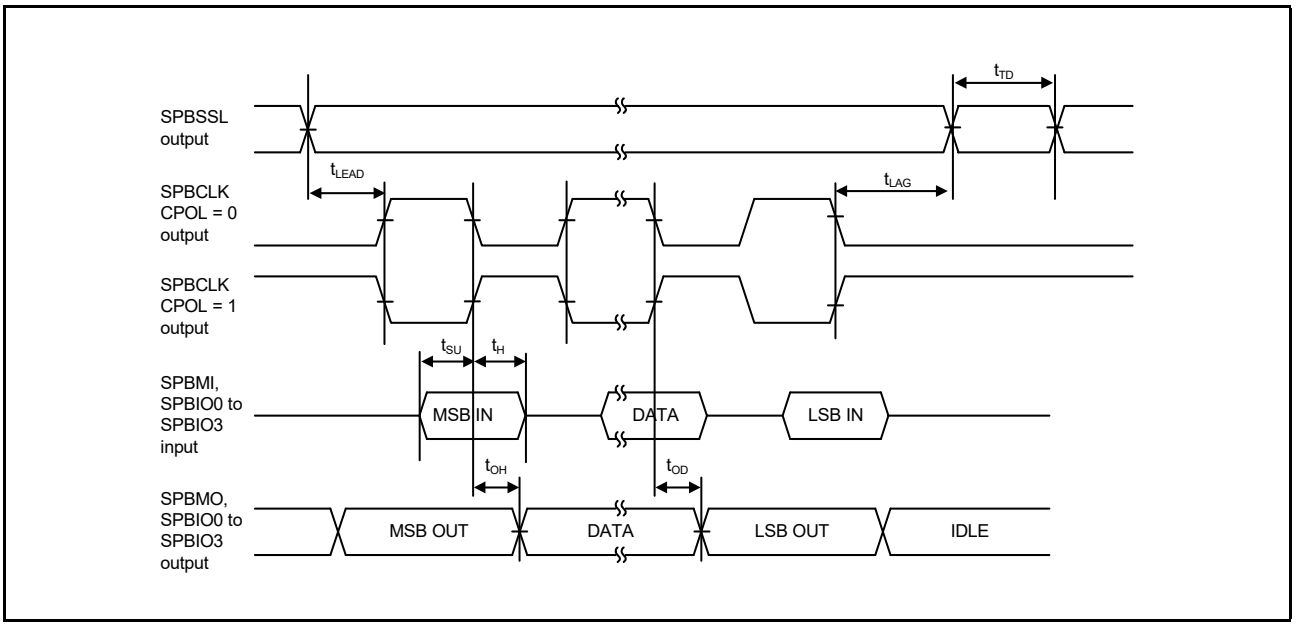


Figure 2.60 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1)

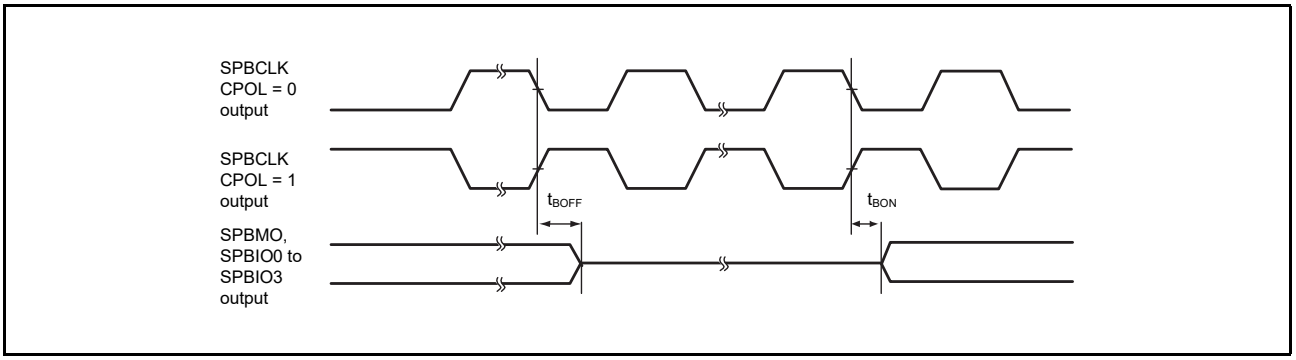


Figure 2.61 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 0)

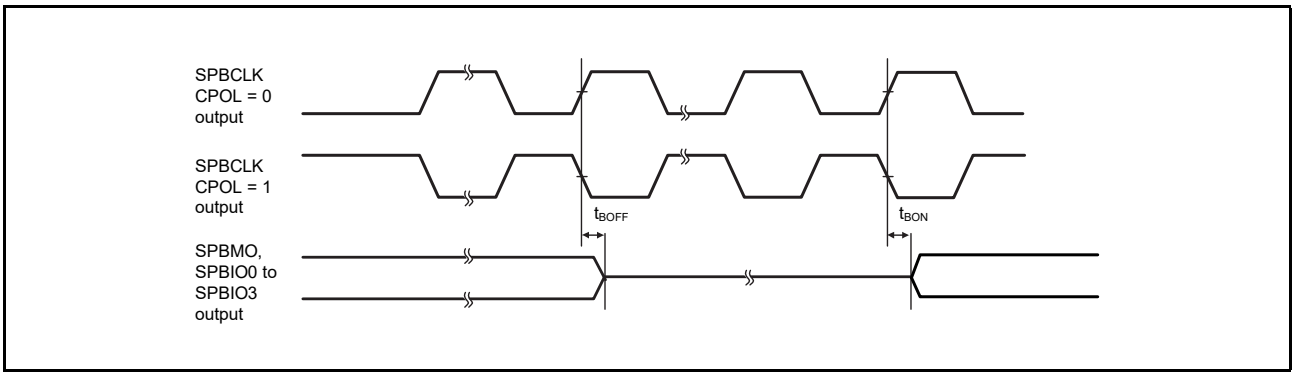


Figure 2.62 SPIBSC Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)

2.4.5.13 CAN Interface Timing

Table 2.31 CAN Interface Timing

Item	Symbol	min	max	Unit	Test Conditions
Internal delay time	tnode	—	100	ns	Figure 2.69
Transmission rate		—	1	Mbps	

Internal delay time (tnode) = Internal transmission delay time (toutput) + Internal reception delay time (tinput)

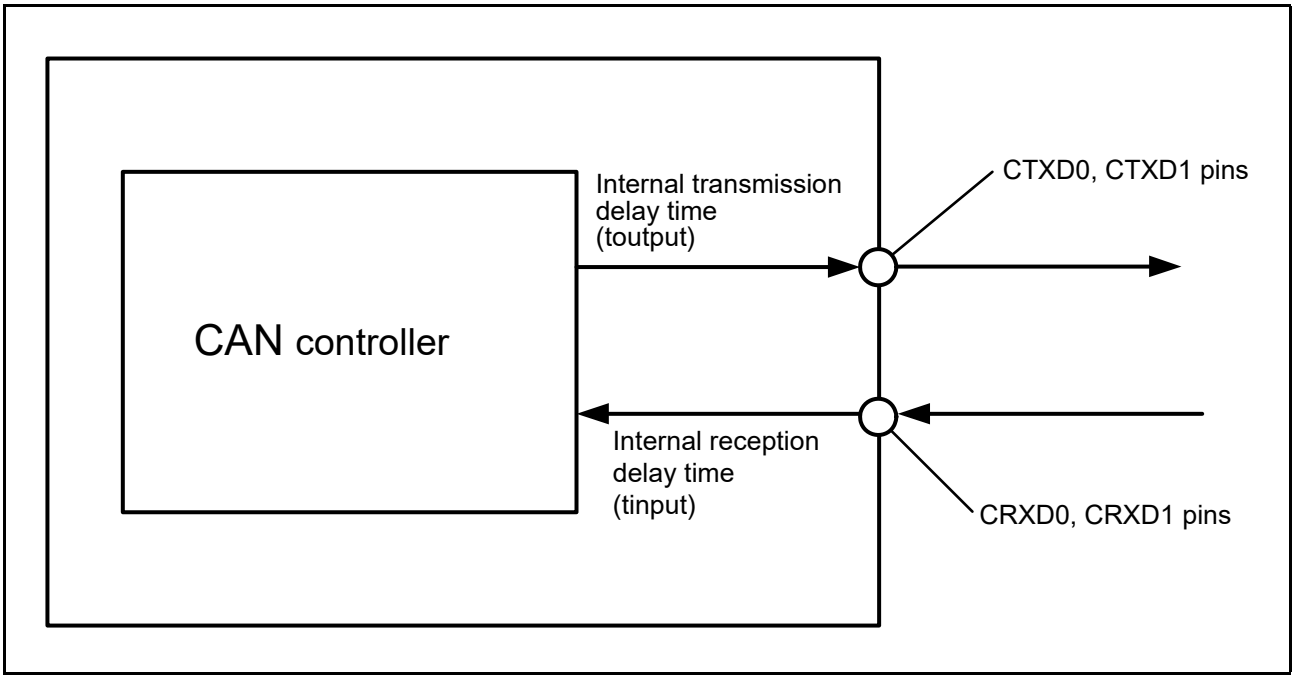


Figure 2.69 CAN Interface Conditions

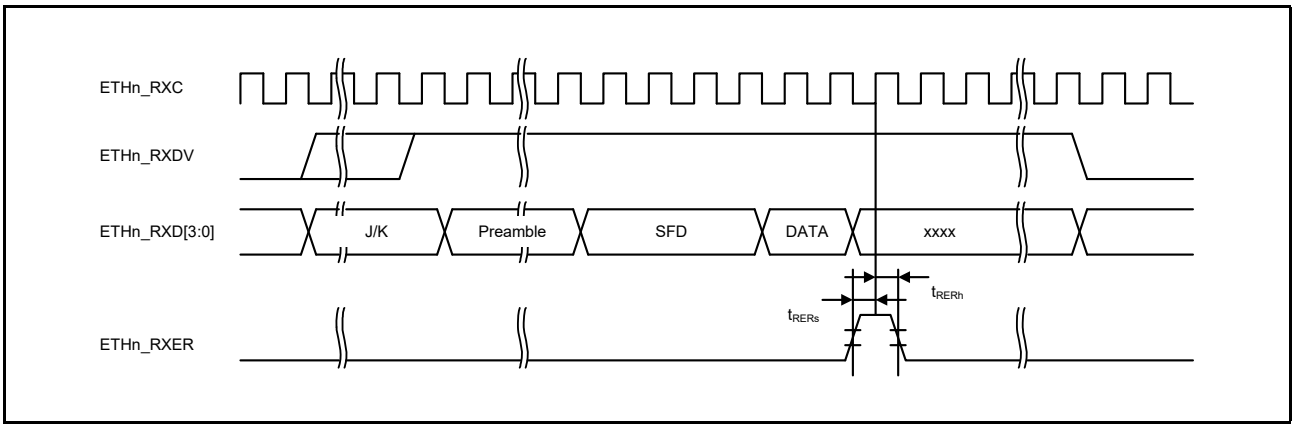


Figure 2.77 MII Reception Timing (Error Occurrence)

2.4.5.16 Delta-Sigma Interface Timing

Table 2.34 ΔΣ Interface Timing

Conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol	min	max	Unit	Test Conditions
DSMIF	Clock cycle	Master	t_{DScyc}	1	1	t_{DCcyc}	Figure 2.79
		Slave		40	200	ns	
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		16	—	ns	
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		16	—	ns	
	Setup time	Master	t_{SU}	15	—	ns	Figure 2.80, Figure 2.81
		Slave		10	—	ns	
	Hold time	Master	t_H	0	—	ns	
		Slave		10	—	ns	

Note: t_{DCcyc}: One cycle time of the ΔΣ interface clock (DSCLK0, DSCLK1)

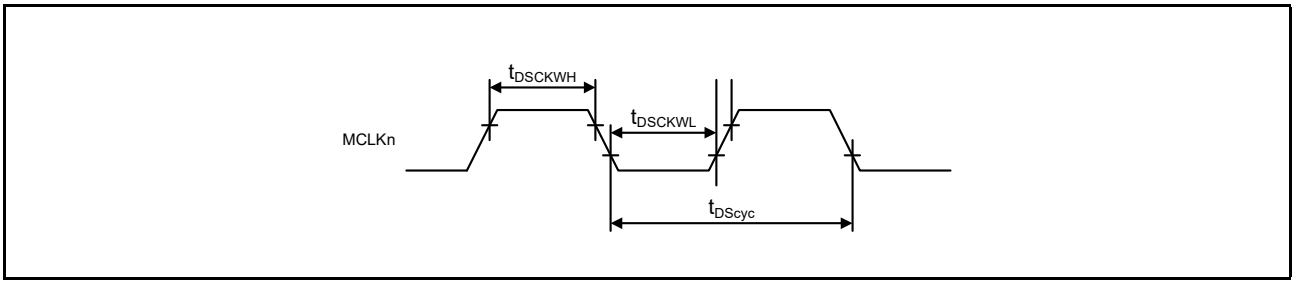


Figure 2.79 Clock Input/Output Timing

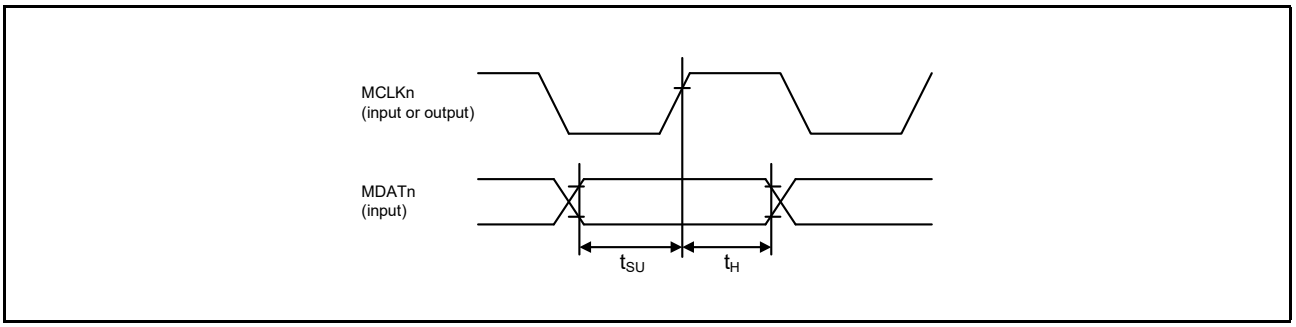


Figure 2.80 Reception Timing (MCLKn Rising Synchronous)

2.6 A/D Conversion Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 2.37 12-Bit A/D (Unit 0) Conversion Characteristics

Item		min	typ	max	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN003) When disconnection detection assistance is in use	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0kΩ	1.2 (0.4 + 0.4) *2	—	3.6	µs	• Sampling of channel dedicated sample-and-hold circuits in 24 states • Sampling in 24 states
	Offset error	—	—	±7.5	LSB	
	Full-scale error	—	—	±7.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±7.5	LSB	
	DNL differential nonlinearity error	—	—	±3.0	LSB	
	INL integral nonlinearity error	—	—	±4.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	3.2	µs	Self-diagnosis + 4-channel simultaneous sampling
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN003) When disconnection detection assistance is not in use	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0kΩ	1.2 (0.4 + 0.4) *2	—	3.6	µs	• Sampling of channel dedicated sample-and-hold circuits in 24 states • Sampling in 24 states
	Offset error	—	—	±6.5	LSB	
	Full-scale error	—	—	±6.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.5	LSB	
	DNL differential nonlinearity error	—	—	±3.0	LSB	
	INL integral nonlinearity error	—	—	±4.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	3.2	µs	Self-diagnosis + 4-channel simultaneous sampling
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0kΩ	0.483 (0.267)*2	—	—	µs	Sampling in 16 states
	Offset error	—	—	±5.0	LSB	
	Full-scale error	—	—	±5.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	
	DNL differential nonlinearity error	—	—	±2.5	LSB	
	INL integral nonlinearity error	—	—	±3.0	LSB	

2.7 Temperature Sensor Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 2.39 Temperature Sensor Characteristics

Item	min	typ	max	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (at 25°C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	µs	
Sampling time	4.25	—	—	µs	ADSSTRT.SST[7:0] = 255 states (when PCLKF [ADC (unit0) sampling CLK] = 60 MHz)

2.8 Oscillation Stop Detection Timing

Table 2.40 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	min	typ	max	Unit	Test Conditions
Clock switching time	t_{dr}	—	—	1	ms	Figure 2.86

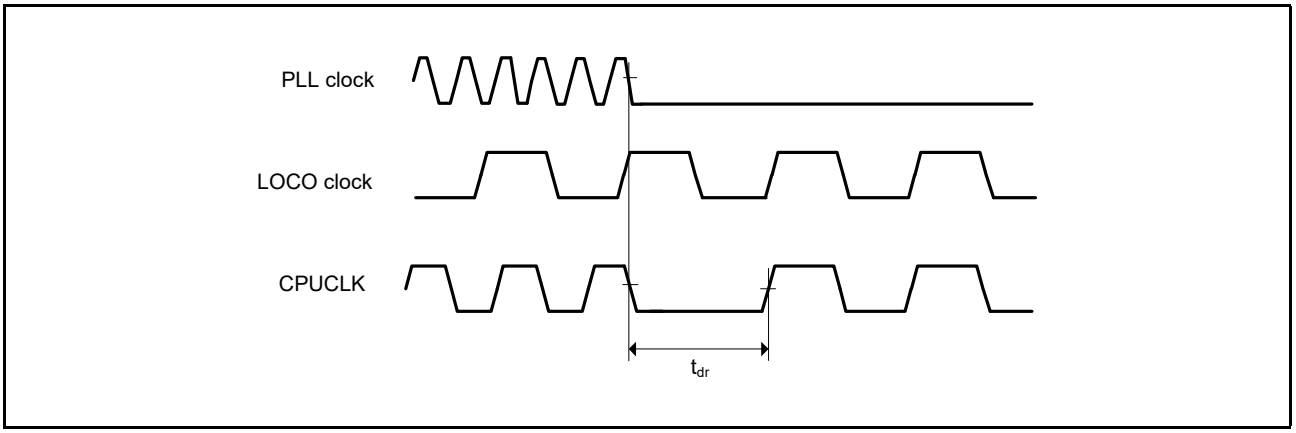


Figure 2.86 Oscillation Stop Detection Timing

REVISION HISTORY — RZ/T1 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.60	Nov. 14, 2014	—	First edition, issued
0.70	Dec. 25, 2014	Features	
		1	■ Operating temperature range: Heading title and description corrected
		Section 1 Overview	
		11	Table 1.3 List of Products (2 / 2): Note corrected
		21	Figure 1.3 Pin Arrangement (176-pin HLQFP): The names of pins 33, 34, 38, 39, and 91, corrected
		26	Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8): The names of pins M20 and P19, corrected
		27	Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8): The names of pins R14, R19, R20, T9, V7, and V8, corrected
		29	Table 1.5 Pin Assignments (320-Pin FBGA) (8 / 8): The names of pins Y16 and Y17, corrected
		30	Table 1.6 Pin Assignments (176-Pin HLQFP) (1 / 4): The names of pins 33, 34, 38, and 39, corrected
		31	Table 1.6 Pin Assignments (176-Pin HLQFP) (2 / 4): The names of pins 58, 59, 60, 79, 82, and 83, corrected
		32	Table 1.6 Pin Assignments (176-Pin HLQFP) (3 / 4): The names of pins 91 and 110, corrected
		33	Table 1.6 Pin Assignments (176-Pin HLQFP) (4 / 4): The names of pins 136, 153, 154, 155, 156, and 157, corrected
		39	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (6 / 10): The name of pin M20, corrected
		40	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10): The names of pins P19, R8, and R14, corrected
		41	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10): The names of pins R19, R20, T9, V7, and V8, corrected
		42	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10): The names of pins Y16 and Y17, corrected
1.10	Jul. 08, 2016	Feature	
		1	Wholly amended
		1. Overview	
		2 to 49	Wholly amended
		2. Electrical Characteristics	
		50 to 129	Newly added
1.20	Mar. 02, 2017	1. Overview	
		9	Table 1.2 Comparison of Functions for Different Packages: Functions of ETHERC and ECATC, modified. Note 1 added.
		12	Figure 1.1 Block Diagram: Functional blocks of ECATC and ETHERC, modified. Note 1 modified.
		20	Figure 1.2 Pin Arrangement (320-Pin FBGA) (Top View): Pin ERROROUT#, modified
		2. Electrical Characteristics	
		53	Table 2.3 DC Characteristics (2) [Power Supply] Test conditions, modified: Product part no. added
		55	Table 2.4 DC Characteristics (3) [Except for USB2.0 Host/Function-Related Pins] Item modified: "Input pull-up MOS current and resistance" and "Input pull-down MOS current and resistance" R_{pu1}, R_{pu2}, R_{pd1}, and R_{pd2} were added. Test conditions for "Input pull-down MOS current and resistance" were modified.
		58	Table 2.10 Operating Frequency: Notes 1 to 3, added. The max. value of the CPU clock (CPUCLK), modified.