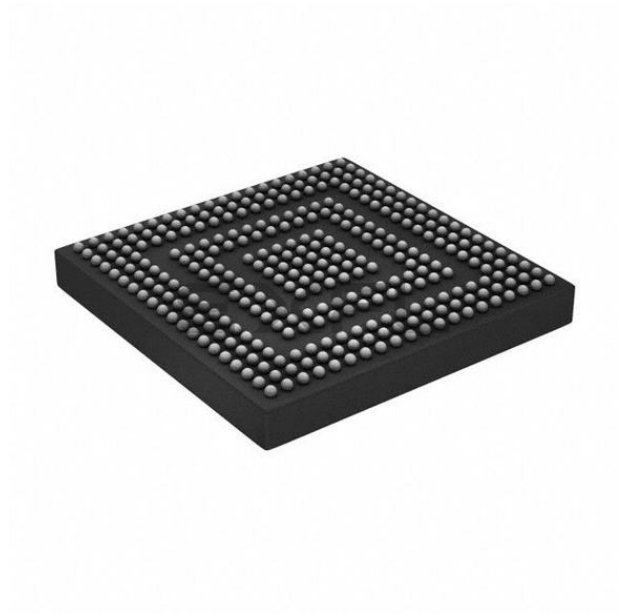
Renesas Electronics America Inc - R7S910002CBG#AC0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R4F
Core Size	32-Bit Single-Core
Speed	450MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	209
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	320-FBGA
Supplier Device Package	320-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910002cbg-ac0

Table 1.1 Outline of Specifications (5 / 7)

Classification	Module/Function	Description
Communication function	Ethernet MAC (ETHERC)	• 1 port • IEEE802.3 is supported • 10BASE and 100BASE are supported • Full duplex and half duplex are supported • Automatic pause packet transmission function • Auto broadcast suspension function by the pause packet reception • MII/RMII interface is supported
	Ethernet switch	• 2-port PHY interfaces • IEEE802.3 • 10BASE, 100BASE • Full and half duplex • Hardware switching, lookup, and filtering • QoS with frame prioritization • Priority control based on VLAN Priority (IEEE802.1q), which enables priority reassignment • Classification and priority assignment based on IPv4 DiffServ Code Point Field, IPv6 Class of Service • Queue with four priority levels • Multicasting and broadcasting • VLAN frame • IEEE1588 timer module • Cut-through and hub features • Device level ring (DLR)
	EtherCAT Slave Controller (ECATC) *2	• 1 channel (2 ports) *3 • EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented
	USB 2.0 HS host/ function module	• 1 port • Compliance with the USB 2.0 specification • Transfer rate High speed (480 Mbps), full speed (12 Mbps) • Communications buffer Incorporates 1 Kbyte of RAM for host mode Incorporates 8 Kbytes of RAM for function mode
	Serial communication interface with FIFO (SCIFA)	• 5 channels • Serial communications modes: Asynchronous, clock synchronous • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Both the transmission and reception sections are equipped with 16-byte FIFO buffers, allowing continuous transmission and reception. • Bit rate modulation
	I^2C bus interface (RIICa)	• 2 channels I^2C bus format Supports the multi-master Max. transfer rate: 400 kbps • Event linking by the ELC
	CAN module (RSCAN)	• 2 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • Message buffers Max. 64 × 2 channels of reception message buffers, which are used by all channels 16 transmission message buffers per channel • Max. transfer rate: 1 Mbps

Table 1.4 Pin Functions (6 / 7)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VDD33_USB	Input	Power supply input pin for USB
	VSS_USB	Input	Ground input pin for USB
	DVDD_USB	Input	Digital power supply input pin for USB
	USB_RREF	Input	Reference current input pin for USB. Connect this pin to the VSS_USB pin via 200Ω (±1%).
	USB_DP	I/O	USB bus D+ data I/O pin
	USB_DM	I/O	USB bus D- data I/O pin
	USB_VBUSEN	Output	Outputs the VBUS power enable signal for USB.
	USB_OVRCUR	Input	Inputs the overcurrent signal for USB.
	USB_VBUSIN	Input	USB cable connection/disconnection detection input pin
CAN module (RSCAN)	CRXD0 to CRXD1	Input	Receive data input pins
	CTXD0 to CTXD1	Output	Transmit data output pins
Serial peripheral interface (RSPIa)	RSPCK0 to RSPCK3	I/O	Clock I/O pins
	MOSI0 to MOSI3	I/O	Master transmit data I/O pins
	MISO0 to MISO3	I/O	Slave transmit data I/O pins
	SSL00, SSL10, SSL20, SSL30	I/O	Slave select signal I/O pins
	SSL01, SSL02, SSL03, SSL11	Output	Slave select signal output pins
SPI multi I/O bus controller (SPIBSC)	SPBCLK	Output	Clock output pin
	SPBSSL	Output	Slave select signal output pin
	SPBMO/SPBIO0	I/O	Master transmit data/data 0 I/O pin
	SPBMI/SPBIO1	I/O	Master input data/data 1 I/O pin
	SPBIO2, SPBIO3	I/O	Data 2, data 3 I/O pins
Serial sound interface (SSI)	SSISCK0	I/O	SSI serial bit clock I/O pin
	SSIWS0	I/O	Word select I/O pin
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
ΔΣ interface (DSMIF)	MCLK0 to MCLK3	I/O	Clock I/O pins
	MDAT0 to MDAT3	Input	Data input pins
12-bit A/D converter (S12ADCa)	AN000 to AN007, AN100 to AN115	Input	Analog input pins for A/D converter
	ADTRG0, ADTRG1	Input	External trigger input pins for the start of A/D conversion
	AN1_ANEX0	Output	Extended analog outpu pin
	AN1_ANEX1	Input	Extended analog input pin
Analog power supply	AVCC0	Input	Analog power supply input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Reference power supply input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.

Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8)

Pin Number	Pin Name
M5	BSCANP
M6	PLLVDD0
M8	VDD
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VDD
M15	VCCQ33
M16	PE6 / IRQ6 / D14 / MTIOC0A / TIOCD0 / RXD1 / MISO0 / TRACEDATA6
M18	P70 / IRQ0 / D16 / MTIOC6D / RTS1# / USB_OVRCUR / TRACECLK / ENCIF00
M19	PT4 / CS3# / PO29
M20	P71 / D17 / POE0# / POE10# / TOC2 / SCK1 / TRACECTL / ENCIF01
N1	VSS
N2	MD0
N3	RSTOUT#
N5	RES#
N6	PLLVSS0
N8	VDD
N9	VSS
N10	VDD
N11	VDD
N12	VDD
N13	VDD
N15	PE2 / IRQ2 / D10 / MTCLKC / TIOCB4 / SSL02 / TRACEDATA2
N16	PE4 / D12 / MTIOC0B / TIOCC0 / RTS1# / SSL00 / TRACEDATA4
N18	PE5 / D13 / MTIOC0C / TIOCC3 / TXD1 / MOSI0 / TRACEDATA5
N19	PT2 / TIOCA1 / TIOCB1 / PO27
N20	PT3 / IRQ11 / TIOCA0 / TIOCB0 / PO28 / CTS2# / ENCIF09
P1	VSS_USB
P2	VDD33_USB
P3	USB_RREF
P5	P31 / USB_VBUSEN
P6	VCCQ33
P15	P06 / D6 / MTIOC2B / TIOCB0
P16	P07 / D7 / MTIOC2A / TIOCB1
P18	PE3 / IRQ3 / D11 / MTIOC0D / TIOCB5 / CTS1# / SSL01 / TRACEDATA3
P19	PT0 / IRQ0 / TIOCA3 / TIOCB3 / PO25 / SCK2 / ENCIF07
P20	PT1 / TIOCA2 / TIOCB2 / PO26 / RTS2# / ENCIF08
R1	USB_DP
R2	USB_DM
R3	P30 / CRXD0 / USB_VBUSIN
R5	PN0 / MTIOC8D / SSL10
R6	PN2 / IRQ10 / MTIOC8B / MOSI1
R7	PG0 / A1 / PO2

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (1 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
A1	VSS							
A2		PC2			ETH0_TXC / ETH1_RXD2 / CATI2CDATA / SDA0			
A3		PJ3			ETH0_TXD0		IRQ11	ADTRG0
A4		PJ1			ETH0_TXD2 / CATLEDSTER / RSPCK3			
A5		PF7	A25		ETH0_TXER / RTS3# / SSL30		IRQ7	
A6		PB4	A24		ETH1_COL / ETH0_RXER / CATSYNC0 / CATLATCH0 / RXD3 / MOSI3	MDAT0		
A7		PB0		MTCLKB / TCLKD / TIC3	ETH1_RXDV			
A8		PC0	WAIT#	GTETRG	ETH1_RXD2 / SCL1	MDAT3		
A9		PF6		MTIOC3D / GTIOC0B / TOC2	ETH1_RXD0			
A10	VCCQ33							
A11		P54			CLKOUT25M1 / MOSI2			
A12	VSS							
A13								AN007
A14								AN005
A15								AN002
A16	AVCC0							
A17	AVCC1							
A18	VREFH1							
A19		P17	CS5#		ETH1_TXER / PHYRESETOUT#			ADTRG0
A20	VSS							
B1		PJ5		TIOCD0	ETH0_RXD1 / RXD3			
B2		PJ4			ETH0_RXD0 / TXD3			
B3		PC3			ETH0_RXC / ETH0_RXDV / CATI2CCLK / RXD4 / SCL0 / CRXD1			
B4		PJ2			ETH0_TXD1 / MISO3		IRQ10	
B5		PJ0			ETH0_TXD3 / CATLEDERR / MOSI3		IRQ8	
B6		PB5		TCLKB / POE0# / POE10#	ETH_MDIO / CTS3# / RSPCK3			

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
R16	VCCQ33							
R18	VCCQ33							
R19		PS6		TIOCA5 / TIOCB5 / PO23	RXD2	ENCIF06	IRQ14	
R20		PS7		TIOCA4 / TIOCB4 / PO24	TXD2			
T1	DVDD_USB							
T2	VDD33_USB							
T3		P32			USB_OVRCUR		IRQ10	
T5		PC6	DREQ0	TCLKC	SCL1 / CRXD0 / USB_VBUSIN			
T6		P37	WE1#/ DQMLU	PO1				
T7		P36	WE0#/ DQMLL	PO0				
T8		PG3	A4	PO5 / TIC1	MISO1			
T9		PG6	A7	TCLKB / PO8	SSL11			
T10		PH3	A12	MTIOC1B / PO13				
T11	VCCQ33							
T12		PH5	A14	PO15				
T13	VCCQ33							
T14		P26	A19 / DREQ1	MTIOC8D				
T15	VCCQ33							
T16	VSS							
T18	VSS							
T19	TRACEDATA0	PE0	D8	MTIOC1B / TIOCB2				
T20	TRACEDATA1	PE1	D9	MTCLKD / TIOCB3	SSL03			
U1		P60	TEND0		CTXD0 / SPBSSL			
U2		P63			SPBMO/SPBIO0			
U3		PN1		MTIOC8C / PO21	MISO1	ENCIF09		
U18	TRACECTL	P00	D0	MTIOC6A / TIOCA1				ADTRG1
U19		P04	D4	MTIOC3C / TIOCA5				
U20		P03	D3	MTIC5U / TIOCA4				
V1		P61	DACK0		CTXD1 / SPBIO3			
V2		P64			SPBMI/SPBIO1			
V3		PN3		MTIOC8A	RSPCK1			
V4		PN4		MTIOC6C / TIOCC6	SSL11		IRQ12	
V5		PC7		TIC0	SDA1 / CRXD1			
V6		PG1	A2	PO3				
V7		PG4	A5	PO6 / TOC1	MOSI1			
V8		PG5	A6	TCLKA / PO7	SSL10			
V9		PH0	A9	PO10				
V10		PH1	A10	MTIOC2B / PO11				
V11		PH7	A16	MTIC5W				

2.3 DC Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125°C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 2.2 DC Characteristics (1)

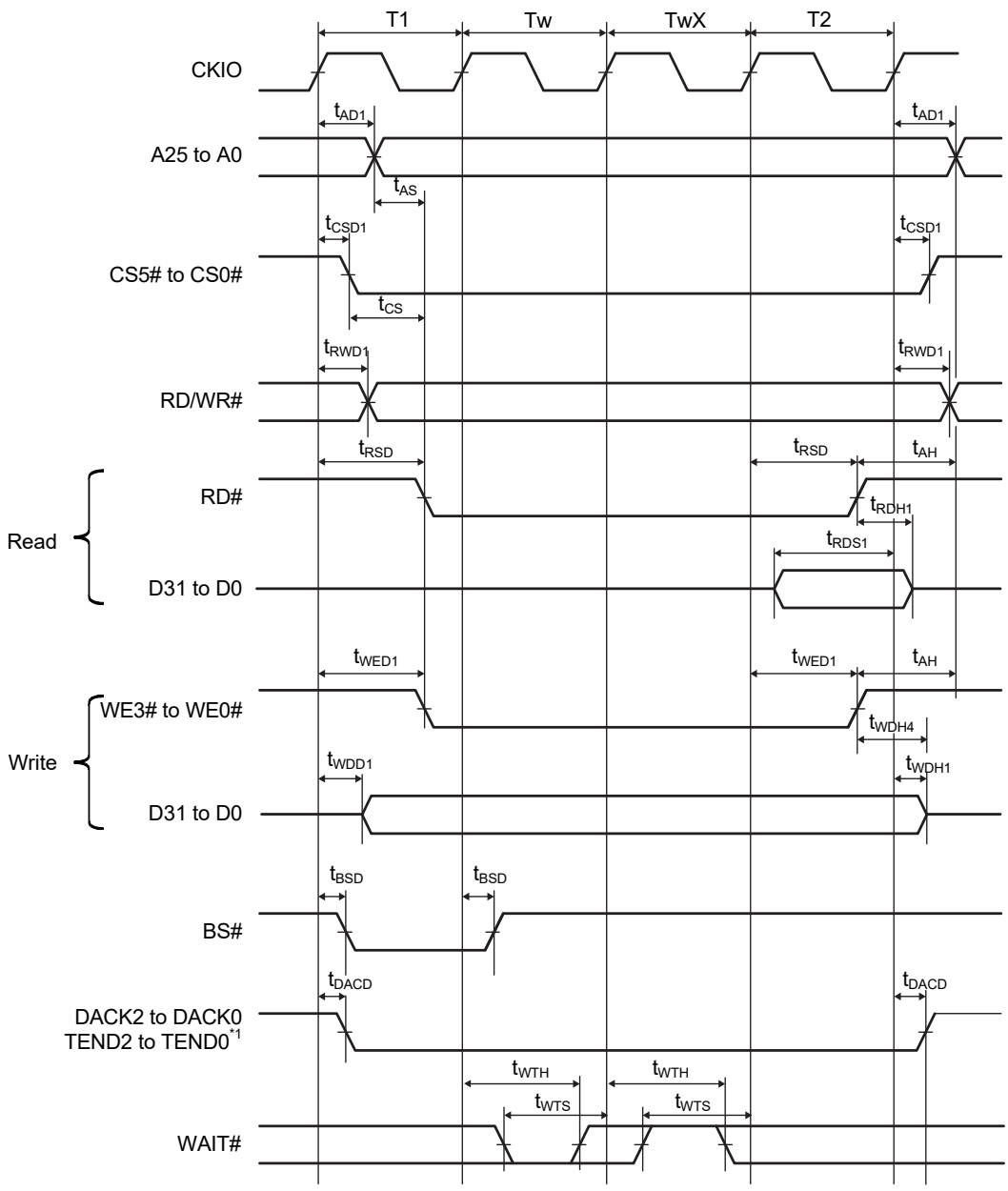
Item	Symbol	min	typ	max	Unit	Test Conditions
Power supply voltage (I/O)	VCCQ33	3.0	3.3	3.6	V	
Power supply voltage (internal)	VDD	1.14	1.2	1.26	V	
PLL power supply voltage	PLLVDD0, PLLVDD1	1.14	1.2	1.26	V	
USB digital power supply voltage	DVDD_USB	1.14	1.2	1.26	V	
Analog power supply voltage	AVCC0, AVCC1	3.0	3.3	3.6	V	
USB power supply voltage	VDD33_USB	3.0	3.3	3.6	V	

2.4.3 Bus Timing

Table 2.17 Bus Timing (1 / 2)

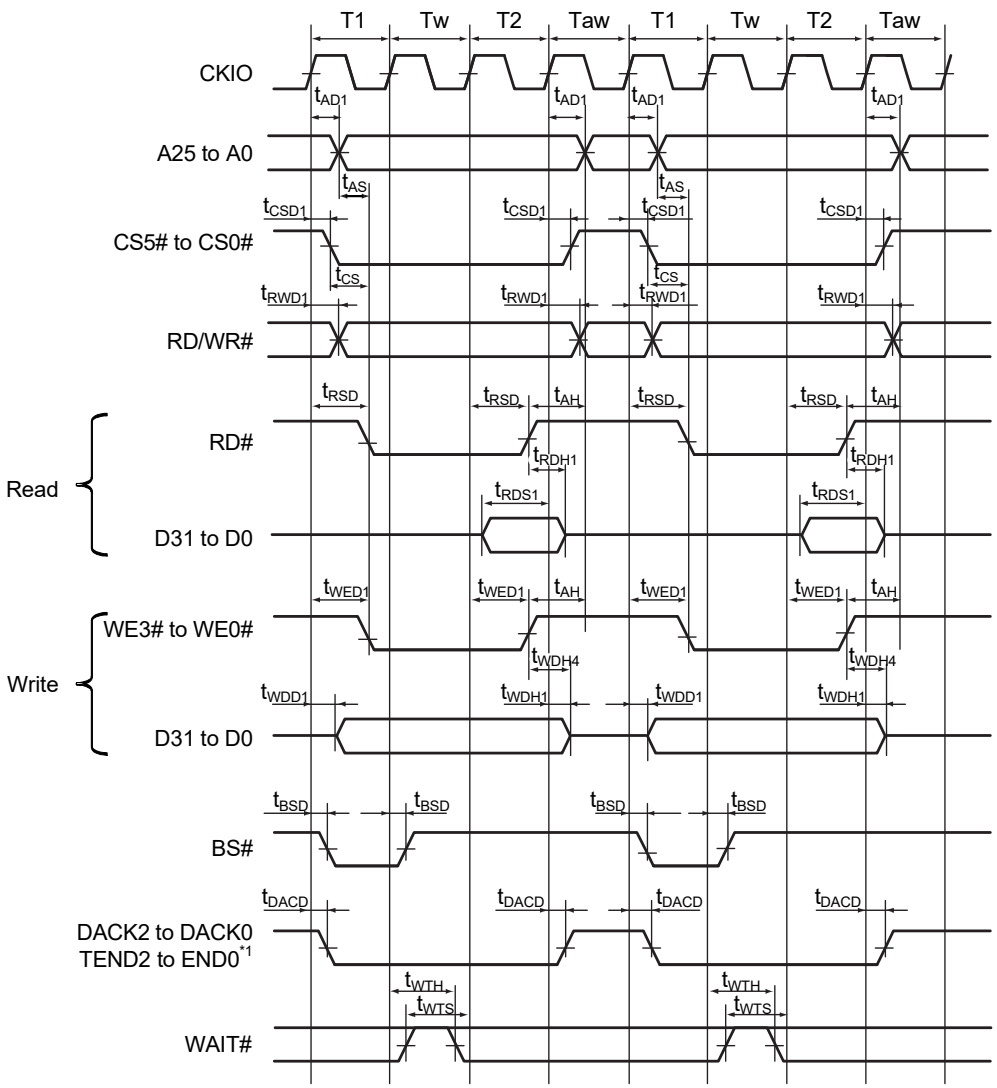
Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	CKIO = $1/t_{CKcyc}$*1 Min.	CKIO = $1/t_{CKcyc}$*1 Max.	Unit	Reference Figure
Address delay time 1	SDRAM*3	t_{AD1}	2	10	ns	Figure 2.12 to Figure 2.36
	Other than the above		0	10	ns	
Address delay time 2		t_{AD2}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.19
Address setup time		t_{AS}	0	—	ns	Figure 2.12 to Figure 2.15, Figure 2.19
Chip enable setup time		t_{cs}	0	—	ns	Figure 2.12 to Figure 2.15, Figure 2.19
Address hold time		t_{AH}	0	—	ns	Figure 2.12 to Figure 2.15
BS# delay time		t_{BSD}	—	10	ns	Figure 2.12 to Figure 2.33
CS# delay time 1	SDRAM*3	t_{CSD1}	2	10	ns	Figure 2.12 to Figure 2.36
	Other than the above		0	10	ns	
Read/write delay time 1	SDRAM*3	t_{RWD1}	2	10	ns	Figure 2.12 to Figure 2.36
	Other than the above		0	10	ns	
Read strobe delay time		t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.12 to Figure 2.19
Read data setup time 1*4	High-drive output	t_{RDS1}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.12 to Figure 2.18
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data setup time 2*4	High-drive output	t_{RDS2}	6.6	—	ns	Figure 2.20 to Figure 2.23, Figure 2.28 to Figure 2.30
	Normal output		10	—	ns	
Read data setup time 3*4	High-drive output	t_{RDS3}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.19
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data hold time 1		t_{RDH1}	0	—	ns	Figure 2.12 to Figure 2.18
Read data hold time 2		t_{RDH2}	2	—	ns	Figure 2.20 to Figure 2.23, Figure 2.28 to Figure 2.30
Read data hold time 3		t_{RDH3}	0	—	ns	Figure 2.19
Write enable delay time 1		t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.12 to Figure 2.17
Write enable delay time 2		t_{WED2}	—	10	ns	Figure 2.18
Write data delay time 1		t_{WDD1}	—	10	ns	Figure 2.12 to Figure 2.18
Write data delay time 2		t_{WDD2}	—	10	ns	Figure 2.24 to Figure 2.27, Figure 2.31 to Figure 2.33
Write data hold time 1		t_{WDH1}	1	—	ns	Figure 2.12 to Figure 2.18



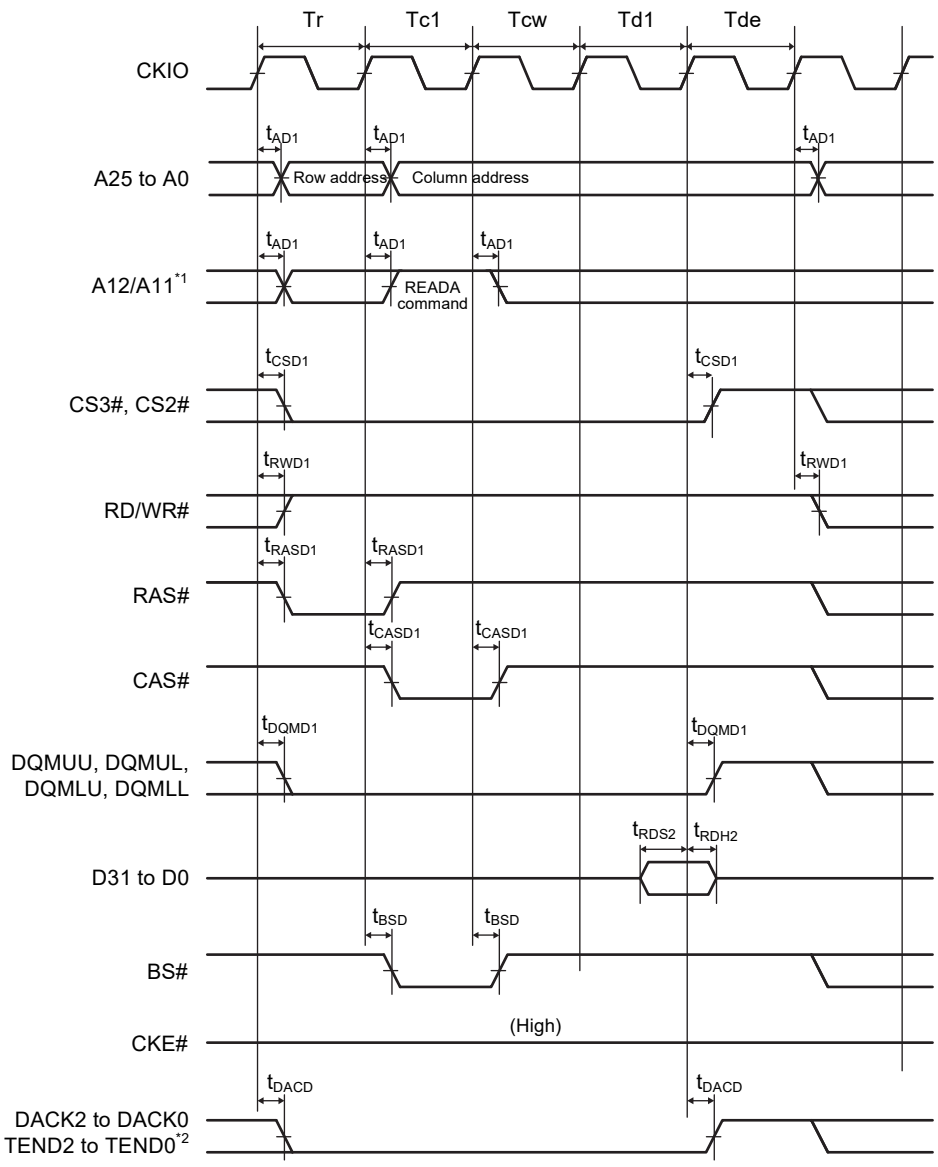
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.14 SRAM Interface Basic Bus Cycle (Software Wait 1, External Wait 1 Inserted)



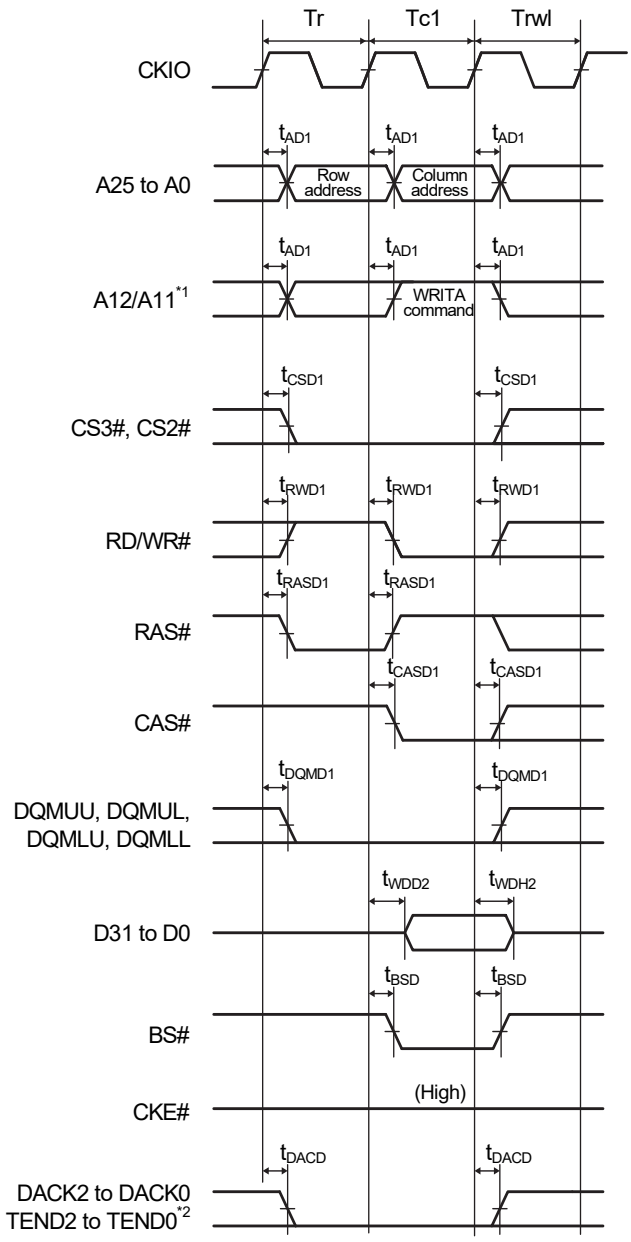
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.15 SRAM Interface Basic Bus Cycle (Software Wait 1, External wait Enabled (WM Bit = 0), No Idle Cycle)



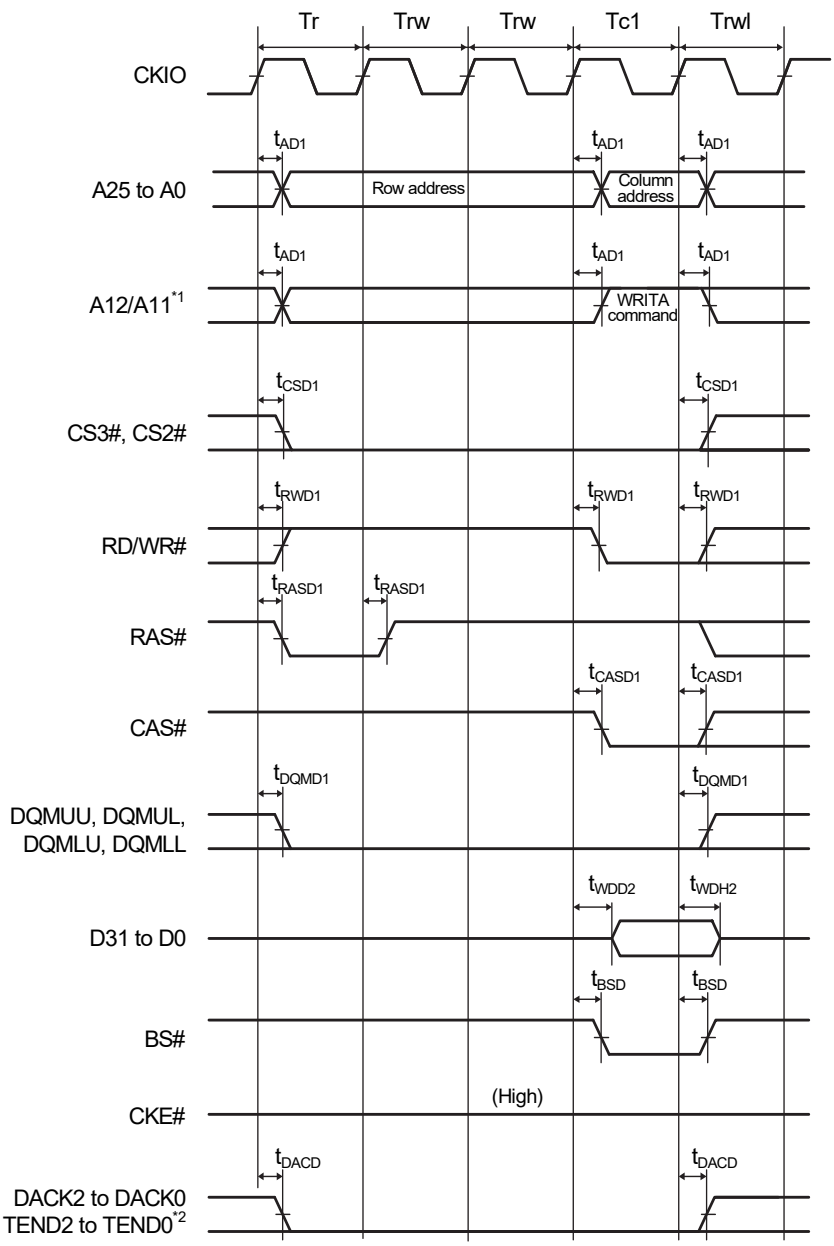
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.20 Synchronous DRAM Single-Read Bus Cycle (with Auto Precharge, CAS Latency 2, WTRCD = 0 Cycles, WTRP = 0 Cycles)



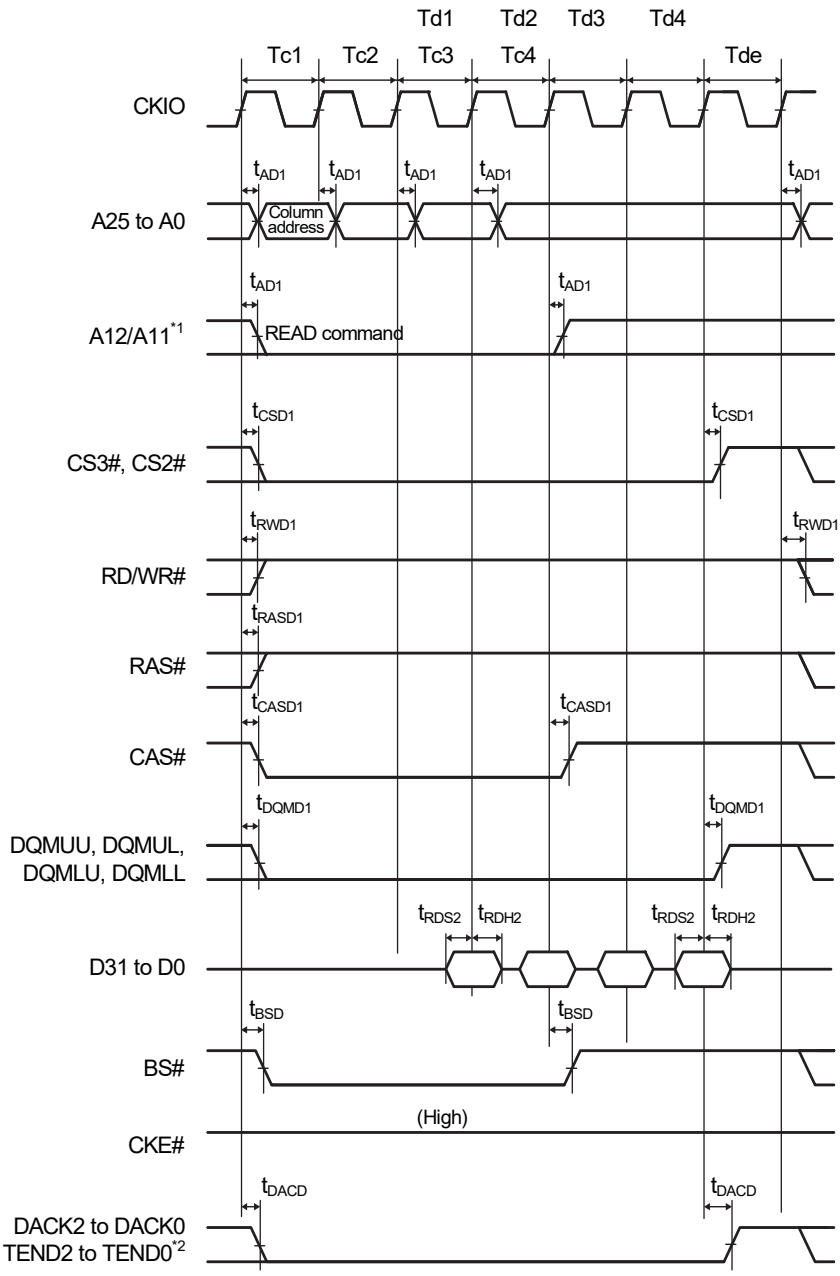
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.24 Synchronous DRAM Single-Write Bus Cycle (with Auto Precharge, TRWL = 1 Cycle)



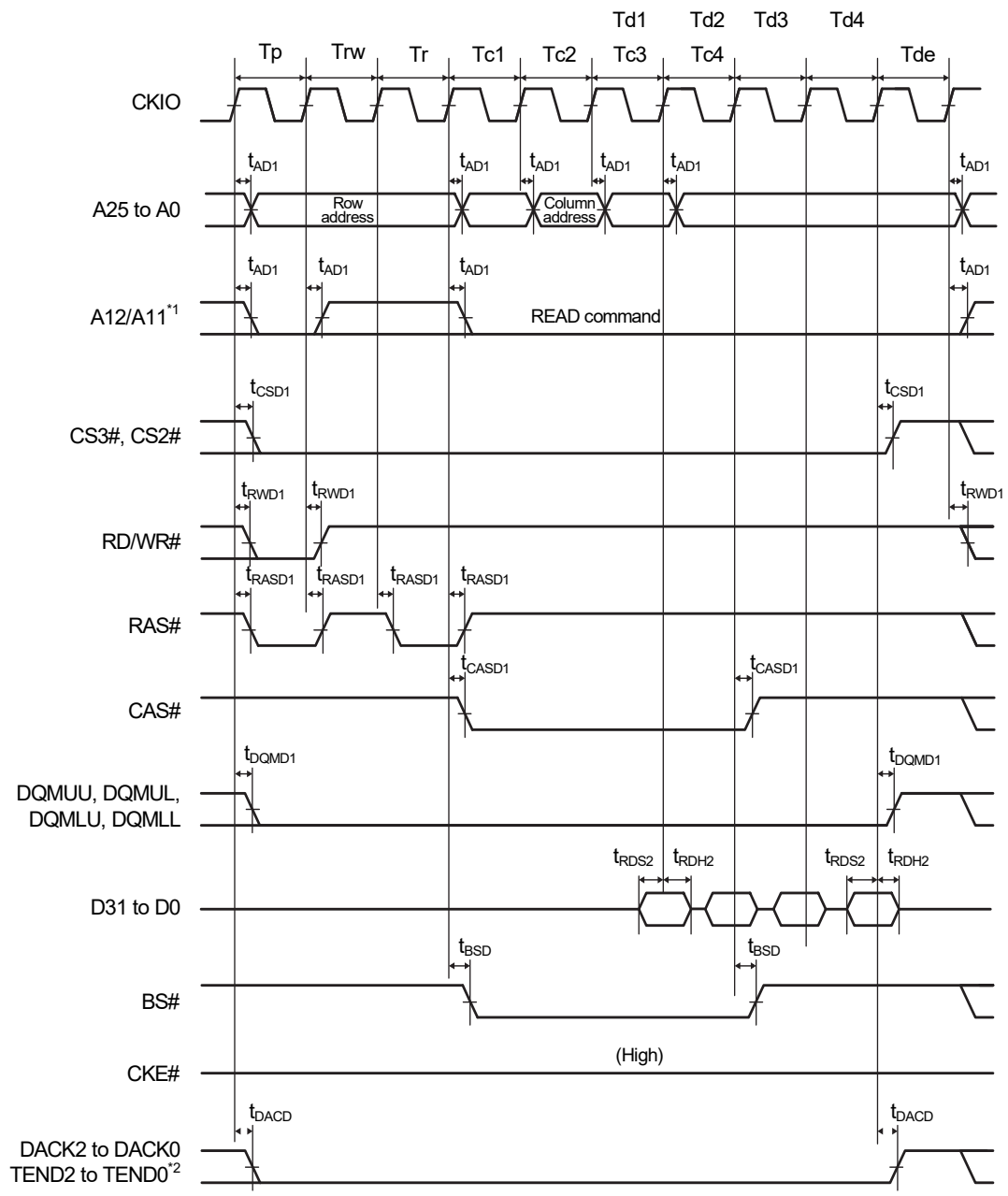
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.25 Synchronous DRAM Single-Write Bus Cycle (with Auto Precharge, WTRCD = 2 Cycles, TRWL = 1 Cycle)



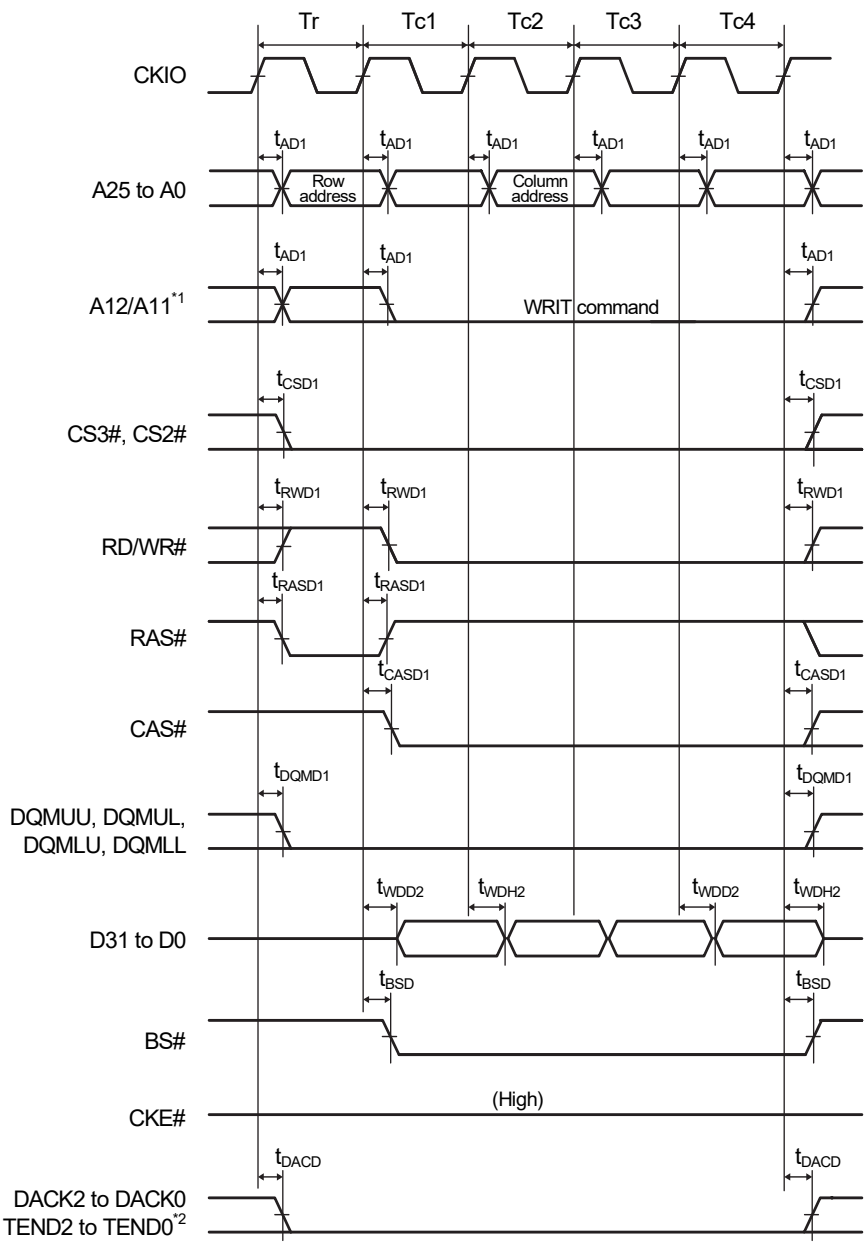
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.29 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: READ Command, Same Row Address, CAS Latency 2, WTRCD = 0 Cycles)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.30 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: PRE + ACT + READ Command, Different Row Address, CAS Latency 2, WTRCD = 0 Cycles)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.31 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (Bank Active Mode: ACT + WRITE Command, WTRCD = 0 Cycles, TRWL = 0 Cycles)

2.4.5.4 MTU3a Timing

Table 2.22 MTU3a Timing

Item			Symbol	min	max	Unit*1	Test Conditions
MTU3a	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PCcyc}	Figure 2.43
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PCcyc}	Figure 2.44
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PCcyc}: PCLKC cycle

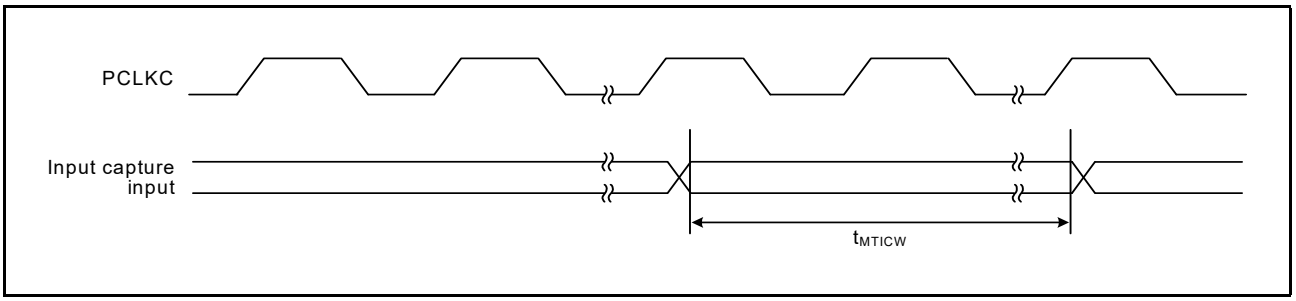


Figure 2.43 MTU3a Input Capture Input Timing

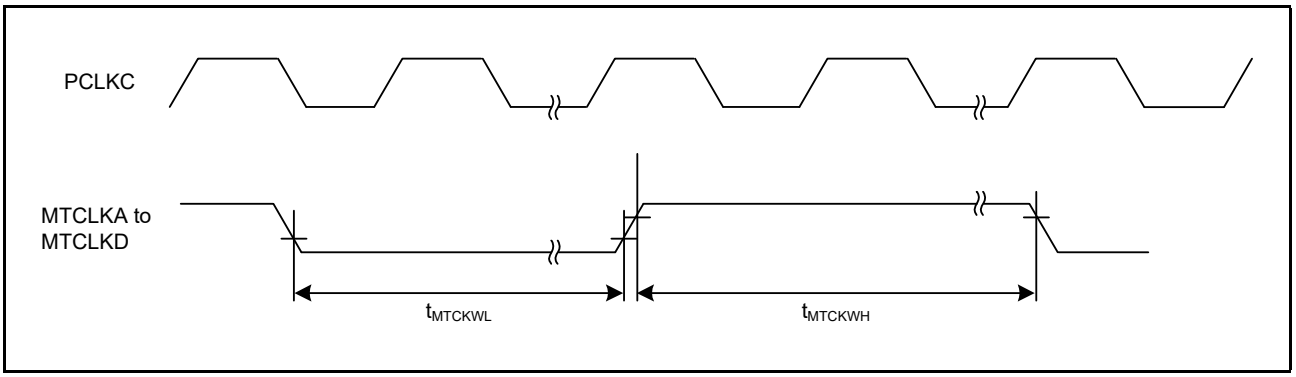


Figure 2.44 MTU3a Clock Input Timing

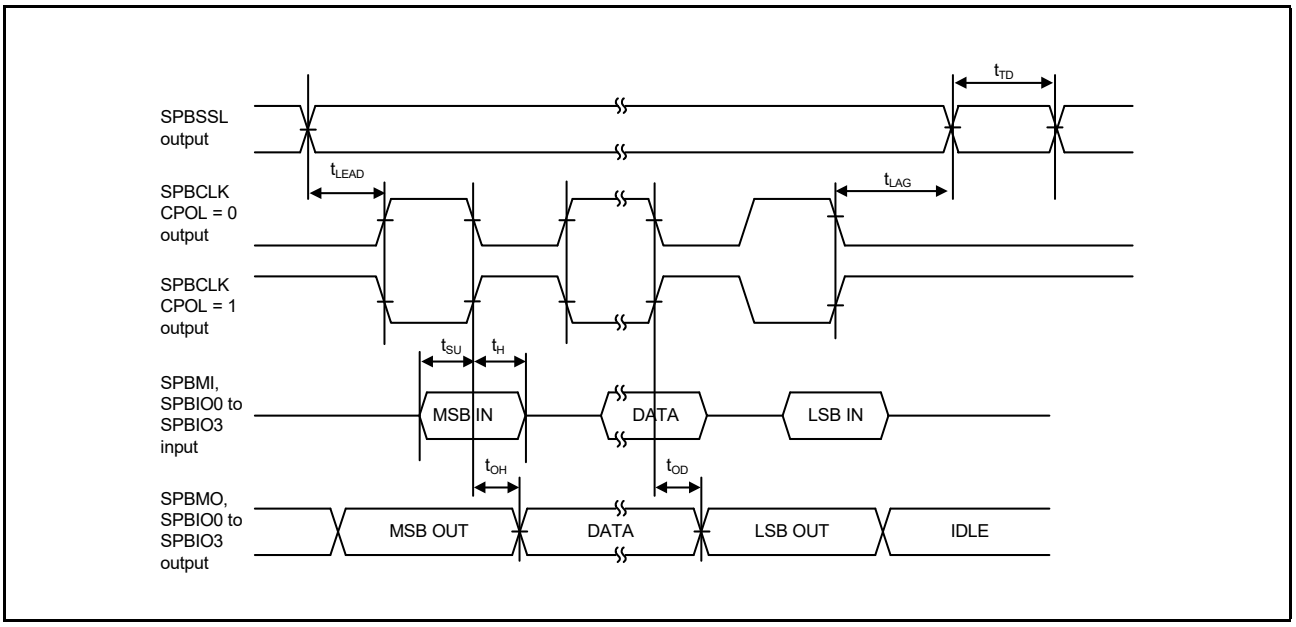


Figure 2.60 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1)

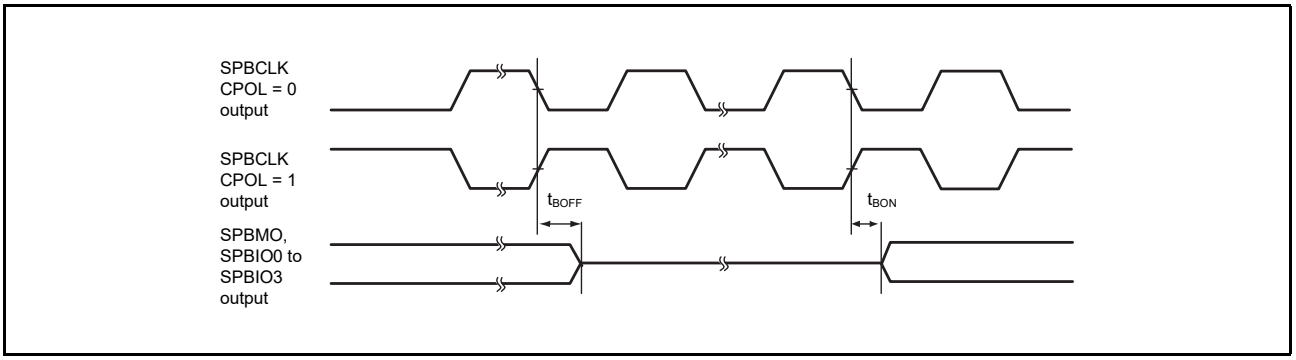


Figure 2.61 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 0)

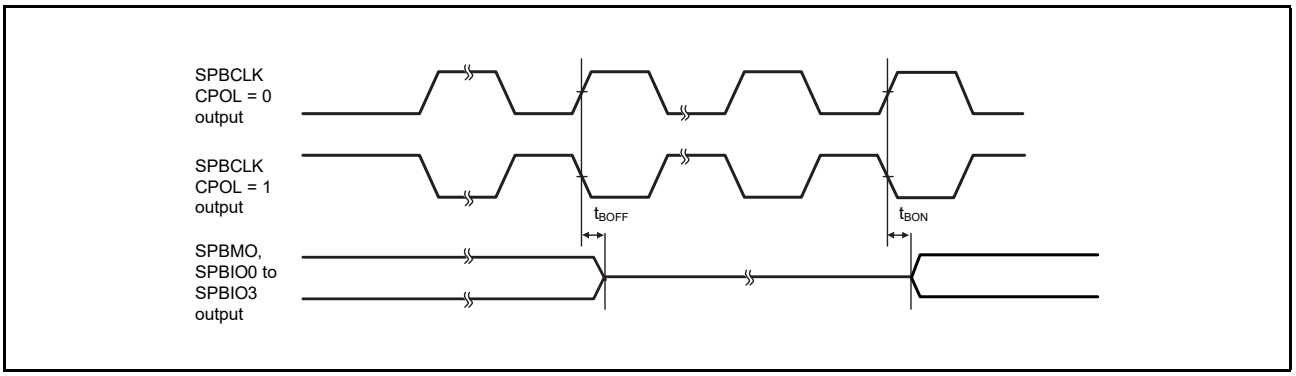


Figure 2.62 SPIBSC Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)

2.4.5.12 Serial Sound Interface Timing

Table 2.30 Serial Sound Interface Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	Min.	Max.	Unit	Test Conditions
SSI	AUDIO_CLK input frequency	t_{AUDIO}	1	50	MHz	
	Output clock cycle	t_O	150	64000	ns	Figure 2.65
	Input clock cycle	t_I	150	64000	ns	
	Clock high level	t_{HC}	60	—	ns	
	Clock low level	t_{LC}	60	—	ns	
	Clock rising time	t_{RC}	—	25	ns	
	Data delay time	t_{DTR}	–5	25	ns	Figure 2.66, Figure 2.67
	Setup time	t_{SR}	25	—	ns	
	Hold time	t_{HTR}	25	—	ns	
	WS change edge SSITXD0 output delay	T_{DTRW}	—	25	ns	Figure 2.68

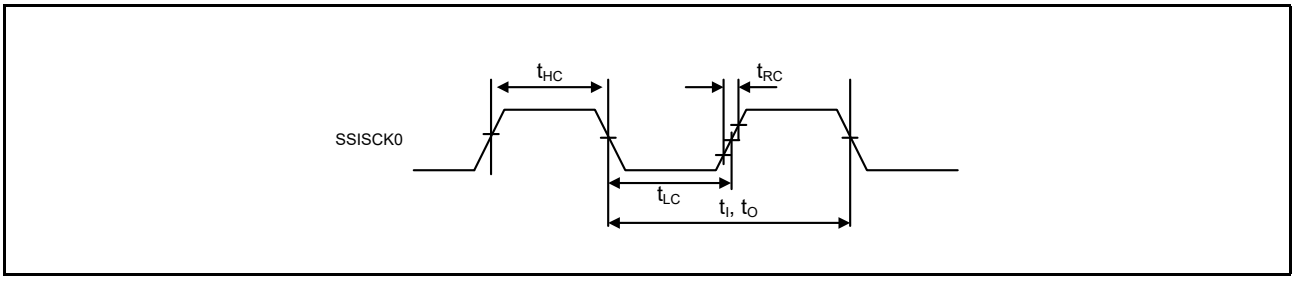


Figure 2.65 Clock Input/Output Timing

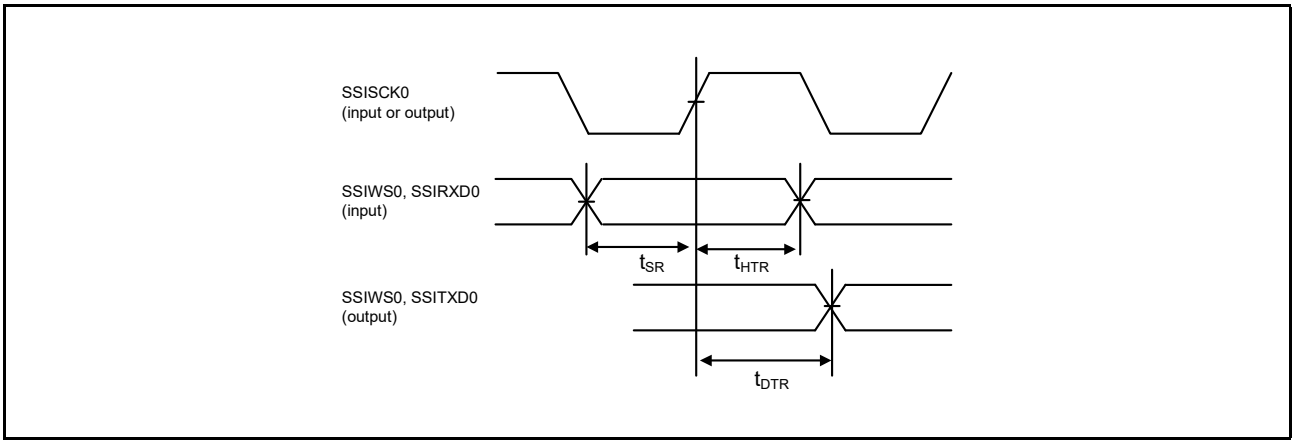


Figure 2.66 Transmit/Receive Timing (SSISCK0 Rising Synchronous)

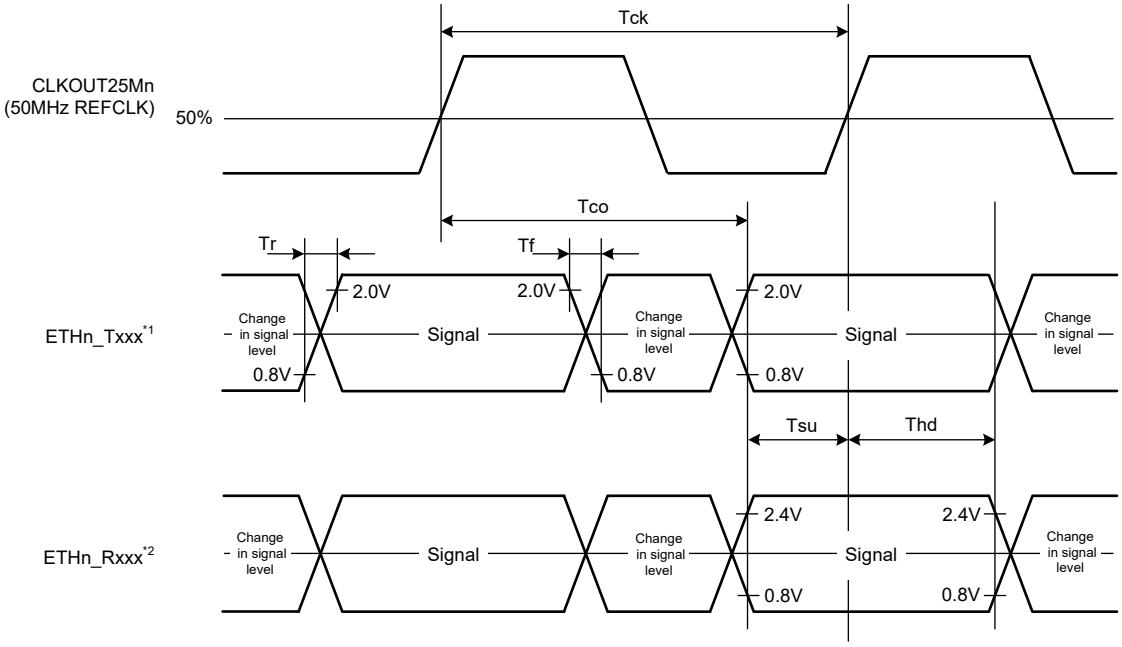
2.4.5.14 ETHERC Timing

Table 2.32 ETHERC Timing

Output load conditions: V_{OH} = 2.0 V, V_{OL1} = 0.8 V, C = 25 pF (RMII)
V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF (MII)

Item		Symbol	min	max	Unit	Test Conditions
ETHERC (RMII)	CLKOUT25Mn cycle time	T_{ck}	20	—	ns	Figure 2.70 to Figure 2.73
	ETHn_Txxx*1 output delay time	Tco	2	16	ns	
	ETHn_Rxxx*2 setup time	T_{su}	4	—	ns	
	ETHn_Rxxx*2 hold time	T_{hd}	2	—	ns	
	ETHn_xxxx*1, *2 rising/falling time	T_r, T_f	0.5	5	ns	
ETHERC (MII)	ETHn_TXC cycle time	t_{Tcyc}	40	—	ns	—
	ETHn_TXEN output delay time	t_{TENd}	0	25	ns	Figure 2.74
	ETHn_TXD0 to ETHn_TXD3 output delay time	t_{MTDd}	0	25	ns	
	ETHn_TXER output delay time	t_{TERd}	—	25	ns	Figure 2.75
	ETHn_RXC cycle time	t_{TRcyc}	40	—	ns	—
	ETHn_RXDV setup time	t_{RDVs}	10	—	ns	Figure 2.76
	ETHn_RXDV hold time	t_{RDVh}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3 setup time	t_{MRDs}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3 hold time	t_{MRDh}	10	—	ns	
	ETHn_RXER setup time	t_{RERs}	10	—	ns	Figure 2.77
	ETHn_RXER hold time	t_{RERh}	10	—	ns	

Note 1. ETHn_TXEN, ETHn_TXD1, ETHn_TXD0
Note 2. ETHn_RXDV, ETHn_RXD1, ETHn_RXD0, ETHn_RXER



Note 1. ETHn_TXEN, ETHn_TXD1, ETHn_TXD0
Note 2. ETHn_RXDV, ETHn_RXD1, ETHn_RXD0, ETHn_RXER

Figure 2.70 Timing with the CLKOUT25Mn and RMII Signals

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(Rev.4.0-1 November 2017)

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