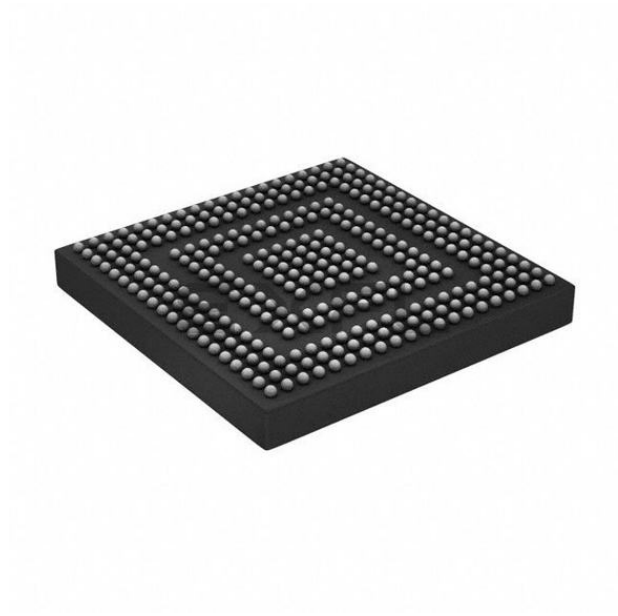
# Renesas Electronics America Inc - R7S910006CBG#AC0 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-R4F |
| Core Size | 32-Bit Single-Core |
| Speed | 450MHz |
| Connectivity | CANbus, CSI, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 209 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 1.5M x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.14V ~ 3.6V |
| Data Converters | A/D 24x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 320-FBGA |
| Supplier Device Package | 320-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910006cbg-ac0 |

**Table 1.1 Outline of Specifications (2 / 7)**

| Classification | Module/Function | Description |
|---|---|---|
| Low power | Low power consumption | • Standby mode (Cortex-R4)<br>• Sleep mode (Cortex-M3) (for products incorporating an R-IN engine)<br>• Module stop function |
| Interrupt | Cortex-R4 vector interrupt controller (VIC) | • Peripheral function interrupts: 273 sources / 276 sources (for products incorporating an R-IN engine)<br>• External interrupts: 20 sources (NMI, IRQ0 to IRQ15, ETH0_INT, ETH1_INT, and ETH2_INT pins)<br>• Software interrupts: 1 source<br>• Non-maskable interrupts: 2 sources<br>• Sixteen levels specifiable for the order of priority |
| | Cortex-M3 nested-type vector interrupt controller (NVIC) (only included in products incorporating an R-IN engine) | • Peripheral function interrupts: 82 sources<br>• External interrupts: 19 sources (IRQ0 to IRQ15, ETH0_INT, ETH1_INT, and ETH2_INT pins)<br>• Software interrupts: 1 source<br>• Non-maskable interrupts: 1 source<br>• Sixteen levels specifiable for the order of priority |
| External bus extension | Bus state controller (BSC) | • The external address space is divided into six areas (CS0 to CS5) for management.<br>• The following features settable for each area independently.<br>Bus size (8, 16, or 32 bits): Available sizes depend on the area.<br>Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas)<br>Idle wait cycle insertion (between same area access cycles or different area access cycles)<br>Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available.<br>• Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing can be selected by software)<br>• SDRAM refresh<br>Auto refresh or self-refresh mode selectable<br>• SDRAM burst access |
| Data transfer | Direct memory access controller (DMAC) | • 2 units (16 channels for unit 0, 16 channels for unit 1)<br>• Transfer modes: Single transfer mode and block transfer mode<br>• Transfer size<br>Unit 0: 1/2/4/16/32/64 bytes<br>Unit 1: 1/2/4/16 bytes<br>• Activation sources: Software trigger, external DMA requests (DREQ0 to DREQ2), external interrupts, and interrupt requests from peripheral functions |
| I/O ports | General-purpose I/O ports | • 320-pin FBGA<br>I/O pins: 209<br>Input pins: 9<br>Pull-up/pull-down resistors: 209<br>5-V tolerance: 9<br>• 176-pin HLQFP<br>I/O pins: 97<br>Input pins: 5<br>Pull-up/pull-down resistors: 97<br>5-V tolerance: 5 |
| Event link controller (ELC) | | • 87 event signals can be interlinked with the operation of modules.<br>• In particular, the operation of timer modules can be started by input event signals.<br>• Event-linked operation of signals of ports B and E is to be possible. |
| Multi-function pin controller (MPC) | | The locations of input/output functions are selectable from among multiple pins. |

**Table 1.5 Pin Assignments (320-Pin FBGA) (7 / 8)**

| Pin Number | Pin Name |
|---|---|
| V10 | PH1 / A10 / MTIOC2B / PO11 |
| V11 | PH7 / A16 / MTIC5W |
| V12 | P20 / A17 / MTCLKD |
| V13 | P21 / IRQ1 / CS0# / MTIC5V / TIOCB1 / CTS0# |
| V14 | VSS |
| V15 | P45 / CS2# |
| V16 | P46 / CKE |
| V17 | PS2 / MTIOC7C / SSIWS0 |
| V18 | P05 / D5 / MTIOC3A |
| V19 | P01 / D1 / MTIC5W / TIOCA2 |
| V20 | P02 / D2 / MTIC5V / TIOCA3 |
| W1 | P62 / SPBCLK |
| W2 | P65 / SPBIO2 / DREQ0 |
| W3 | PN5 / IRQ5 / MTIOC6A / TIOCD9 / ENCIF10 |
| W4 | PN6 / MTIOC3C / TIOCC9 / MCLK3 / ENCIF11 |
| W5 | PP0 / POE8# / TEND0 / MCLK2 |
| W6 | PP2 / MTIOC0C / TCLKH / MCLK1 |
| W7 | PP4 / MTIOC0A / MCLK0 |
| W8 | PP6 / TIOCA11 / RXD1 / TRACECTL / ENCIF06 |
| W9 | PP7 / TCLKF / TCLKH / SCK1 / DACK1 / TRACECLK |
| W10 | PR1 / IRQ9 / POE4# / CTS1# / TEND1 / TRACEDATA1 / ENCIF08 |
| W11 | PR3 / TIOCA10 / TIOCB10 / TRACEDATA3 / ENCIF01 |
| W12 | PR5 / TIOCA8 / TIOCB8 / TRACEDATA5 / ENCIF03 |
| W13 | P24 / IRQ12 / RD/WR# / RXD0 |
| W14 | P22 / IRQ2 / RD# / MTIOC7B / TIOCD0 / SCK0 |
| W15 | P44 / IRQ12 / WAIT# / TCLKD / ADTRG0 / CTS0# |
| W16 | P43 / WE2#/DQMUL / MTIOC8B / USB_VBUSEN |
| W17 | PS1 / IRQ1 / MTIOC7B / SSISCK0 |
| W18 | PS3 / MTIOC7A / SSIRXD0 |
| W19 | PS4 / MTIOC6D / SSITXD0 |
| W20 | PS5 / MTIOC6B |
| Y1 | VSS |
| Y2 | P67 / IRQ15 / GTIOC3B / CTXD0 / TEND0 / USB_OVRCUR |
| Y3 | P66 / IRQ14 / GTIOC3A / CTXD1 / DACK0 / USB_VBUSEN |
| Y4 | PN7 / MTIOC3A / TIOCD6 / DREQ0 / MDAT3 / ENCIF12 |
| Y5 | PP1 / MTIOC0D / DACK0 / MDAT2 |
| Y6 | PP3 / MTIOC0B / TCLKC / MDAT1 |
| Y7 | PP5 / PO22 / MDAT0 |
| Y8 | VSS |
| Y9 | PR0 / TCLKE / TCLKG / TXD1 / DREQ1 / TRACEDATA0 / ENCIF07 |
| Y10 | PR2 / TIOCA11 / TIOCB11 / RTS1# / TRACEDATA2 / ENCIF00 |
| Y11 | PR4 / TIOCA9 / TIOCB9 / TRACEDATA4 / ENCIF02 |
| Y12 | PR6 / TIOCA7 / TIOCB7 / TRACEDATA6 / ENCIF04 |
| Y13 | PR7 / TIOCA6 / TIOCB6 / TRACEDATA7 / ENCIF05 |
| Y14 | P25 / A18 / MTCLKC / TEND1 |

**Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10)**

| Pin Number 320-Pin FBGA | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW) | Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB) | Others (SSI, DSMIF, Encoder I/F) | Interrupt | S12ADCa |
|---|---|---|---|---|---|---|---|---|
| C15 | | | | | | | | AN000 |
| C16 | VREFL0 | | | | | | | |
| C17 | VREFH0 | | | | | | | |
| C18 | | PD2 | WAIT# | | | | | AN110 |
| C19 | | P14 | CAS# | MTIOC4A / GTIOC1A | | ENCIF10 | | |
| C20 | | P13 | RAS# | MTIOC4C / GTIOC1B | | | | |
| D1 | | P81 | | TIOCC0 | ETH0_RXER / CTS4# | | | |
| D2 | | P80 | | TIOCC3 | ETH0_RXDV / RTS4# | | IRQ8 | |
| D3 | | PU3 | | TIOCD6 | ETH2_COL / TXD3 | | | |
| D18 | | PD0 | CS4# | | | | | AN108 |
| D19 | | P96 | | POE0# / POE10# | | ENCIF09 | | AN106 |
| D20 | | P95 | | MTCLKA | CTS2# | | IRQ13 | AN105 |
| E1 | | P84 | | | ETH0_COL / CATLINKACT1 / RXD4 | | | |
| E2 | | P82 | | TIOCD3 | ETH0_TXEN / ETH1_CRS / SCK4 / RTS3# / USB_OVRCUR | | | |
| E3 | | PU1 | | TIOCA11 | ETH2_RXC / SCK3 | | | |
| E5 | | PU0 | | TIOCA10 | ETH2_RXER | | | |
| E6 | | PL6 | | TIOCA9 | ETH2_RXD3 | | | |
| E7 | | PL4 | | | ETH2_RXD1 | | IRQ4 | |
| E8 | | PL2 | | TIOCA6 | ETH2_TXEN | | | ADTRG1 |
| E9 | | PL0 | | TIOCB9 | ETH2_TXD0 | | | |
| E10 | | PK7 | | TIOCB7 | ETH2_TXD2 | | | |
| E11 | | PK6 | | TIOCB6 | ETH2_TXD3 | | | |
| E12 | | PD5 | A21 | TIC0 | ETH1_TXD3 / ETH0_TXD0 / SSL20 | MCLK3 | | AN113 |
| E13 | | P56 | BS# | | ETH1_TXER | | | |
| E14 | | PD4 | | | ETH2_INT | | | AN112 |
| E15 | VCCQ33 | | | | | | | |
| E16 | | PD1 | CS1# | | | | | AN109 |
| E18 | | P97 | A25 | | | | IRQ7 | ADTRG1 / AN107 |
| E19 | | P94 | | MTCLKB | RTS2# | ENCIF08 | IRQ4 | AN104 |
| E20 | | P93 | | MTIOC1A / TIC3 | SCK2 | ENCIF07 | | AN103 |
| F1 | | PC4 | | TCLKH | CATI2CCLK / SCL0 | | | |
| F2 | | P83 | | | ETH0_CRS / CATLINKACT0 / TXD4 | | IRQ11 | |

**Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (6 / 10)**

| Pin Number 320-Pin FBGA | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW) | Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB) | Others (SSI, DSMIF, Encoder I/F) | Interrupt | S12ADCa |
|---|---|---|---|---|---|---|---|---|
| K18 | TRACEDATA4 | P76 | D22 | MTIOC4B / GTIOC2A | SSL01 | SSIWS0 | | |
| K19 | TRACEDATA3 | P75 | D21 | MTIOC4D / GTIOC2B | SSL00 | ENCIF04 | IRQ13 | |
| K20 | | PT5 | BS# / TEND2 | PO30 | | | | |
| L1 | MD1 | | | | | | | |
| L2 | MD2 | | | | | | | |
| L3 | TMS | | | | | | | |
| L5 | TCK | | | | | | | |
| L6 | PLLVSS1 | | | | | | | |
| L8 | VDD | | | | | | | |
| L9 | VSS | | | | | | | |
| L10 | VSS | | | | | | | |
| L11 | VSS | | | | | | | |
| L12 | VSS | | | | | | | |
| L13 | VDD | | | | | | | |
| L15 | VSS | | | | | | | |
| L16 | TRACEDATA7 | PE7 | D15 | MTIOC7A / TIOCD3 / POE8# | SCK1 / RSPCK0 | | | |
| L18 | TRACEDATA0 | P72 | D18 | MTIOC1A / TIC2 | TXD1 | SSITXD0 / ENCIF02 | | |
| L19 | TRACEDATA1 | P73 | D19 | MTCLKB | RXD1 | SSIRXD0 / ENCIF03 | IRQ3 | |
| L20 | TRACEDATA2 | P74 | D20 | MTCLKA | CTS1# / SSL03 | SSISCK0 | | |
| M1 | XTAL | | | | | | | |
| M2 | EXTAL | | | | | | | |
| M3 | OSCTH | | | | | | | |
| M5 | BSCANP | | | | | | | |
| M6 | PLLVDD0 | | | | | | | |
| M8 | VDD | | | | | | | |
| M9 | VSS | | | | | | | |
| M10 | VSS | | | | | | | |
| M11 | VSS | | | | | | | |
| M12 | VSS | | | | | | | |
| M13 | VDD | | | | | | | |
| M15 | VCCQ33 | | | | | | | |
| M16 | TRACEDATA6 | PE6 | D14 | MTIOC0A / TIOCD0 | RXD1 / MISO0 | | IRQ6 | |
| M18 | TRACECLK | P70 | D16 | MTIOC6D | RTS1# / USB_OVRCUR | ENCIF00 | IRQ0 | |
| M19 | | PT4 | CS3# | PO29 | | | | |
| M20 | TRACECTL | P71 | D17 | POE0# / POE10# / TOC2 | SCK1 | ENCIF01 | | |
| N1 | VSS | | | | | | | |
| N2 | MD0 | | | | | | | |

**Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP) (1 / 6)**

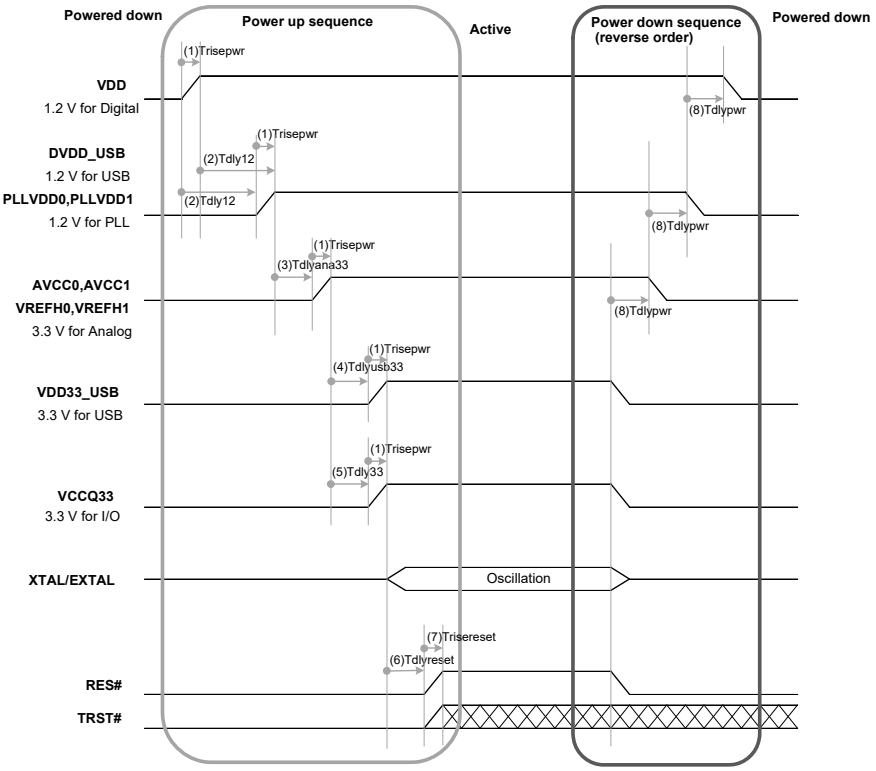
| Pin Number 176-Pin HLQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW) | Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB) | Others (SSI, DSMIF) | Interrupt | S12ADCa |
|---|---|---|---|---|---|---|---|---|
| 1 | | PC3 | | | ETH0_RXC / ETH0_RXDV / RXD4 / SCL0 / CRXD1 | | | |
| 2 | VCCQ33 | | | | | | | |
| 3 | VSS | | | | | | | |
| 4 | VDD | | | | | | | |
| 5 | | P82 | | TIOCD3 | ETH0_TXEN / ETH1_CRS / SCK4 / RTS3# / USB_OVRCUR | | | |
| 6 | | P85 | | | CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN | | IRQ5 | |
| 7 | ERROROUT# | | | | | | | |
| 8 | | P35 | | | | | NMI | |
| 9 | TRST# | | | | | | | |
| 10 | TDO | P33 | | | | | | |
| 11 | TDI | P34 | | | | | | |
| 12 | TMS | | | | | | | |
| 13 | TCK | | | | | | | |
| 14 | BSCANP | | | | | | | |
| 15 | VDD | | | | | | | |
| 16 | VSS | | | | | | | |
| 17 | MD2 | | | | | | | |
| 18 | MD1 | | | | | | | |
| 19 | PLLVDD1 | | | | | | | |
| 20 | PLLVSS1 | | | | | | | |
| 21 | OSCTH | | | | | | | |
| 22 | VCCQ33 | | | | | | | |
| 23 | EXTAL | | | | | | | |
| 24 | XTAL | | | | | | | |
| 25 | VSS | | | | | | | |
| 26 | MD0 | | | | | | | |
| 27 | PLLVDD0 | | | | | | | |
| 28 | PLLVSS0 | | | | | | | |
| 29 | RES# | | | | | | | |
| 30 | RSTOUT# | | | | | | | |
| 31 | VDD | | | | | | | |
| 32 | VSS | | | | | | | |
| 33 | VDD33_USB | | | | | | | |
| 34 | VSS_USB | | | | | | | |
| 35 | USB_RREF | | | | | | | |

**Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP) (4 / 6)**

| Pin Number 176-Pin HLQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW) | Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB) | Others (SSI, DSMIF) | Interrupt | S12ADCa |
|---|---|---|---|---|---|---|---|---|
| 106 | TRACEDATA 7 | PE7 | D15 | MTIOC7A / TIOCD3 / POE8# | SCK1 / RSPCK0 | | | |
| 107 | VSS | | | | | | | |
| 108 | VDD | | | | | | | |
| 109 | TRACECLK | P70 | D16 | MTIOC6D | RTS1# / USB_OVRCUR | | IRQ0 | |
| 110 | TRACECTL | P71 | D17 | POE0# / POE10# / TOC2 | SCK1 | | | |
| 111 | TRACEDATA 0 | P72 | D18 | MTIOC1A / TIC2 | TXD1 | SSITXD0 | | |
| 112 | TRACEDATA 1 | P73 | D19 | MTCLKB | RXD1 | SSIRXD0 | IRQ3 | |
| 113 | TRACEDATA 2 | P74 | D20 | MTCLKA | CTS1# / SSL03 | SSISCK0 | | |
| 114 | TRACEDATA 3 | P75 | D21 | MTIOC4D / GTIOC2B | SSL00 | | IRQ13 | |
| 115 | TRACEDATA 4 | P76 | D22 | MTIOC4B / GTIOC2A | SSL01 | SSIWS0 | | |
| 116 | TRACEDATA 5 | P77 | D23 | MTIOC4C / GTIOC1B | RSPCK0 | | | |
| 117 | TRACEDATA 6 | PA0 | D24 | MTIOC4A / GTIOC1A | MOSI0 | MDAT3 | | |
| 118 | TRACEDATA 7 | PA1 | D25 | MTIOC3D / GTIOC0B | MISO0 | AUDIO_CLK / MCLK3 | | |
| 119 | VSS | | | | | | | |
| 120 | VDD | | | | | | | |
| 121 | | PA2 | D26 / DREQ2 | MTIOC3B / GTIOC0A | SSL02 | MDAT2 | | |
| 122 | | PA3 | D27 / DACK2 | GTETRG / TIOCA2 | ETHSWSECOUT / SCK2 | MCLK2 | | |
| 123 | | PA4 | D28 / TEND2 | TIOCA3 | ETH1_INT / RXD2 | MDAT1 | | ADTRG0 |
| 124 | | PA5 | D29 | TIOCA4 | ETH0_INT / ETH1_TXER / TXD2 | MCLK1 | | |
| 125 | | PA6 | D30 / A21 | GTIOC3A | CTS2# | MDAT0 | IRQ6 | |
| 126 | VCCQ33 | | | | | | | |
| 127 | | PA7 | D31 / A22 | MTIOC6B / GTIOC3B | RTS2# | MCLK0 | IRQ7 | |
| 128 | VDD | | | | | | | |
| 129 | VSS | | | | | | | |
| 130 | | P13 | RAS# | MTIOC4C / GTIOC1B | | | | |
| 131 | | P14 | CAS# | MTIOC4A / GTIOC1A | | | | |
| 132 | | P15 | CS3# / CKE | MTIOC3D / GTIOC0B | | | | |
| 133 | | P16 | CS4# / CS2# | MTIOC3B / GTIOC0A | | | | |

## 2.2 Power On/Off Sequence

Turn on and off each power supply voltage according to the procedure shown in the figure below.
When turning on the power, be sure to fix TRST# pins and RES# pins to the low level. Otherwise, initialization is not performed successfully.




Timing

| | | Value | | |
|---|---|---|---|---|
| No. | Item | min | typ | max |
| (1) | Trisepwr | 100 µs | — | 50 ms |
| (2) | Tdly12 | 0 ms | — | 100 ms |
| (3) | Tdlyana33 | 0 ms | | 100 ms |
| (4) | Tdlyusb33 | 0 ms | | 100 ms |
| (5) | Tdly33 | 0 ms | | 100 ms |
| (6) | Tdlyreset | 10 ms | — | — |
| (7) | Trisereset | — | — | 150 µs |
| (8) | Tdlypwr | 0 ms | — | — |

Note 1. Turn on all power supply voltages and reset signals with a monotonic increase and turn off with a monotonic decrease.
Note 2. Do not apply a negative voltage to power supply voltages.
Note 3. Before turning on the power, be sure to make reset pins (TRST# and RES#) active (low). Otherwise, inputs and outputs on the pins may be unstable. If this may also be a problem when turning off the power, make reset pins (TRST# and RES#) active (low.)

Note: If the power on/off sequence is not met (out of operation guarantee range), the pin input state and output state may be undefined.

**Figure 2.1 Power On/Off Sequence**

**Table 2.9 Permissible Output Currents**

| Item | | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (average value per pin) | Other than 5-V tolerant pins | $I_{OL1}$ | — | — | 2.0 | mA |
| | 5-V tolerant pins | $I_{OL2}$ | — | — | 3.0 | mA |
| Permissible output low current (maximum value per pin) | Other than 5-V tolerant pins | $I_{OL1}$ | — | — | 4.0 | mA |
| | 5-V tolerant pins | $I_{OL2}$ | — | — | 6.0 | mA |
| Permissible output low current (total) | Total of all output pins | $\Sigma I_{OL}$ | — | — | 80 | mA |
| Permissible output high current (average value per pin) | All output pins | $I_{OH}$ | — | — | –2.0 | mA |
| Permissible output high current (maximum value per pin) | All output pins | $I_{OH}$ | — | — | –4.0 | mA |
| Permissible output high current (total) | Total of all output pins | $\Sigma I_{OH}$ | — | — | –80 | mA |

[Usage Notes] All output current values shall be within the values in Table 2.9 to ensure the reliability of this LSI.

## 2.4.1 Clock Timing

**Table 2.11 CKIO Pin Output Timing**

Output load condition: C = 30 pF

| Item | Symbol | min | typ | max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| CKIO pin output cycle time | $t_{CKcyc}$ | 13.3 | — | 53.4 | ns | Figure 2.2 |
| CKIO pin output high level pulse width | $t_{CKH}$ | $t_{CKcyc}/2 - t_{CKr}$ | — | — | ns | |
| CKIO pin output low level pulse width | $t_{CKL}$ | $t_{CKcyc}/2 - t_{CKf}$ | — | — | ns | |
| CKIO pin output rising time 1 | $t_{CKr}$ | — | — | 5 | ns | CKIO: High drive output setting*1<br>$V_{OH}$ = VCCQ33 – 0.5 V<br>$V_{OL1}$ = 0.4 V |
| CKIO pin output falling time 1 | $t_{CKf}$ | — | — | 5 | ns | |
| CKIO pin output rising time 2 | $t_{CKr}$ | — | — | 9 | ns | CKIO: Normal output setting<br>$V_{OH}$ = VCCQ33 – 0.5 V<br>$V_{OL1}$ = 0.4 V |
| CKIO pin output falling time 2 | $t_{CKf}$ | — | — | 9 | ns | |
| CKIO pin output rising time 3 | $t_{CKr}$ | — | — | 2.5 | ns | CKIO: High drive output setting*1<br>$V_{OH}$ = 2.0 V<br>$V_{OL1}$ = 0.8 V |
| CKIO pin output falling time 3 | $t_{CKf}$ | — | — | 2.5 | ns | |
| CKIO pin output rising time 4 | $t_{CKr}$ | — | — | 4.5 | ns | CKIO: Normal output setting<br>$V_{OH}$ = 2.0 V<br>$V_{OL1}$ = 0.8 V |
| CKIO pin output falling time 4 | $t_{CKf}$ | — | — | 4.5 | ns | |

Note 1. When connecting SDRAM, be sure to set the B0 bit in the drive capacity control register (DSCR) to 1 to be a high drive output.

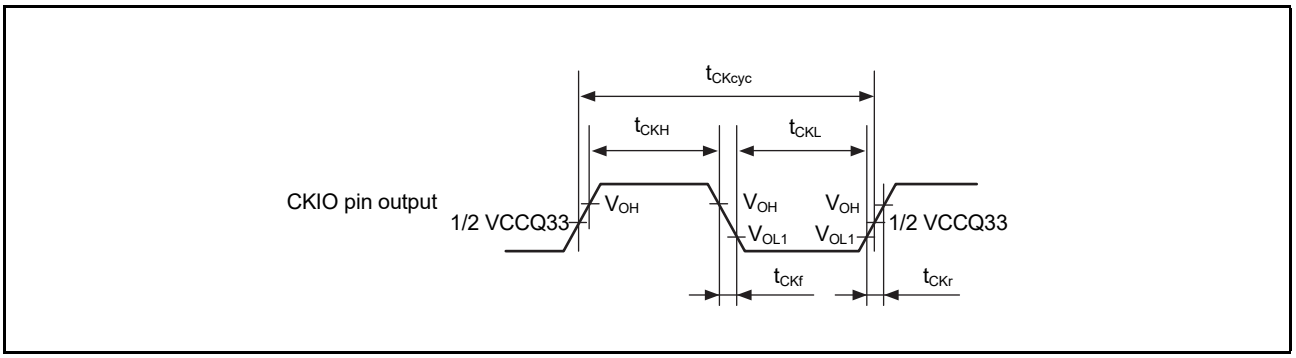



**Figure 2.2 CKIO Pin Output Timing**

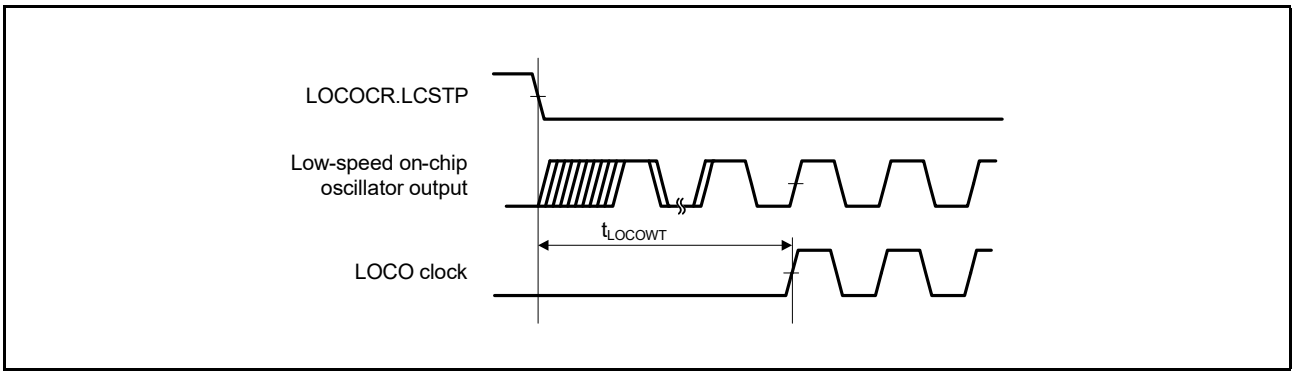
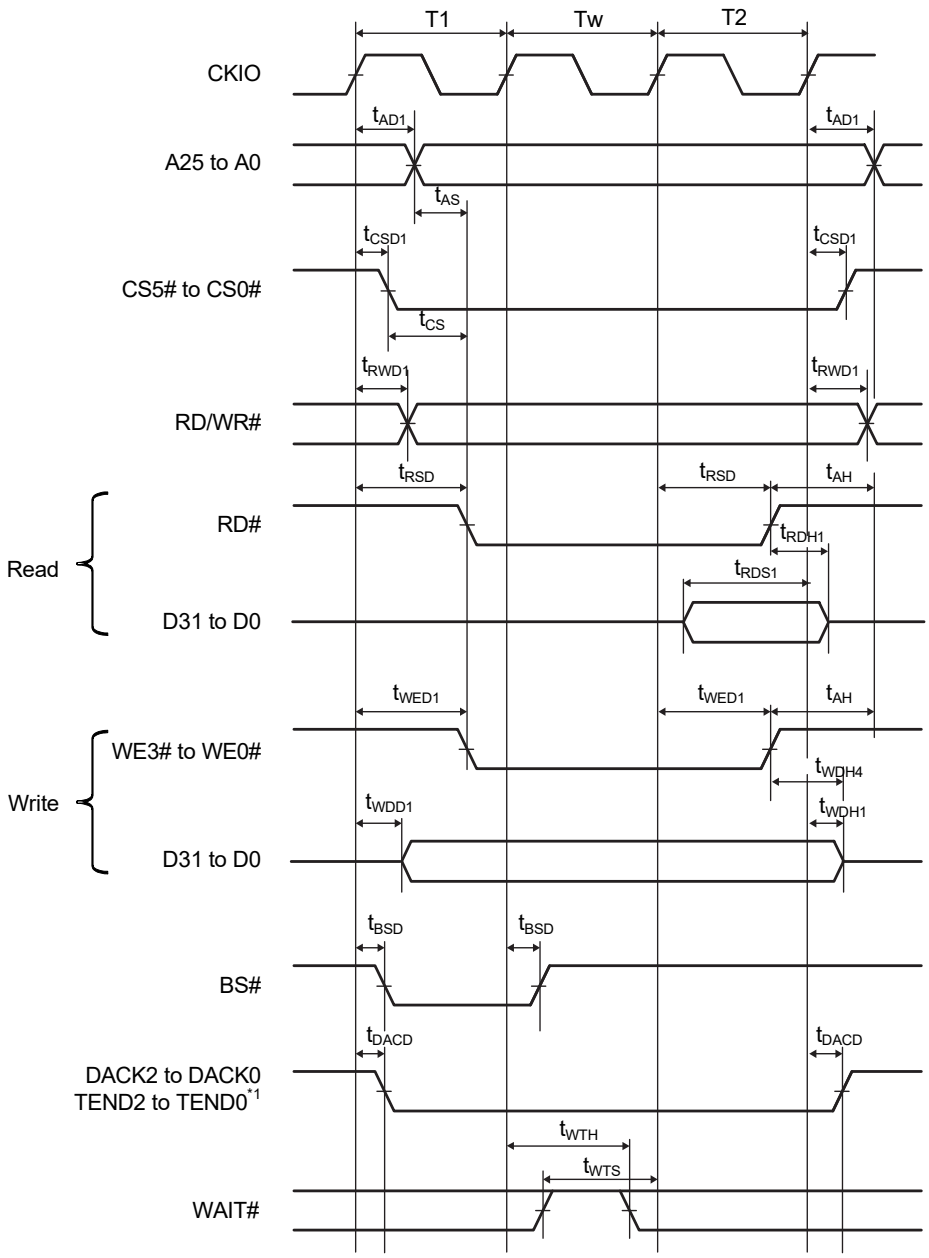
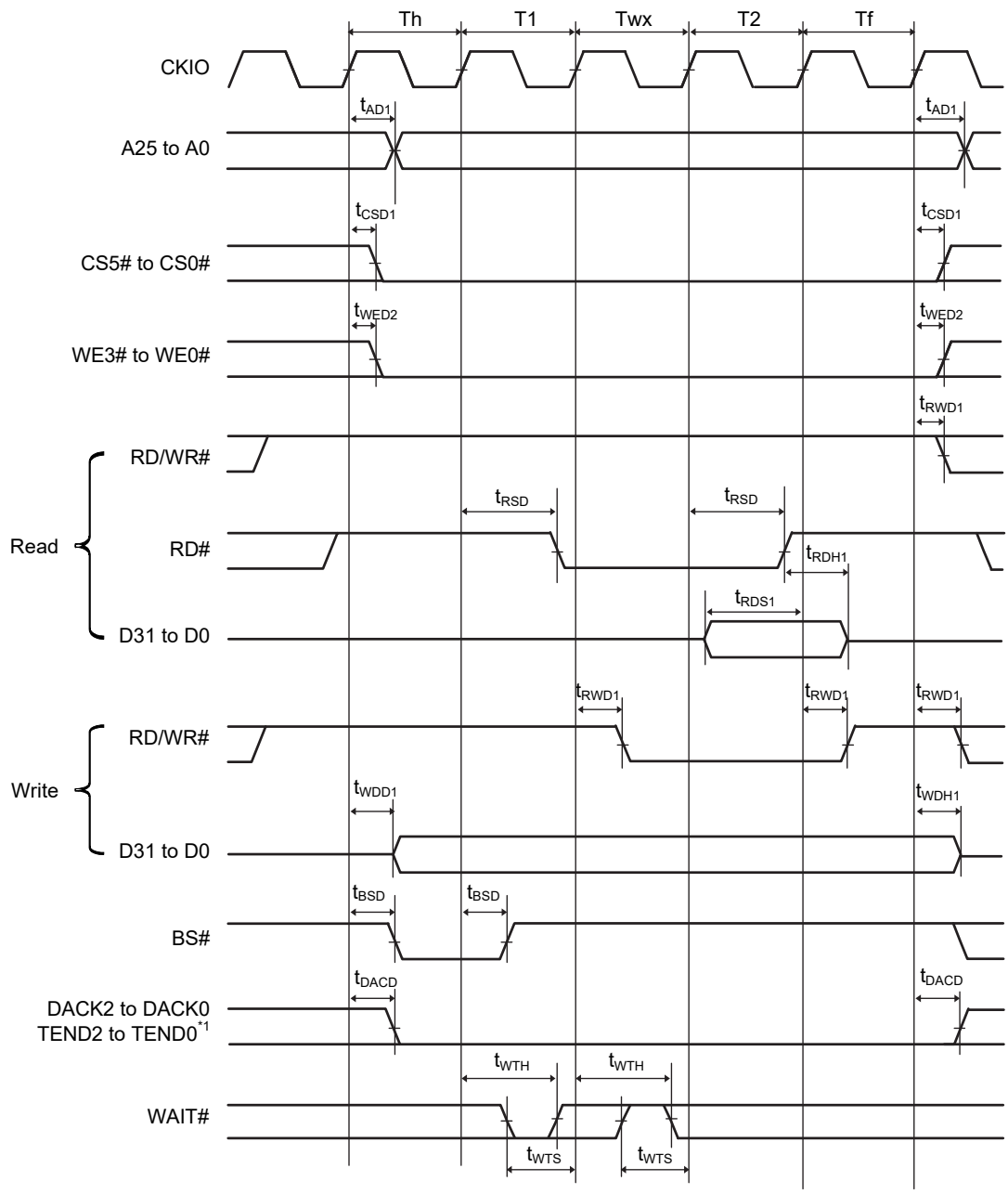



**Figure 2.7 LOCO Clock Oscillation Start Timing**



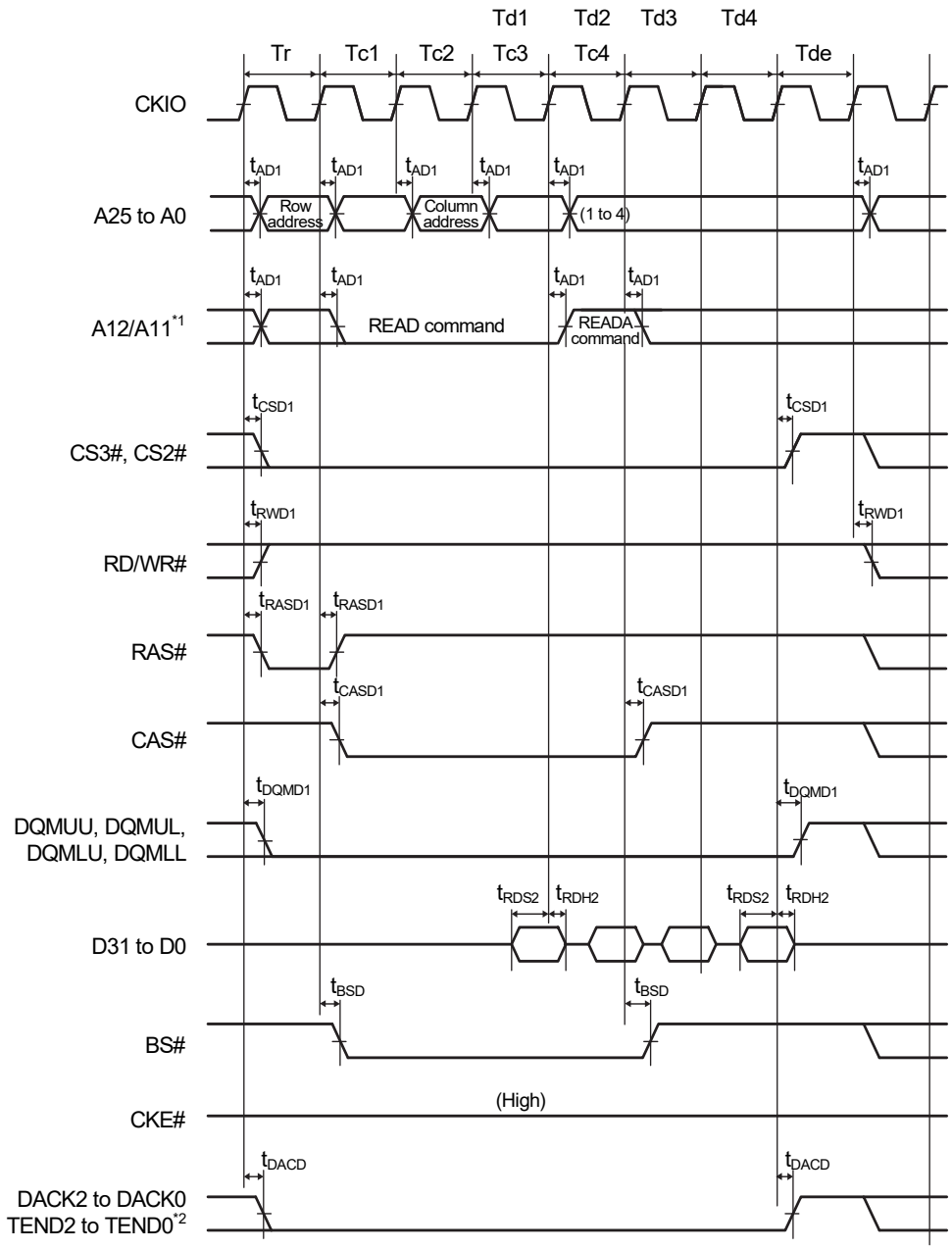

Note 1. DACKn and TENDn are waveforms when “active low” is specified.

**Figure 2.13 SRAM Interface Basic Bus Cycle (Software Wait 1)**



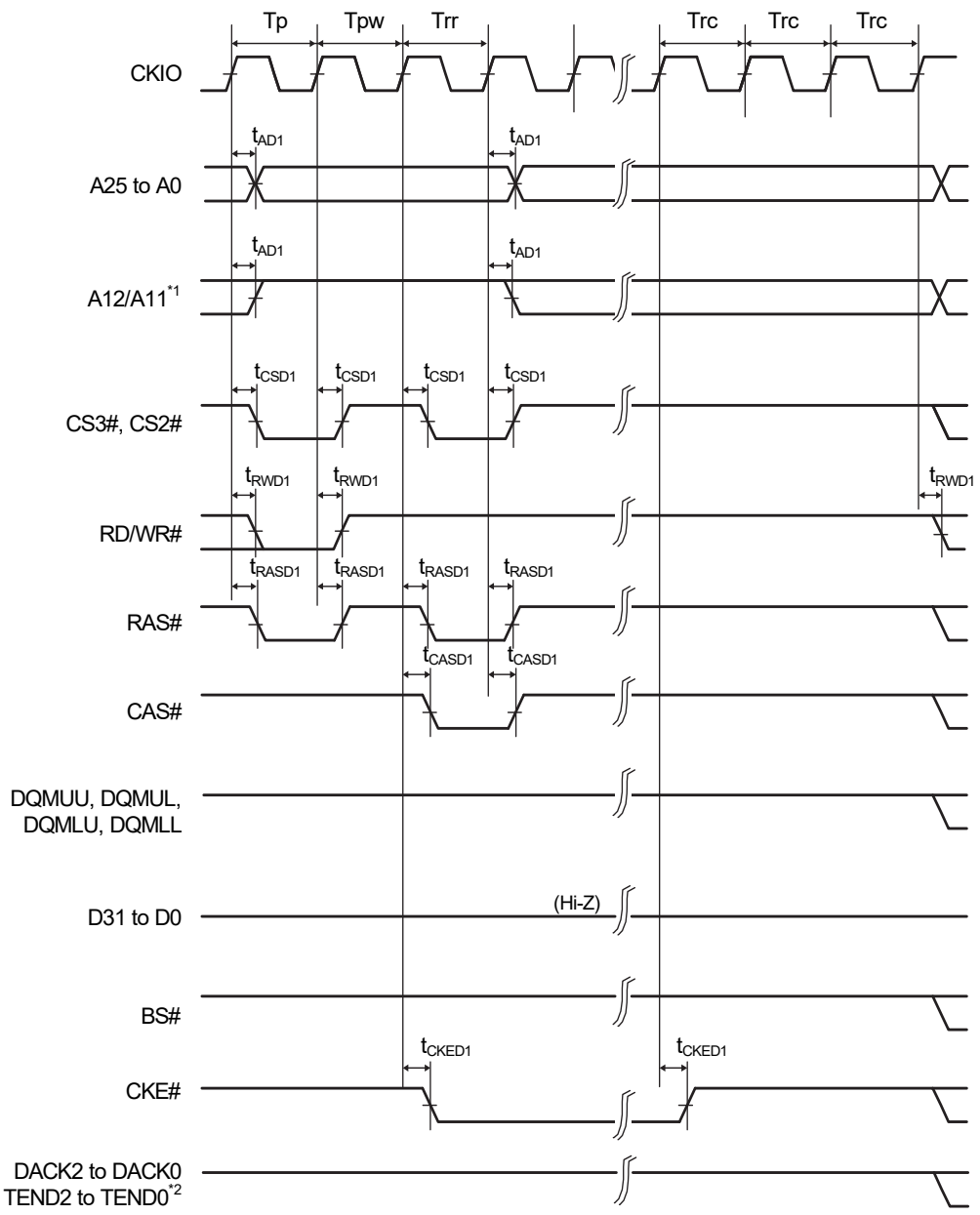

Note 1. DACKn and TENDn are waveforms when “active low” is specified.

**Figure 2.18 SRAM Bus Cycle with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1 Inserted, BAS = 1 (Write Cycle WE Control))**




Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

**Figure 2.22 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (with Auto Precharge, CAS Latency 2, WTRCD = 0 Cycles, WTRP = 1 Cycle)**




Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

**Figure 2.35 Synchronous DRAM Self-Refresh Timing (WTRP = 1 Cycle)**

## 2.4.4 DMAC Timing

**Table 2.18 DMAC Timing**

Output load conditions: $V_{OH}$ = VCCQ33 × 0.5, $V_{OL1}$ = VCCQ33 × 0.5, C = 30 pF

| Item | | Symbol | min*1 | max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DMAC | DREQ pulse width | $t_{DRQW}$ | $t_{PBcyc}$ × 2 | — | ns | Figure 2.37 |
| | DACK and TEND delay time | $t_{DACD}$ | 0 | 10 | ns | Figure 2.38 |

Note 1. $t_{PBcyc}$: PCLKB cycle

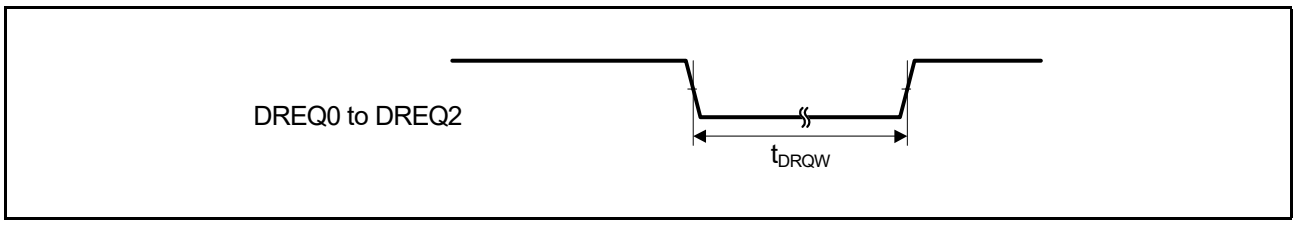



**Figure 2.37 DREQ Input Timing**

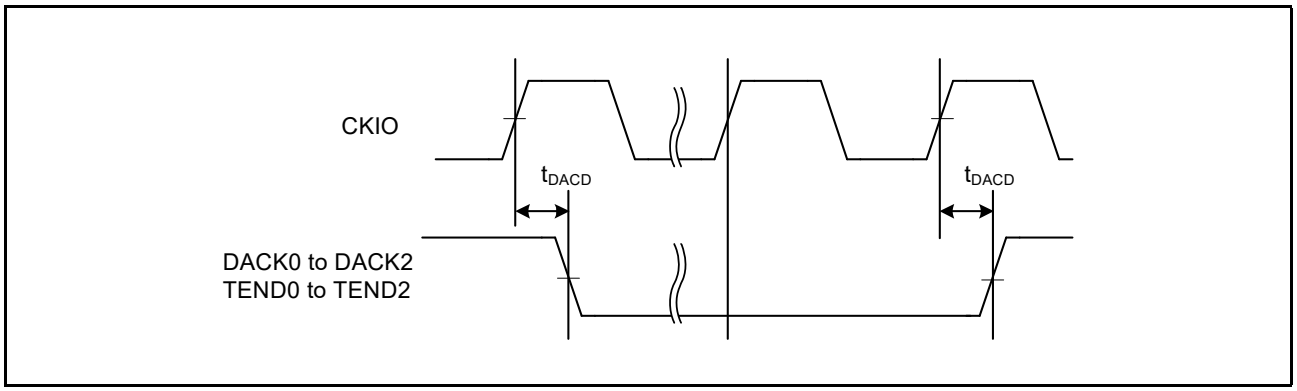



**Figure 2.38 DACK and TEND Output Timing**

### 2.4.5.6 GPTa Timing

**Table 2.24 GPTa Timing**

| Item | | | Symbol | min | max | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| GPTa | Input capture input pulse width | Single-edge setting | $t_{GTICW}$ | 3 | — | $t_{PCcyc}$ | Figure 2.46 |
| | | Both-edge setting | | 5 | — | | |
| | External trigger input pulse width | Single-edge setting | $T_{OTETW}$ | 1.5 | — | $t_{PCcyc}$ | Figure 2.47 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PCcyc}$: PCLKC cycle

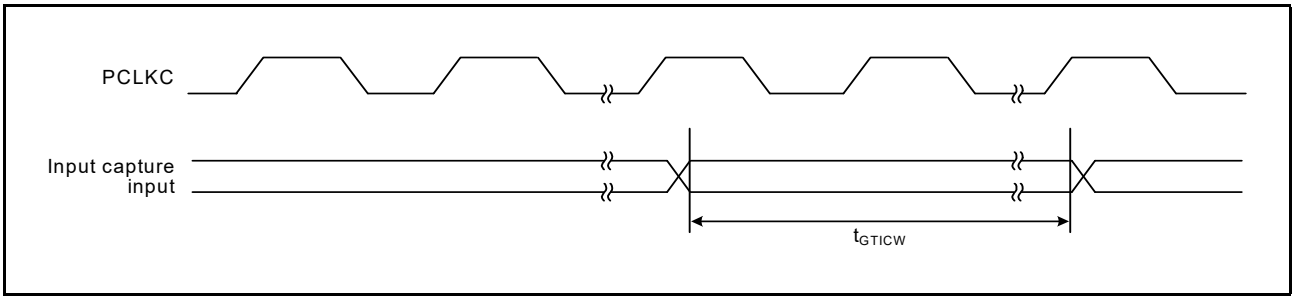



**Figure 2.46 GPTa Input Capture Input Timing**

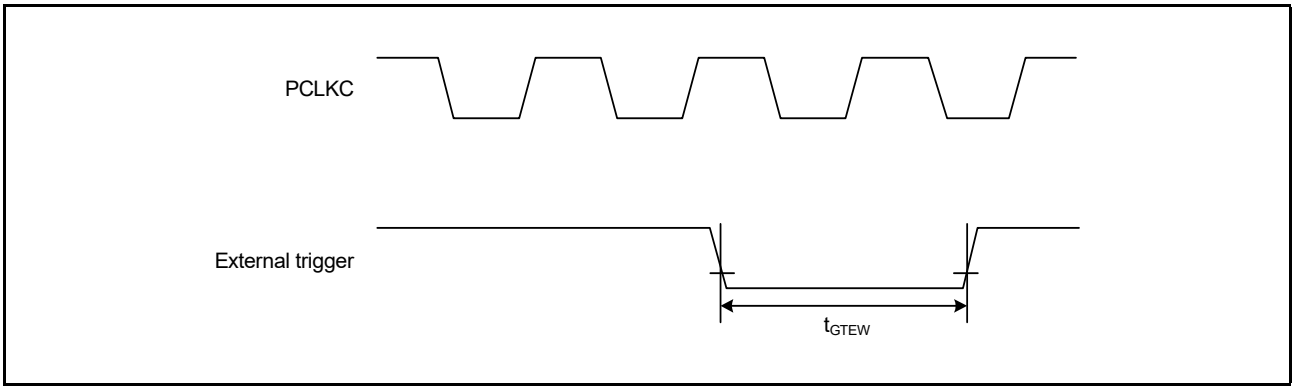
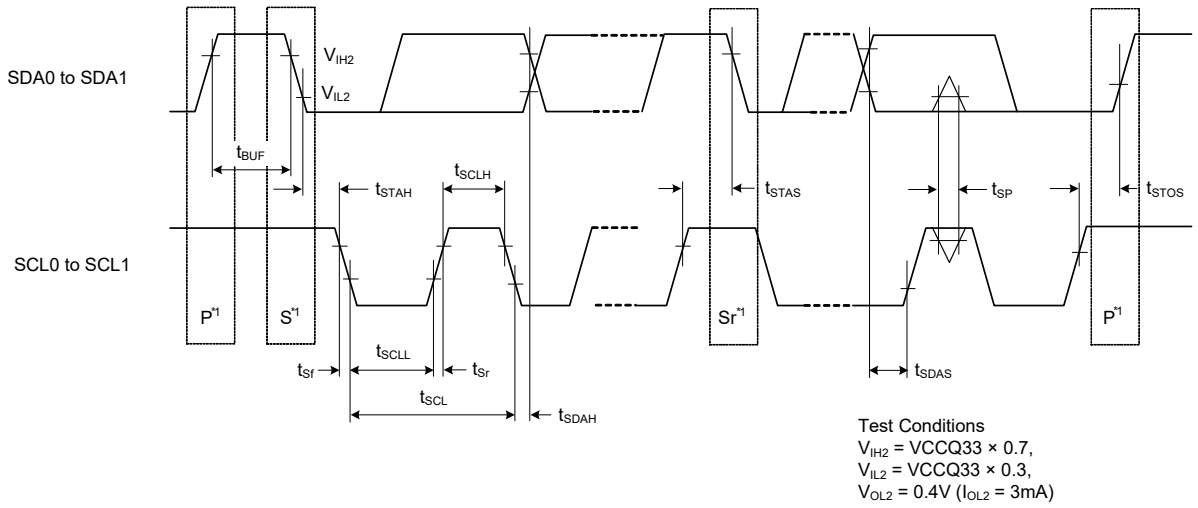



**Figure 2.47 GPTa External Trigger Input Timing**




Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

**Figure 2.64 RIICa Bus Interface Input/Output Timing**

### 2.4.5.15 Serial Management Interface Timing

#### (1) Timing

**Table 2.33 Serial Management Interface**

Output load conditions: $V_{OH}$ = VCCQ33 × 0.5, $V_{OL1}$ = VCCQ33 × 0.5, C = 30 pF

| Item | | Symbol | min | max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| MDIO | ETHn_MDC output cycle | $t_{MDC}$ | 80 | — | ns | Figure 2.78 |
| | ETHn_MDIO input setting time (to ETHn_MDC↑) | $t_{SMDIO}$ | 10 | — | ns | |
| | ETHn_MDIO input hold time (to ETHn_MDC↑) | $t_{HMDIO}$ | 0 | — | ns | |
| | ETHn_MDIO output delay time (to ETHn_MDC↓) | $t_{DMDIO}$ | — | 20 | ns | |

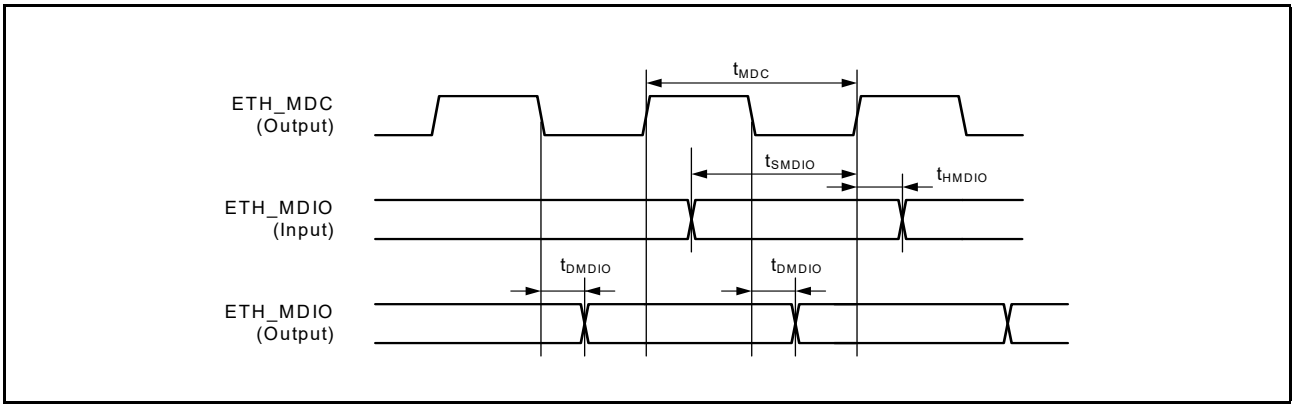



**Figure 2.78 Serial Management Access Timing**

## 2.5 USB Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

**Table 2.35 On-chip USB Full-Speed Characteristics (USB_DP, USB_DM Pin Characteristics)**

| Item | Symbol | min | typ | max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Rising time | $t_{FR}$ | 4 | — | 20 | ns | Figure 2.82 |
| Falling time | $t_{FF}$ | 4 | — | 20 | ns | |
| Rising/falling time ratio | $t_{FR} / t_{FF}$ | 90 | — | 111.11 | % | $t_{FR} / t_{FF}$ |

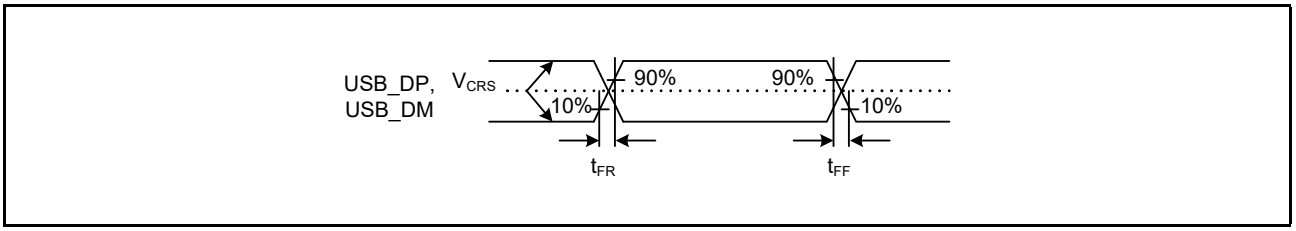



**Figure 2.82 USB_DP, USB_DM Output Timing (Full Speed)**

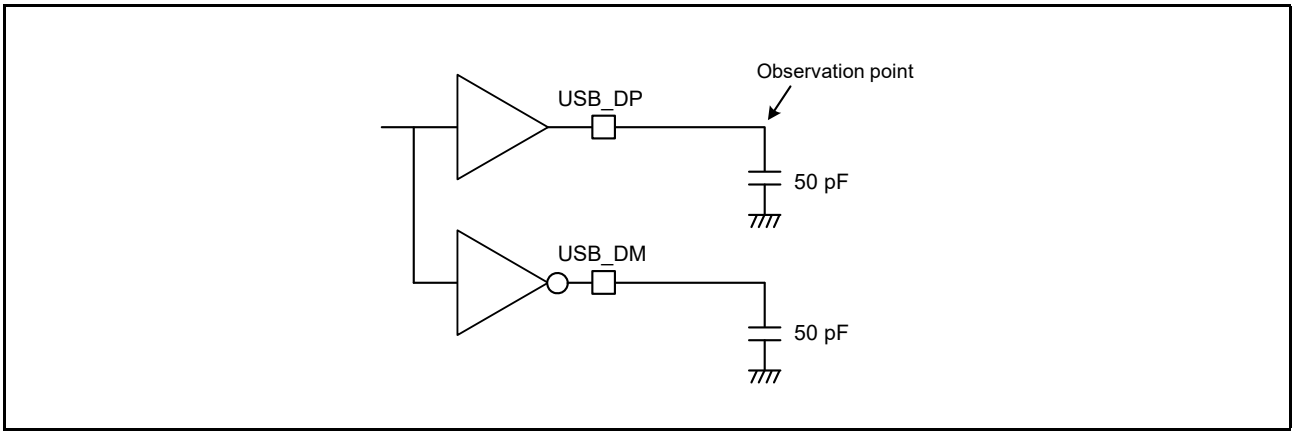



**Figure 2.83 Measurement Circuit (Full Speed)**

## 2.9 Debug Interface Timing

**Table 2.41 Debug Interface Timing**

Output load conditions: $V_{OH}$ = VCCQ33 – 0.5 V, $V_{OL1}$ = 0.4 V

| Item | Symbol | Min. | Max. | Unit | Reference Figure |
|---|---|---|---|---|---|
| TCK cycle time | $t_{TCKcyc}$ | 30 | — | ns | Figure 2.87 |
| TCK high pulse width | $t_{TCKH}$ | 0.4 | 0.6 | $t_{TCKcyc}$ | |
| TCK low pulse width | $t_{TCKL}$ | 0.4 | 0.6 | $t_{TCKcyc}$ | |
| TDI setup time | $t_{TDIS}$ | 5 | — | ns | Figure 2.88 Output load: 30 pF |
| TDI hold time | $t_{TDIH}$ | 5 | — | ns | |
| TMS/SWDIO setup time | $t_{TMSS}$ | 5 | — | ns | |
| TMS/SWDIO hold time | $t_{TMSH}$ | 5 | — | ns | |
| SWDIO delay time | $t_{SWDO}$ | — | 15 | ns | |
| TDO delay time | $t_{TDOD}$ | — | 15 | ns | |
| Capture register setup time | $t_{CAPTS}$ | 5 | — | ns | Figure 2.89 |
| Capture register hold time | $t_{CAPTH}$ | 5 | — | ns | |
| Update register delay time | $t_{UPDATED}$ | — | 15 | ns | |
| Trace clock cycle | $t_{TCYC}$ | 26.6 | — | ns | Figure 2.90 Output load: 15 pF |
| Trace data delay time | $t_{TDT}$ | 0.25 × $t_{TCYC}$ – 2 | 0.25 × $t_{TCYC}$ + 2 | ns | |

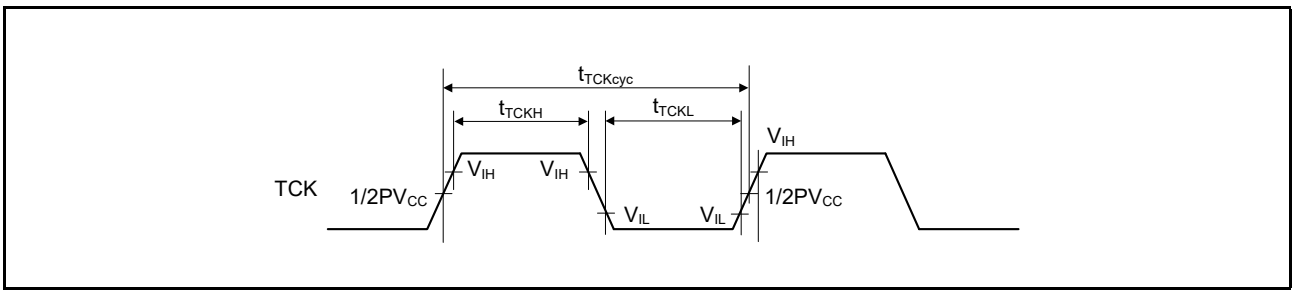



**Figure 2.87 TCK Input Timing**