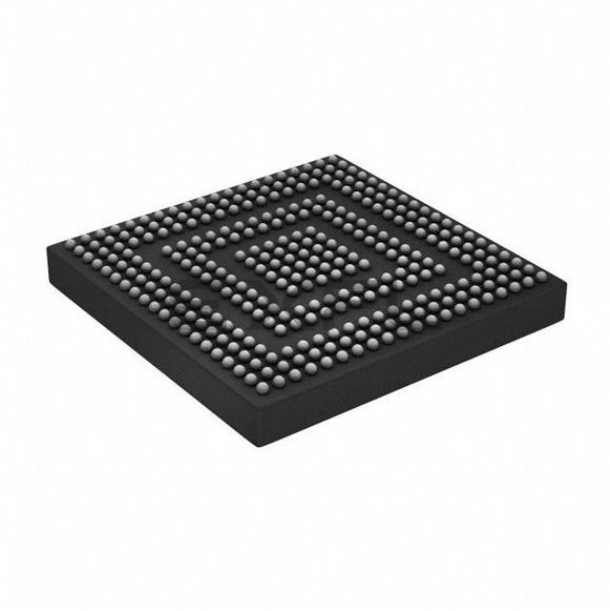

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R4F
Core Size	32-Bit Single-Core
Speed	600MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	209
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	320-FBGA
Supplier Device Package	320-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910007cbg-ac0

Table 1.1 Outline of Specifications (3 / 7)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 2 units*1 • Maximum of 32 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Input capture/output compare function • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Output of PWM waveforms in up to 30 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 4 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Digital noise filtering of signals from the input capture pins • Event linking by the ELC
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 9, 11, or 12 counter-input clock signals for each channel (with maximum operating frequency of 150 MHz) • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital noise filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC

Table 1.1 Outline of Specifications (4 / 7)

Classification	Module/Function	Description
Timers	General PWM timer (GPTa)	• 16 bits × 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 150 MHz) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: software, and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter function for signals on the input capture and external trigger pins • Event linking by the ELC
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units*1 • Pulse output with the MTU3a or TPUa output as a trigger • Maximum of 32 pulse-output possible
	Compare match timer (CMT)	• (16 bits × 2 channels) × 3 units • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Digital noise filter function for signals on the input capture pins • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel Products incorporating an R-IN engine: 14 bits × 2 channels • Select from among six counter-input clock signals for each channel (with maximum operating frequency of 75 MHz)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Low-speed on-chip oscillator (LOCO)/2 Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 (with maximum operating frequency of 120 MHz)
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3a / GPTa's waveform output pins • 4 pins for input from signal sources: POE0, POE4, POE8, POE10 • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by input clock oscillation-stoppage detection, PLL oscillation anomaly detection, or software • Additional programming of output control target pins is enabled

Table 1.4 Pin Functions (3 / 7)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3a)	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins
	MTIOC1A, MTIOC1B	I/O	TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins
	MTIOC2A, MTIOC2B	I/O	TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	TGRA7 to TGRD7 input capture input/output compare output/ PWM output pins
	MTIOC8A, MTIOC8B MTIOC8C, MTIOC8D	I/O	TGRA8 to TGRD8 input capture input/output compare output/ PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	External clock input pins for MTU3a
Port output enable 3 (POE3)	POE0#, POE4# POE8#, POE10#	Input	Input the request signal to place the MTU3a or GPTa in the high impedance state.
General-purpose PWM timer (GPTa)	GTIOC0A, GTIOC0B	I/O	GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins
	GTIOC1A, GTIOC1B	I/O	GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins
	GTIOC2A, GTIOC2B	I/O	GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins
	GTIOC3A, GTIOC3B	I/O	GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins
	GTETRG	Input	External trigger input pin for GPT0 to GPT3

Table 1.4 Pin Functions (4 / 7)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit (TPUa)	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	TPU0.TGRA0 to TPU0.TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	TPU0.TGRA1 and TPU0.TGRB1 input capture input/output compare output/PWM output pins
	TIOCA2, TIOCB2	I/O	TPU0.TGRA2 and TPU0.TGRB2 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	TPU0.TGRA3 to TPU0.TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	TPU0.TGRA4 and TPU0.TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	TPU0.TGRA5 and TPU0.TGRB5 input capture input/output compare output/PWM output pins
	TCLKA, TCLKB TCLKC, TCLKD	Input	External clock input pins for TPU0
	TIOCA6, TIOCB6 TIOCC6, TIOCD6	I/O	TPU1.TGRA0 to TPU1.TGRD0 input capture input/output compare output/PWM output pins
	TIOCA7, TIOCB7	I/O	TPU1.TGRA1 and TPU1.TGRB1 input capture input/output compare output/PWM output pins
	TIOCA8, TIOCB8	I/O	TPU1.TGRA2 and TPU1.TGRB2 input capture input/output compare output/PWM output pins
	TIOCA9, TIOCB9 TIOCC9, TIOCD9	I/O	TPU1.TGRA3 to TPU1.TGRD3 input capture input/output compare output/PWM output pins
	TIOCA10, TIOCB10	I/O	TPU1.TGRA4 and TPU1.TGRB4 input capture input/output compare output/PWM output pins
	TIOCA11, TIOCB11	I/O	TPU1.TGRA5 and TPU1.TGRB5 input capture input/output compare output/PWM output pins
	TCLKE, TCLKF TCLKG, TCLKH	Input	External clock input pins for TPU1
Programmable pulse generator (PPG)	PO0 to PO31	Output	Pulse output pins
Compare match timer W (CMTW)	TIC0 to TIC3	Input	CMTW input capture input pins
	TOC0 to TOC3	Output	CMTW output compare output pins
Serial communication interface with FIFO (SCIFA)	SCK0 to SCK4	I/O	Clock I/O pins
	RXD0 to RXD4	Input	Input the receive data.
	TXD0 to TXD4	Output	Output the transmit data.
	CTS0# to CTS4#	I/O	Hardware flow control input (transmission enable signal)/general output
	RTS0# to RTS4#	Output	Hardware flow control output (transmission request signal)/general output
I^2C bus interface (RIICa)	SCL0, SCL1	I/O	Clock I/O pins. The bus can be directly driven by the N-channel open drain.
	SDA0, SDA1	I/O	Data I/O pins. The bus can be directly driven by the N-channel open drain.

Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8)

Pin Number	Pin Name
C5	PL5 / ETH2_RXD2 / TIOCA8
C6	PB6 / ETH_MDC / TCLKA / SCK3 / RTS4# / MISO3
C7	PB3 / IRQ3 / CS1# / ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1 / MCLK0
C8	PB1 / ETH1_RXER / MTCLKA / TCLKC / CTS4#
C9	PF5 / ETH1_TXEN / MTIOC4A / GTIOC1A / TIC2
C10	P87 / AN1_ANEX1 / A23 / ETH1_TXC / ETH0_RXD0 / MTIOC4C / GTIOC1B / MCLK1
C11	PD6 / AN114 / A22 / ETH1_TXD2 / ETH0_TXD1 / TIC1 / MISO2 / MCLK2
C12	P53 / ETH1_INT / MISO2
C13	P51 / IRQ1 / PHYLINK1 / RSPCK2
C14	AN004
C15	AN000
C16	VREFL0
C17	VREFH0
C18	PD2 / AN110 / WAIT#
C19	P14 / CAS# / MTIOC4A / GTIOC1A / ENCIF10
C20	P13 / RAS# / MTIOC4C / GTIOC1B
D1	P81 / ETH0_RXER / TIOCC0 / CTS4#
D2	P80 / IRQ8 / ETH0_RXDV / TIOCC3 / RTS4#
D3	PU3 / ETH2_COL / TIOCD6 / TXD3
D18	PD0 / AN108 / CS4#
D19	P96 / AN106 / POE0# / POE10# / ENCIF09
D20	P95 / AN105 / IRQ13 / MTCLKA / CTS2#
E1	P84 / ETH0_COL / CATLINKACT1 / RXD4
E2	P82 / ETH0_TXEN / ETH1_CRS / TIOCD3 / SCK4 / RTS3# / USB_OVRCUR
E3	PU1 / ETH2_RXC / TIOCA11 / SCK3
E5	PU0 / ETH2_RXER / TIOCA10
E6	PL6 / ETH2_RXD3 / TIOCA9
E7	PL4 / IRQ4 / ETH2_RXD1
E8	PL2 / ETH2_TXEN / TIOCA6 / ADTRG1
E9	PL0 / ETH2_TXD0 / TIOCB9
E10	PK7 / ETH2_TXD2 / TIOCB7
E11	PK6 / ETH2_TXD3 / TIOCB6
E12	PD5 / AN113 / A21 / ETH1_TXD3 / ETH0_TXD0 / TIC0 / SSL20 / MCLK3
E13	P56 / BS# / ETH1_TXER
E14	PD4 / AN112 / ETH2_INT
E15	VCCQ33
E16	PD1 / AN109 / CS1#
E18	P97 / AN107 / IRQ7 / A25 / ADTRG1
E19	P94 / AN104 / IRQ4 / MTCLKB / RTS2# / ENCIF08
E20	P93 / AN103 / MTIOC1A / TIC3 / SCK2 / ENCIF07
F1	PC4 / CATI2CCLK / TCLKH / SCL0
F2	P83 / IRQ11 / ETH0_CRS / CATLINKACT0 / TXD4
F3	P85 / IRQ5 / CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN
F5	PU4 / MII2_MDC / TIOCC9 / CTS3#
F6	VSS

Table 1.5 Pin Assignments (320-Pin FBGA) (8 / 8)

Pin Number	Pin Name
Y15	P41 / BS# / SCK0
Y16	P42 / MTIOC7C / RXD0
Y17	P40 / MTIOC8A / TXD0
Y18	PS0 / MTIOC7D / AUDIO_CLK
Y19	P10 / IRQ0 / CKIO / TIOCA0 / TRACECLK
Y20	VSS

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (2 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
B7		PB2		MTIOC1A	ETH1_RXC / ETH0_RXD1 / CATSYNC1 / CATLATCH1 / SSL30	MDAT1		
B8		PC1			ETH1_RXD3 / PHYLINK0 / SDA1	MDAT2	IRQ9	
B9		PB7		MTIOC3B / GTIOC0A / TOC3	ETH1_RXD1			
B10		P86		MTIOC4B / GTIOC2A / TOC1	ETH1_TXD0 / RSPCK2			AN1_ANEX0
B11		PD7		MTIOC4D / GTIOC2B / TOC0	ETH1_TXD1			AN115
B12		P52			ETH0_INT / SSL20			
B13								AN006
B14								AN003
B15								AN001
B16	AVSS0							
B17	AVSS1							
B18	VREFL1							
B19		P16	CS4# / CS2#	MTIOC3B / GTIOC0A		ENCIF12		
B20		P15	CS3# / CKE	MTIOC3D / GTIOC0B		ENCIF11		
C1		PJ7			ETH0_RXD3 / CATLEDRUN / CTS3#		IRQ15	
C2		PJ6			ETH0_RXD2 / CATIRQ / SCK3		IRQ14	
C3		PU2		TIOCD9	ETH2_CRS / RXD3		IRQ2	
C4		PL7			ETH2_RXDV		IRQ15	
C5		PL5		TIOCA8	ETH2_RXD2			
C6		PB6		TCLKA	ETH_MDC / SCK3 / RTS4# / MISO3			
C7		PB3	CS1#		ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1	MCLK0	IRQ3	
C8		PB1		MTCLKA / TCLKC	ETH1_RXER / CTS4#			
C9		PF5		MTIOC4A / GTIOC1A / TIC2	ETH1_TXEN			
C10		P87	A23	MTIOC4C / GTIOC1B	ETH1_TXC / ETH0_RXD0	MCLK1		AN1_ANEX1
C11		PD6	A22	TIC1	ETH1_TXD2 / ETH0_TXD1 / MISO2	MCLK2		AN114
C12		P53			ETH1_INT / MISO2			
C13		P51			PHYLINK1 / RSPCK2		IRQ1	
C14								AN004

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
C15								AN000
C16	VREFL0							
C17	VREFH0							
C18		PD2	WAIT#					AN110
C19		P14	CAS#	MTIOC4A / GTIOC1A		ENCIF10		
C20		P13	RAS#	MTIOC4C / GTIOC1B				
D1		P81		TIOCC0	ETH0_RXER / CTS4#			
D2		P80		TIOCC3	ETH0_RXDV / RTS4#		IRQ8	
D3		PU3		TIOCD6	ETH2_COL / TXD3			
D18		PD0	CS4#					AN108
D19		P96		POE0# / POE10#		ENCIF09		AN106
D20		P95		MTCLKA	CTS2#		IRQ13	AN105
E1		P84			ETH0_COL / CATLINKACT1 / RXD4			
E2		P82		TIOCD3	ETH0_TXEN / ETH1_CRS / SCK4 / RTS3# / USB_OVRCUR			
E3		PU1		TIOCA11	ETH2_RXC / SCK3			
E5		PU0		TIOCA10	ETH2_RXER			
E6		PL6		TIOCA9	ETH2_RXD3			
E7		PL4			ETH2_RXD1		IRQ4	
E8		PL2		TIOCA6	ETH2_TXEN			ADTRG1
E9		PL0		TIOCB9	ETH2_TXD0			
E10		PK7		TIOCB7	ETH2_TXD2			
E11		PK6		TIOCB6	ETH2_TXD3			
E12		PD5	A21	TIC0	ETH1_TXD3 / ETH0_TXD0 / SSL20	MCLK3		AN113
E13		P56	BS#		ETH1_TXER			
E14		PD4			ETH2_INT			AN112
E15	VCCQ33							
E16		PD1	CS1#					AN109
E18		P97	A25				IRQ7	ADTRG1 / AN107
E19		P94		MTCLKB	RTS2#	ENCIF08	IRQ4	AN104
E20		P93		MTIOC1A / TIC3	SCK2	ENCIF07		AN103
F1		PC4		TCLKH	CATI2CCLK / SCL0			
F2		P83			ETH0_CRS / CATLINKACT0 / TXD4		IRQ11	

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (5 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
H12	VDD							
H13	VSS							
H15		PA6	D30 / A21	GTIOC3A	CTS2#	MDAT0	IRQ6	
H16		PA5	D29	TIOCA4	ETH0_INT / ETH1_TXER / TXD2	MCLK1		
H18		PA2	D26 / DREQ2	MTIOC3B / GTIOC0A	SSL02	MDAT2 / ENCIF05		
H19		PK0	CAS#	PO31		ENCIF11		
H20		PK1	CS5#			ENCIF12		
J1		PM6		PO19	CATLINKACT0		IRQ6	
J2		PM3		PO16	CATSYNC0 / CATLATCH0			
J3		PM2		TCLKE	CATSYNC1 / CATLATCH1 / RTS4#			
J5	TDO	P33						
J6	TRST#							
J8	VDD							
J9	VSS							
J10	VSS							
J11	VSS							
J12	VSS							
J13	VDD							
J15	VCCQ33							
J16	TRACEDATA7	PA1	D25	MTIOC3D / GTIOC0B	MISO0	AUDIO_CLK / MCLK3		
J18	TRACEDATA6	PA0	D24	MTIOC4A / GTIOC1A	MOSI0	MDAT3		
J19		PT7	A22 / DACK2			ENCIF10		
J20		PT6	A21 / DREQ2					
K1		PM7		PO20	CATLINKACT1			
K2		PM5		PO18	CATLEDSTER			
K3		PM4		PO17	CATLEDRUN			
K5	TDI	P34						
K6	PLLVDD1							
K8	VDD							
K9	VSS							
K10	VSS							
K11	VSS							
K12	VSS							
K13	VDD							
K15	VSS							
K16	TRACEDATA5	P77	D23	MTIOC4C / GTIOC1B	RSPCK0			

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
N3	RSTOUT#							
N5	RES#							
N6	PLLVSS0							
N8	VDD							
N9	VSS							
N10	VDD							
N11	VDD							
N12	VDD							
N13	VDD							
N15	TRACEDATA2	PE2	D10	MTCLKC / TIOCB4	SSL02		IRQ2	
N16	TRACEDATA4	PE4	D12	MTIOC0B / TIOCC0	RTS1# / SSL00			
N18	TRACEDATA5	PE5	D13	MTIOC0C / TIOCC3	TXD1 / MOSI0			
N19		PT2		TIOCA1 / TIOCB1 / PO27				
N20		PT3		TIOCA0 / TIOCB0 / PO28	CTS2#	ENCIF09	IRQ11	
P1	VSS_USB							
P2	VDD33_USB							
P3	USB_RREF							
P5		P31			USB_VBUSEN			
P6	VCCQ33							
P15		P06	D6	MTIOC2B / TIOCB0				
P16		P07	D7	MTIOC2A / TIOCB1				
P18	TRACEDATA3	PE3	D11	MTIOC0D / TIOCB5	CTS1# / SSL01		IRQ3	
P19		PT0		TIOCA3 / TIOCB3 / PO25	SCK2	ENCIF07	IRQ0	
P20		PT1		TIOCA2 / TIOCB2 / PO26	RTS2#	ENCIF08		
R1	USB_DP							
R2	USB_DM							
R3		P30			CRXD0 / USB_VBUSIN			
R5		PN0		MTIOC8D	SSL10			
R6		PN2		MTIOC8B	MOSI1		IRQ10	
R7		PG0	A1	PO2				
R8		PG2	A3	PO4 / TOC0	RSPCK1			
R9		PG7	A8	PO9				
R10		PH2	A11	MTIOC2A / PO12				
R11		PH4	A13	PO14			IRQ4	
R12		PH6	A15	MTIOC7D	RTS0#			
R13		P23	A0 / DACK1	MTIC5U	TXD0			
R14		P27	A20	MTIOC8C / TIOCB0	RTS0#			
R15		P47	WE3#/ DQMUU/ AH#	MTIOC6C				

Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP) (5 / 6)

Pin Number 176-Pin HLQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
134		P17	CS5#		ETH1_TXER / PHYRESETOUT#			ADTRG0
135	VCCQ33							
136	VREFH0							
137	VREFL0							
138	AVSS0							
139	AVCC0							
140								AN000
141								AN001
142								AN002
143								AN003
144								AN004
145								AN005
146								AN006
147								AN007
148	VDD							
149	VSS							
150		P51			PHYLINK1 / RSPCK2		IRQ1	
151		P54			CLKOUT25M1 / MOSI2			
152		P56	BS#		ETH1_TXER			
153		PD5	A21	TIC0	ETH1_TXD3 / ETH0_TXD0 / SSL20	MCLK3		
154		PD6	A22	TIC1	ETH1_TXD2 / ETH0_TXD1 / MISO2	MCLK2		
155		PD7		MTIOC4D / GTIOC2B / TOC0	ETH1_TXD1			
156		P86		MTIOC4B / GTIOC2A / TOC1	ETH1_TXD0 / RSPCK2			
157		P87	A23	MTIOC4C / GTIOC1B	ETH1_TXC / ETH0_RXD0	MCLK1		
158		PF5		MTIOC4A / GTIOC1A / TIC2	ETH1_TXEN			
159	VCCQ33							
160	VDD							
161	VSS							
162		PF6		MTIOC3D / GTIOC0B / TOC2	ETH1_RXD0			
163		PB7		MTIOC3B / GTIOC0A / TOC3	ETH1_RXD1			
164		PC0	WAIT#	GTETRG	ETH1_RXD2 / SCL1	MDAT3		

Table 2.3 DC Characteristics (2) [Power Supply]

Item	Type		Symbol	typ	max	Unit	Test Conditions
Normal operation	VDD	600MHz	VIcc	330	820	mA	Tj = -40 to 125 °C (R7S910018CBG, R7S910118CBG)
				273	752	mA	Tj = -40 to 125 °C (R7S910017CBG, R7S910117CBG)
				265	740	mA	Tj = -40 to 125°C (R7S910028CBG, R7S910128CBG)
				258	731	mA	Tj = -40 to 125 °C (R7S910013CBG, R7S910113CBG)
				209	673	mA	Tj = -40 to 125 °C (R7S910027CBG, R7S910127CBG)
				201	663	mA	Tj = -40 to 125 °C (R7S910007CBG, R7S910107CBG)
		450MHz		310	798	mA	Tj = -40 to 125 °C (R7S910016CBG, R7S910116CBG)
				253	730	mA	Tj = -40 to 125 °C (R7S910015CBG, R7S910115CBG)
				245	718	mA	Tj = -40 to 125 °C (R7S910026CBG, R7S910126CBG)
				238	709	mA	Tj = -40 to 125 °C (R7S910011CBG, R7S910111CBG)
				189	651	mA	Tj = -40 to 125 °C (R7S910025CBG, R7S910125CBG)
				181	641	mA	Tj = -40 to 125 °C (R7S910002CBG, R7S910006CBG, R7S910102CBG, R7S910106CBG)
				180	640	mA	Tj = -40 to 125 °C (R7S910001CFP, R7S910101CFP)
		300MHz		225	696	mA	Tj = -40 to 125 °C (R7S910036CBG, R7S910136CBG)
				169	629	mA	Tj = -40 to 125 °C (R7S910035CBG, R7S910135CBG)
				220	511	mA	Tj = -40 to 110 °C R7S9100022 R7S910023 R7S910122 R7S910123
	PLLVDD0 + PLLVDD1		PLLIcc	3.2	5	mA	
	VCCQ33		V33Icc	19*1, *2	—	mA	
	AVCC0		AV0Icc	2	5	mA	A/D conversion (unit 0)
	AVCC1		AV1Icc	0.7	1.5	mA	A/D conversion (unit 1)

2.4.2 Reset Timing and Interrupt Timing

Table 2.16 Reset Timing and Interrupt Timing

Item		Symbol	Min*1	typ	max	Unit	Test Conditions
RES# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	Figure 2.8
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
RES# rising time		$T_{risereset}$	—	—	150	μs	
TRST# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
TRST# rising time		$T_{risereset}$	—	—	150	μs	
NMI pulse width		t_{NMIW}	t_{Icyc} × 2	—	—	ns	Figure 2.9
IRQ pulse width		t_{IRQW}	t_{Icyc} × 2	—	—	ns	Figure 2.10
ETH_INT pulse width		t_{EINTW}	t_{Icyc} × 2	—	—	ns	Figure 2.11

Note 1. t_{Icyc}: ICLK cycle

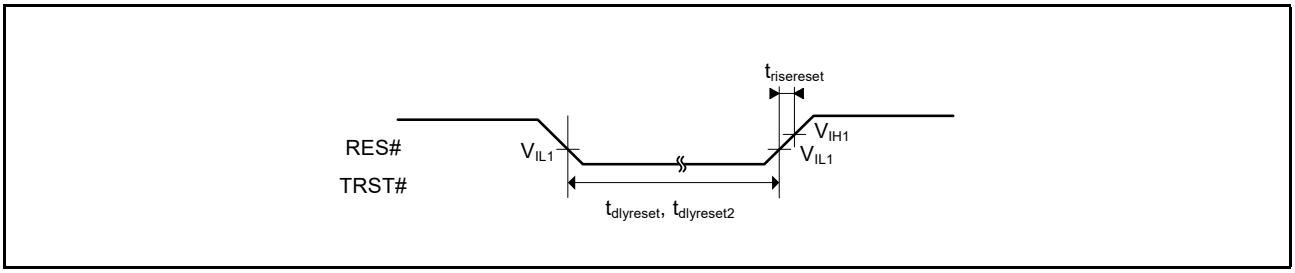


Figure 2.8 Reset Input Timing

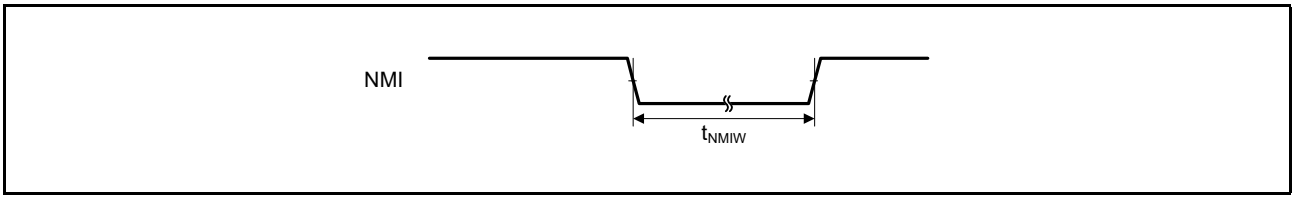


Figure 2.9 NMI Interrupt Input Timing

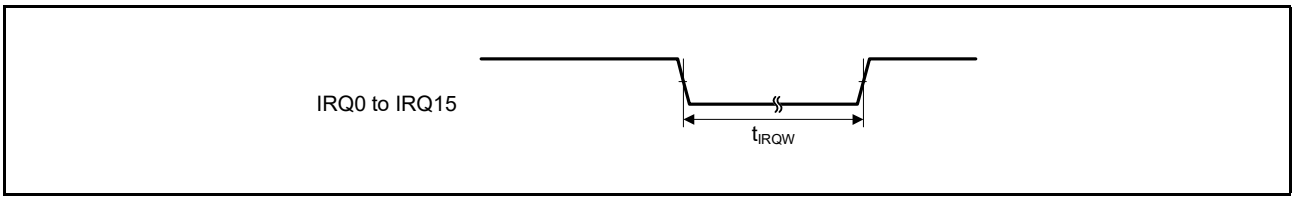
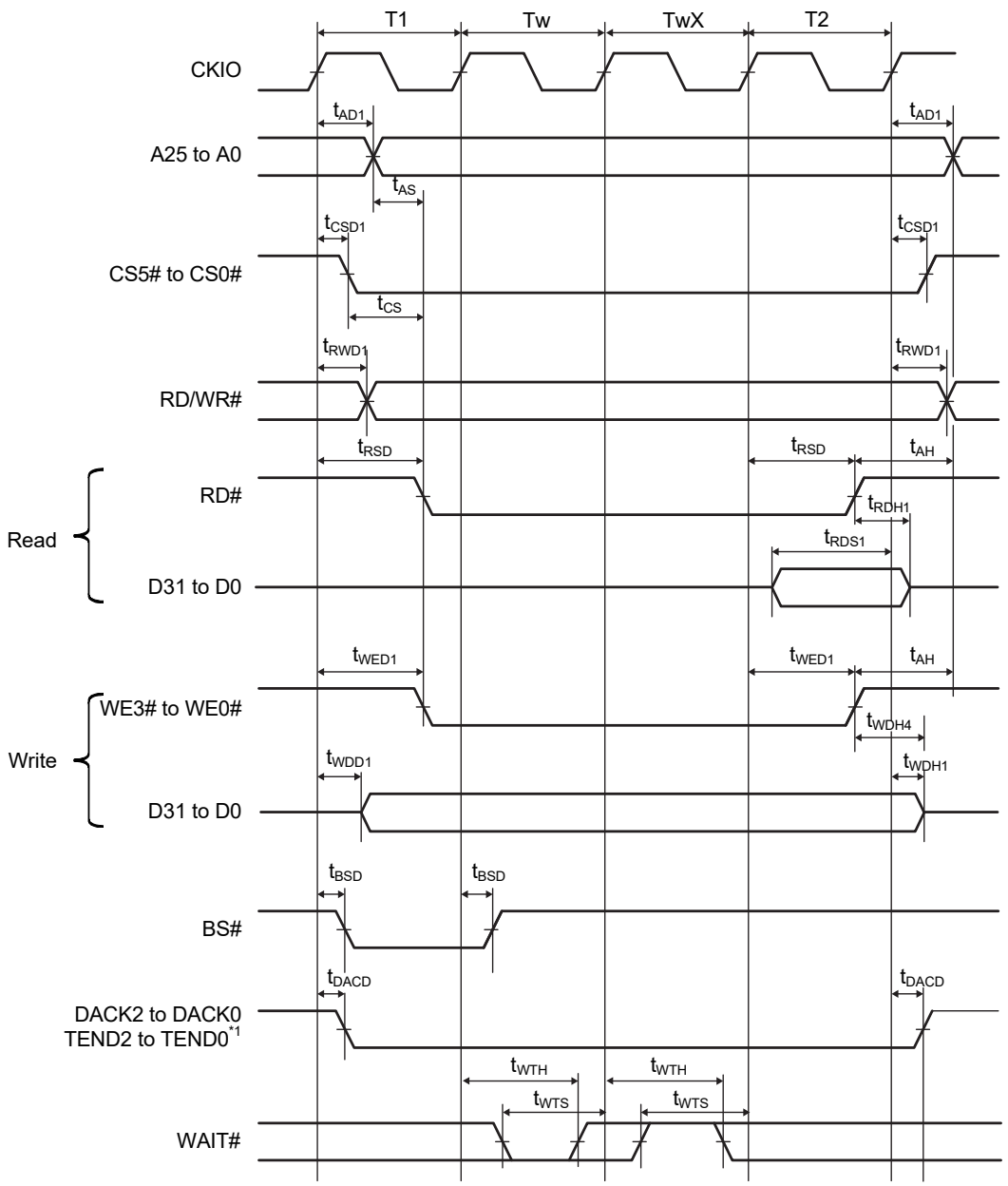
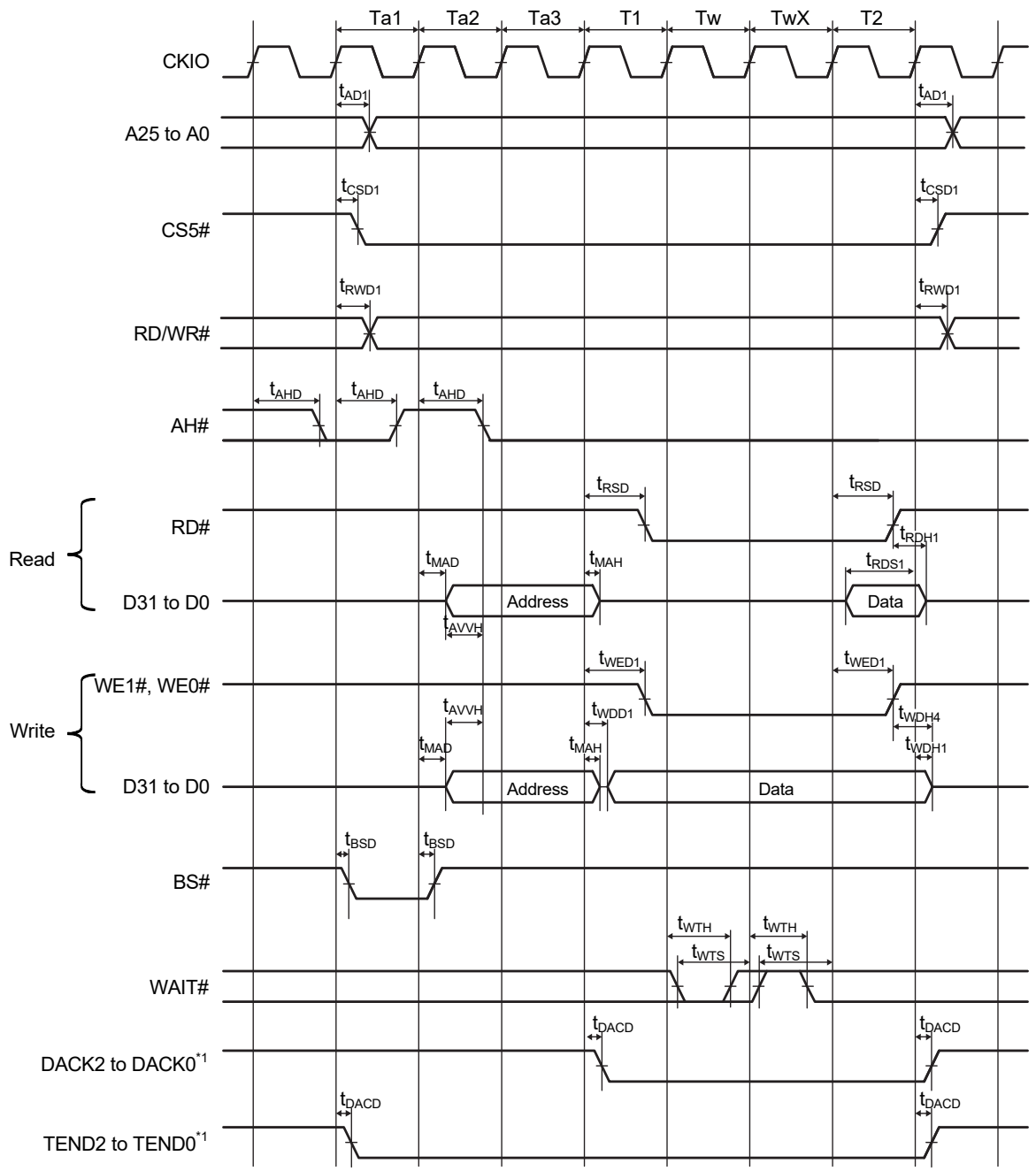


Figure 2.10 IRQ Interrupt Input Timing



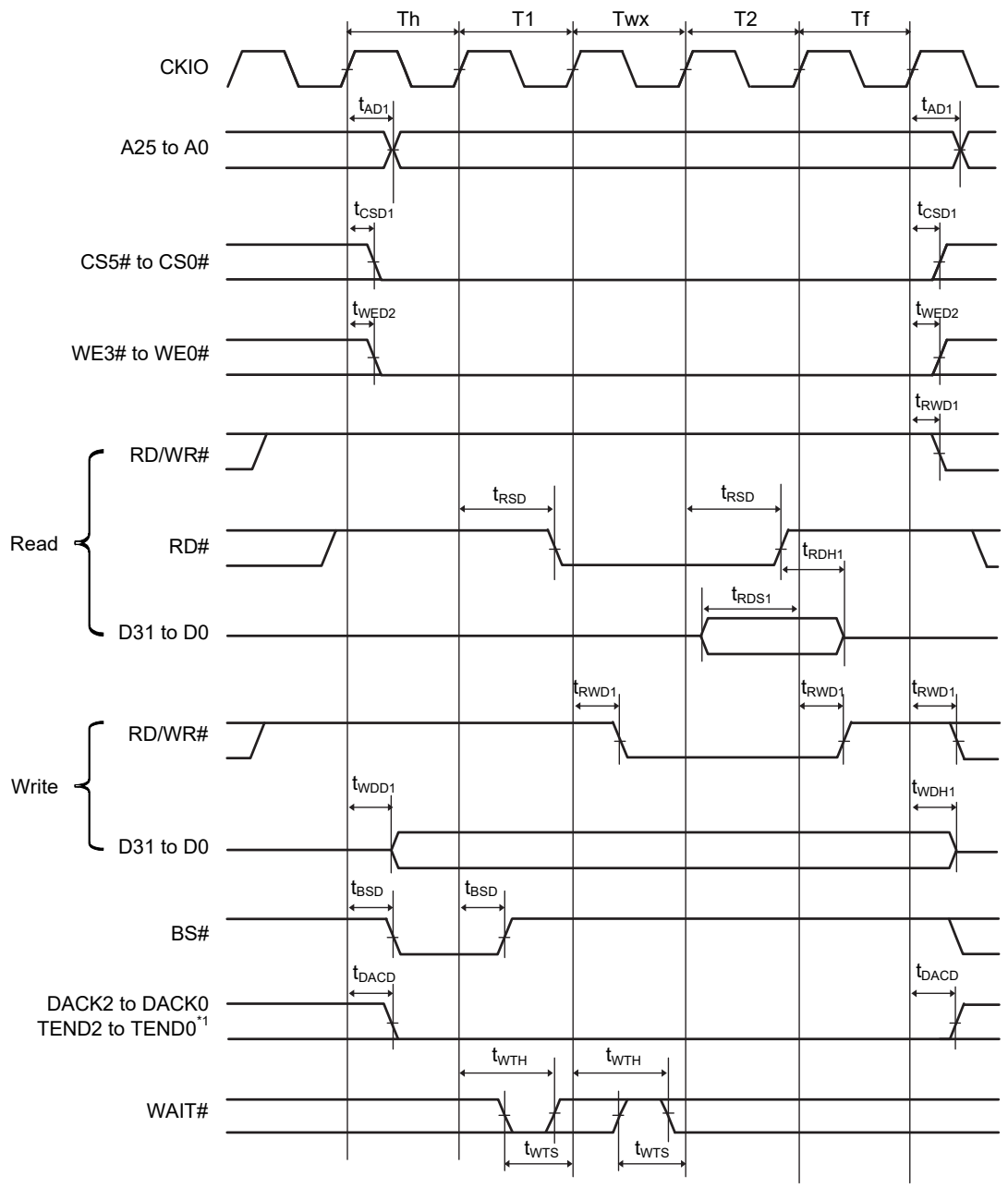
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.14 SRAM Interface Basic Bus Cycle (Software Wait 1, External Wait 1 Inserted)



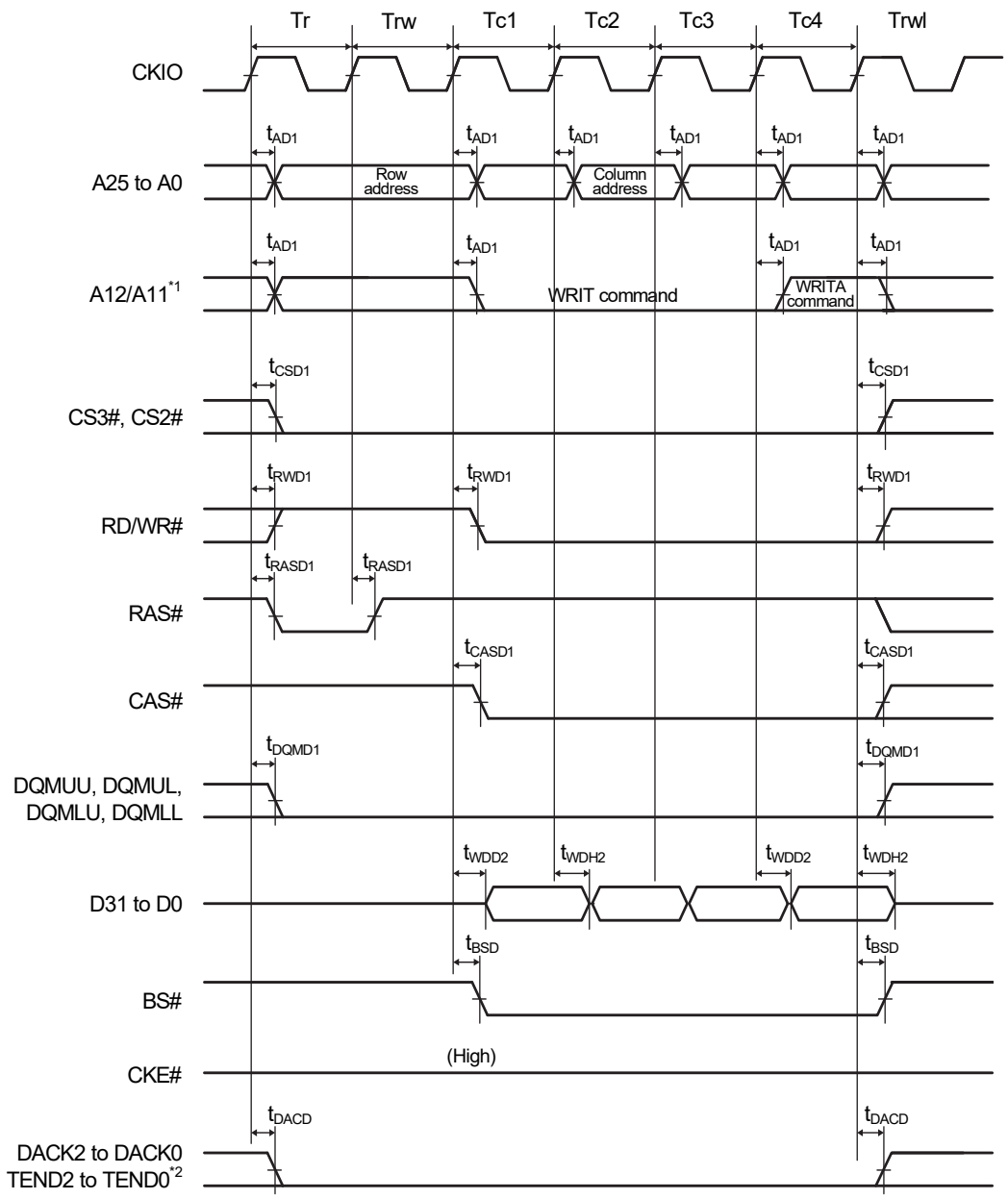
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.16 MPX-I/O Interface Bus Cycle (Address Cycle 3, Software Wait 1, External Wait 1 Inserted)



Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.18 SRAM Bus Cycle with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1 Inserted, BAS = 1 (Write Cycle WE Control))



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.27 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (with Auto Precharge, WTRCD = 1 Cycle, TRWL = 1 Cycle)

2.4.5.2 TPUa Timing

Table 2.20 TPUa Timing

Item			Symbol	min	max	Unit*1	Test Conditions
TPUa	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PDcyc}	Figure 2.40
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PDcyc}	Figure 2.41
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PDcyc}: PCLKD cycle

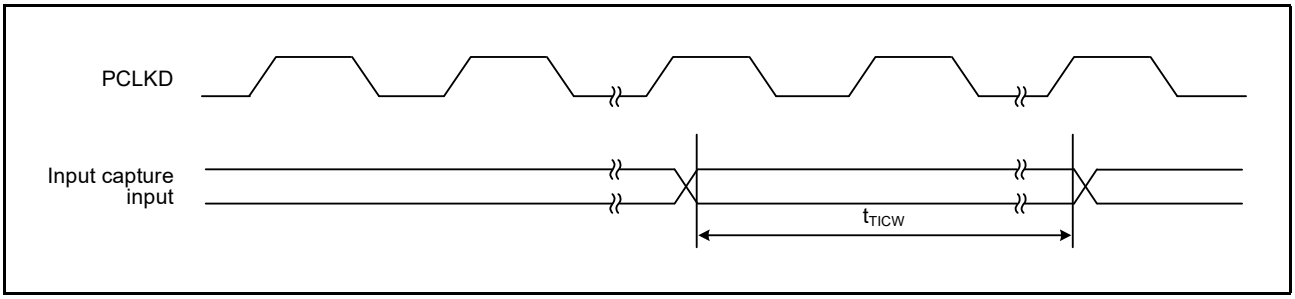


Figure 2.40 TPUa Input Capture Input Timing

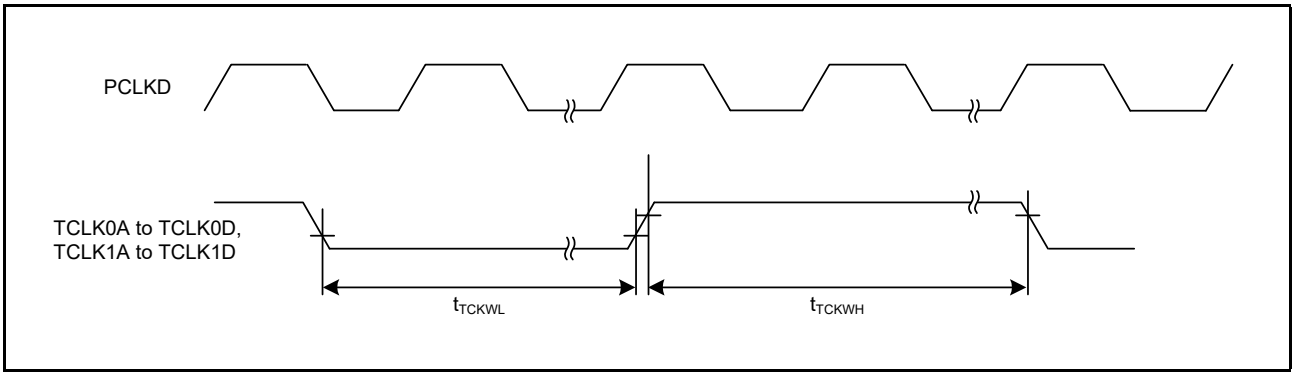


Figure 2.41 TPUa Clock Input Timing

REVISION HISTORY	RZ/T1 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.60	Nov. 14, 2014	—	First edition, issued
0.70	Dec. 25, 2014	Features	
		1	■ Operating temperature range: Heading title and description corrected
		Section 1 Overview	
		11	Table 1.3 List of Products (2 / 2): Note corrected
		21	Figure 1.3 Pin Arrangement (176-pin HLQFP): The names of pins 33, 34, 38, 39, and 91, corrected
		26	Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8): The names of pins M20 and P19, corrected
		27	Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8): The names of pins R14, R19, R20, T9, V7, and V8, corrected
		29	Table 1.5 Pin Assignments (320-Pin FBGA) (8 / 8): The names of pins Y16 and Y17, corrected
		30	Table 1.6 Pin Assignments (176-Pin HLQFP) (1 / 4): The names of pins 33, 34, 38, and 39, corrected
		31	Table 1.6 Pin Assignments (176-Pin HLQFP) (2 / 4): The names of pins 58, 59, 60, 79, 82, and 83, corrected
		32	Table 1.6 Pin Assignments (176-Pin HLQFP) (3 / 4): The names of pins 91 and 110, corrected
		33	Table 1.6 Pin Assignments (176-Pin HLQFP) (4 / 4): The names of pins 136, 153, 154, 155, 156, and 157, corrected
		39	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (6 / 10): The name of pin M20, corrected
		40	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10): The names of pins P19, R8, and R14, corrected
		41	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10): The names of pins R19, R20, T9, V7, and V8, corrected
		42	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10): The names of pins Y16 and Y17, corrected
1.10	Jul. 08, 2016	Feature	
		1	Wholly amended
		1. Overview	
		2 to 49	Wholly amended
		2. Electrical Characteristics	
		50 to 129	Newly added
1.20	Mar. 02, 2017	1. Overview	
		9	Table 1.2 Comparison of Functions for Different Packages: Functions of ETHERC and ECATC, modified. Note 1 added.
		12	Figure 1.1 Block Diagram: Functional blocks of ECATC and ETHERC, modified. Note 1 modified.
		20	Figure 1.2 Pin Arrangement (320-Pin FBGA) (Top View): Pin ERROROUT#, modified
		2. Electrical Characteristics	
		53	Table 2.3 DC Characteristics (2) [Power Supply] Test conditions, modified: Product part no. added
		55	Table 2.4 DC Characteristics (3) [Except for USB2.0 Host/Function-Related Pins] Item modified: "Input pull-up MOS current and resistance" and "Input pull-down MOS current and resistance" R_{pu1}, R_{pu2}, R_{pd1}, and R_{pd2} were added. Test conditions for "Input pull-down MOS current and resistance" were modified.
		58	Table 2.10 Operating Frequency: Notes 1 to 3, added. The max. value of the CPU clock (CPUCLK), modified.

Rev.	Date	Description	
		Page	Summary
1.40	Jan. 19, 2018	All	Cortex-R4F changed to Cortex-R4
			Terms corrected (Ether Switch → Ethernet switch; Ether Mac → Ethernet Mac; Ether PHY → Ethernet PHY; Ether clock(s) → Ethernet clock(s); receive buffer(s) → reception buffer(s); transmit buffer(s) → transmission buffer(s); transmit/receive buffer(s) → transmission/reception buffer(s); transmit mode → transmission mode; receive mode → reception mode; compare match counter (CMCNT) → compare match timer counter (CMCNT); compare match constant register (CMCOR) → compare match timer constant register (CMCOR); low active → active low; high active → active high; valley → trough)
		Features	
		1	■ Encoder interfaces, changed ■ Various communications interfaces: Features of Ethernet changed
		1. Overview	
		2	1.1 Outline of Specifications: "Cortex®-R4F processor" changed to "Cortex®-R4 processor with FPU"
		2	Table 1.1 Outline of Specifications (1 / 7): Registered trademark symbol added to "Thumb"; description of "Clock" changed
		8	Table 1.1 Outline of Specifications (7 / 7): Description of the encoder interfaces changed
		16	Table 1.4 Pin Functions (4 / 7): CTS0# to CTS4#: I/O and functional description changed; RTS0# to RTS4#: Functional description changed
		19	Table 1.4 Pin Functions (7 / 7): ENCIF07 to ENCIF12 changed to ENCIF00 to ENCIF12
		22	Table 1.5 Pin Assignments (320-Pin FBGA) (1 / 8): ENCIF12 added to B19; ENCIF11 added to B20
		23	Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8): ENCIF10 added to C19; ENCIF09 added to D19; ENCIF08 added to E19
		24	Table 1.5 Pin Assignments (320-Pin FBGA) (3 / 8): ENCIF11 added to H19; ENCIF12 added to H20
		25	Table 1.5 Pin Assignments (320-Pin FBGA) (4 / 8): ENCIF10 added to J19
		26	Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8): ENCIF09 added to N20; ENCIF08 added to P20
		27	Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8): ENCIF09 added to U3
		28	Table 1.5 Pin Assignments (320-Pin FBGA) (7 / 8): ENCIF10 added to W3; ENCIF11 added to W4; ENCIF08 added to W10; ENCIF12 added to Y4
		35	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (2 / 10): ENCIF12 added to B19 under "Others"; ENCIF11 added to B20 under "Others"
		36	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10): ENCIF10 added to C19 under "Others"; ENCIF09 added to D19 under "Others"; ENCIF08 added to E19 under "Others"
		38	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (5 / 10); ENCIF11 added to H19 under "Others"; ENCIF12 added to H20 under "Others"; ENCIF10 added to J19 under "Others"
		40	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10): ENCIF09 added to N20 under "Others"; ENCIF08 added to P20 under "Others"
		41	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10): ENCIF09 added to U3 under "Others"
		42	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10): ENCIF10 added to W3 under "Others"; ENCIF11 added to W4 under "Others"; ENCIF08 added to W10 under "Others; ENCIF12 added to Y4
		2. Electrical Characteristics	
		54	Table 2.3 DC Characteristics (2) [Power Supply]: Entries added to the "300MHz" row of VDD
		65, 66	Table 2.17 Bus Timing: "CKIO = 75MHz" changed to "CKIO = 1/tCKcyc; "tcyc" changed to "tCKcyc"; entries for "Address delay time 1", "CS# delay time 1", "Read/write delay time 1", "Read data setup time 1 to 3" and "WAIT# setup time" changed; Notes 1, 3, and 4 changed
		102	Table 2.27 RSPIa Timing: Note 2 changed (SSLND → SPCKD): Note 3 added
		111	Figure 2.64 RIICa Bus Interface Input/Output Timing: SDA0 to SDA3 and SCL0 to SCL3 deleted