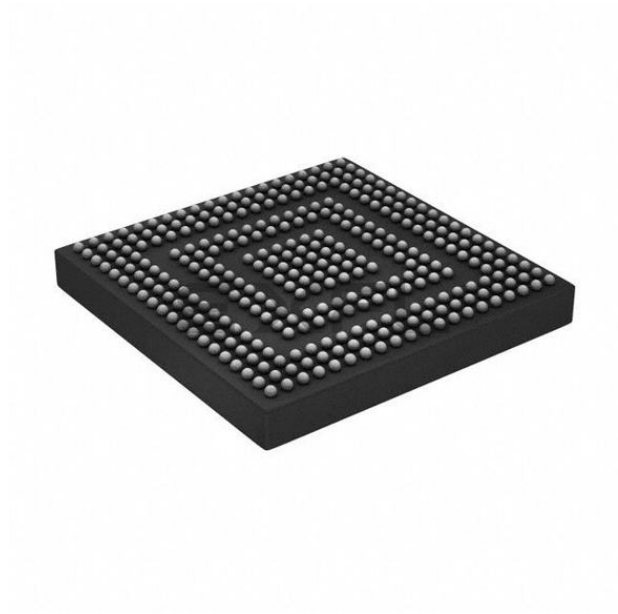
Renesas Electronics America Inc - R7S910011CBG#AC0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R4F
Core Size	32-Bit Single-Core
Speed	450MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	209
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	320-FBGA
Supplier Device Package	320-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910011cbg-ac0

Table 1.3 List of Products (2 / 2)

Part No.	Package	CPU	On-Chip Extended SRAM Capacity	EtherCAT	Operating Frequency (max.)	Security Function *1	Optional Function
R7S910118CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Available	Encoder I/F R-IN Engine (CM3 : 150 MHz)
R7S910025CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	—
R7S910125CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	—
R7S910026CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	Encoder I/F
R7S910126CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	Encoder I/F
R7S910027CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	—
R7S910127CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	—
R7S910028CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	Encoder I/F
R7S910128CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	Encoder I/F
R7S910035CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	—
R7S910135CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	—
R7S910036CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	Encoder I/F
R7S910136CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	Encoder I/F

Note: See the separate documents regarding the encoder I/F.

Note 1. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.

Table 1.4 Pin Functions (2 / 7)

Classifications	Pin Name	I/O	Description
Bus state controller (BSC)	A0 to A25	Output	Output the address.
	D0 to D31	I/O	Input and output the data.
	CS0# to CS5#	Output	Output the chip select signal for the external memory or device.
	RD#	Output	Outputs the strobe signal which indicates reading is in progress.
	RD/WR#	Output	Outputs the strobe signal which indicates the read or write access.
	BS#	Output	Outputs the status signal which indicates the start of bus cycles.
	AH#	Output	Outputs the address hold signal for the device that uses the multiplexed I/O bus.
	WAIT#	Input	Inputs the external wait control signal which inserts a wait cycle into the bus cycles.
	WE0#	Output	Outputs the write strobe signal to D7 to D0.
	WE1#	Output	Outputs the write strobe signal to D15 to D8.
	WE2#	Output	Outputs the write strobe signal to D23 to D16.
	WE3#	Output	Outputs the write strobe signal to D31 to D24.
	DQMLL	Output	Outputs the data mask enable signal to D7 to D0 when SDRAM is connected.
	DQMLU	Output	Outputs the data mask enable signal to D15 to D8 when SDRAM is connected.
	DQMUL	Output	Outputs the data mask enable signal to D23 to D16 when SDRAM is connected.
	DQMUU	Output	Outputs the data mask enable signal to D31 to D24 when SDRAM is connected.
	RAS#	Output	Outputs the low-address strobe signal to the SDRAM. This pin should be connected to the RAS pin on the SDRAM.
	CAS#	Output	Outputs the column-address strobe signal to the SDRAM. This pin should be connected to the CAS pin on the SDRAM.
	CKE	Output	Outputs the clock enable signal to the SDRAM. This pin should be connected to the CKE pin on the SDRAM.
Direct memory access controller (DMAC)	DREQ0 to DREQ2	Input	Input the DMA transfer request signal from the external device.
	DACK0 to DACK2	Output	Output the acknowledge signal which indicates acceptance of the DMA transfer request from the external device.
	TEND0 to TEND2	Output	Output the DMA transfer end signal.
Interrupt	NMI	Input	Inputs the non-maskable interrupt request signal.
	IRQ0 to IRQ15	Input	Input the external interrupt request signal.
	ETH0_INT, ETH1_INT, ETH2_INT	Input	Input the Ethernet PHY interrupt request signal.

Table 1.4 Pin Functions (4 / 7)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit (TPUa)	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	TPU0.TGRA0 to TPU0.TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	TPU0.TGRA1 and TPU0.TGRB1 input capture input/output compare output/PWM output pins
	TIOCA2, TIOCB2	I/O	TPU0.TGRA2 and TPU0.TGRB2 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	TPU0.TGRA3 to TPU0.TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	TPU0.TGRA4 and TPU0.TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	TPU0.TGRA5 and TPU0.TGRB5 input capture input/output compare output/PWM output pins
	TCLKA, TCLKB TCLKC, TCLKD	Input	External clock input pins for TPU0
	TIOCA6, TIOCB6 TIOCC6, TIOCD6	I/O	TPU1.TGRA0 to TPU1.TGRD0 input capture input/output compare output/PWM output pins
	TIOCA7, TIOCB7	I/O	TPU1.TGRA1 and TPU1.TGRB1 input capture input/output compare output/PWM output pins
	TIOCA8, TIOCB8	I/O	TPU1.TGRA2 and TPU1.TGRB2 input capture input/output compare output/PWM output pins
	TIOCA9, TIOCB9 TIOCC9, TIOCD9	I/O	TPU1.TGRA3 to TPU1.TGRD3 input capture input/output compare output/PWM output pins
	TIOCA10, TIOCB10	I/O	TPU1.TGRA4 and TPU1.TGRB4 input capture input/output compare output/PWM output pins
	TIOCA11, TIOCB11	I/O	TPU1.TGRA5 and TPU1.TGRB5 input capture input/output compare output/PWM output pins
	TCLKE, TCLKF TCLKG, TCLKH	Input	External clock input pins for TPU1
Programmable pulse generator (PPG)	PO0 to PO31	Output	Pulse output pins
Compare match timer W (CMTW)	TIC0 to TIC3	Input	CMTW input capture input pins
	TOC0 to TOC3	Output	CMTW output compare output pins
Serial communication interface with FIFO (SCIFA)	SCK0 to SCK4	I/O	Clock I/O pins
	RXD0 to RXD4	Input	Input the receive data.
	TXD0 to TXD4	Output	Output the transmit data.
	CTS0# to CTS4#	I/O	Hardware flow control input (transmission enable signal)/general output
	RTS0# to RTS4#	Output	Hardware flow control output (transmission request signal)/general output
I^2C bus interface (RIICa)	SCL0, SCL1	I/O	Clock I/O pins. The bus can be directly driven by the N-channel open drain.
	SDA0, SDA1	I/O	Data I/O pins. The bus can be directly driven by the N-channel open drain.

Table 1.4 Pin Functions (5 / 7)

Classifications	Pin Name	I/O	Description
Ethernet controller (ETHERC)	ETH0_TXC, ETH1_TXC, ETH2_TXC	Input	Input the 10 M/100 M transmission clock (2.5 MHz/25 MHz).
	ETH0_TXEN, ETH1_TXEN, ETH2_TXEN	Output	Output the transmission enable signal.
	ETH0_TXER, ETH1_TXER, ETH2_TXER	Output	Output the transmission error signal.
	ETH0_TXD0 to 3, ETH1_TXD0 to 3, ETH2_TXD0 to 3	Output	Output the transmission data signal.
	ETH0_RXC, ETH1_RXC, ETH2_RXC	I/O	Receive clock I/O pins
	ETH0_RXDV, ETH1_RXDV, ETH2_RXDV	Input	Input the receive data enable signal.
	ETH0_RXER, ETH1_RXER, ETH2_RXER	Input	Input the receive data error signal.
	ETH0_RXD0 to 3, ETH1_RXD0 to 3 ETH2_RXD0 to 3	Input	Input the receive data signal.
	ETH0_CRS, ETH1_CRS, ETH2_CRS	Input	Input the carrier sense signal.
	ETH0_COL, ETH1_COL, ETH2_COL	Input	Input the collision detection signal.
	ETH_MDC, MII2_MDC	Output	Output the management interface clock.
	ETH_MDIO, MII2_MDIO	I/O	Management data signal I/O pins
	PHYLINK0, PHYLINK1	Input	Input the PHY Link signal.
	ETHSWSECOUT	Output	Event output pin for Ethernet switch per second
	PHYRESETOUT#, PHYRESETOUT2#	Output	Output the PHY RESET signal (PHYRESETOUT#: for Ether0 and Ether1, PHYRESETOUT2#: for Ether2)
EtherCAT slave controller (ECATC) (optional)	CATLEDRUN	Output	Outputs the EtherCAT RUN LED signal.
	CATIRQ	Output	Outputs the EtherCAT IRQ signal.
	CATLEDSTER	Output	Outputs the EtherCAT Dual-color state LED signal.
	CATLEDERR	Output	Outputs the EtherCAT error LED signal.
	CATLINKACT0, CATLINKACT1	Output	Output the EtherCAT link/activity LED signal.
	CATSYNC0, CATSYNC1	Output	Output the EtherCAT SYNC signal.
	CATLATCH0, CATLATCH1	Input	Input the EtherCAT LATCH signal.
	CATI2CCLK	Output	Outputs the EtherCAT EEPROM I^2C clock signal.
	CATI2CDATA	I/O	Inputs/outputs the EtherCAT EEPROM I^2C data signal.

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10)

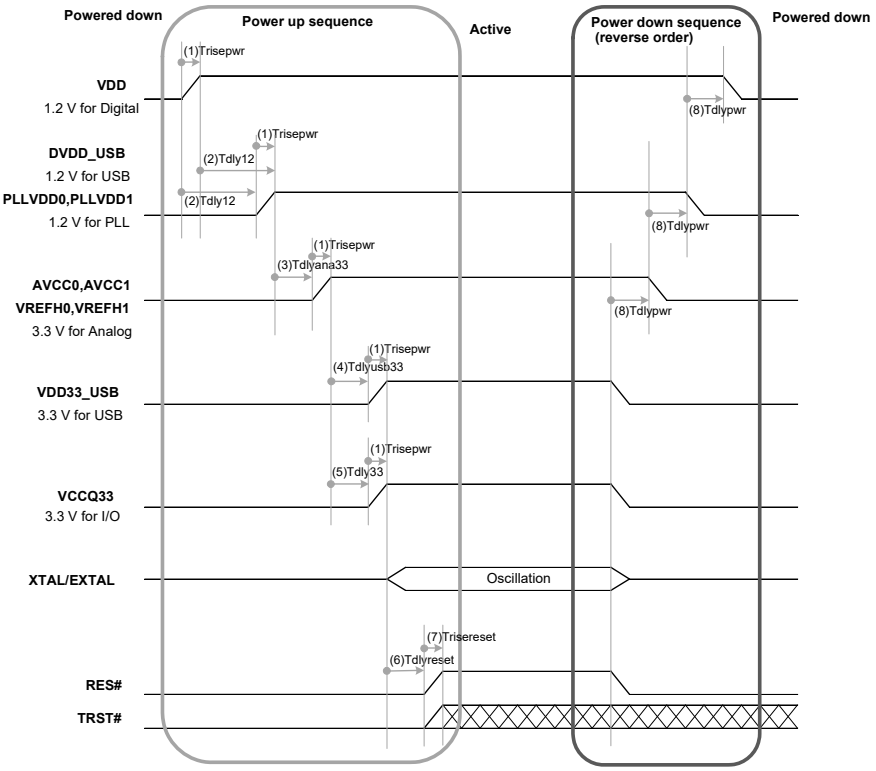
Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
N3	RSTOUT#							
N5	RES#							
N6	PLLVSS0							
N8	VDD							
N9	VSS							
N10	VDD							
N11	VDD							
N12	VDD							
N13	VDD							
N15	TRACEDATA2	PE2	D10	MTCLKC / TIOCB4	SSL02		IRQ2	
N16	TRACEDATA4	PE4	D12	MTIOC0B / TIOCC0	RTS1# / SSL00			
N18	TRACEDATA5	PE5	D13	MTIOC0C / TIOCC3	TXD1 / MOSI0			
N19		PT2		TIOCA1 / TIOCB1 / PO27				
N20		PT3		TIOCA0 / TIOCB0 / PO28	CTS2#	ENCIF09	IRQ11	
P1	VSS_USB							
P2	VDD33_USB							
P3	USB_RREF							
P5		P31			USB_VBUSEN			
P6	VCCQ33							
P15		P06	D6	MTIOC2B / TIOCB0				
P16		P07	D7	MTIOC2A / TIOCB1				
P18	TRACEDATA3	PE3	D11	MTIOC0D / TIOCB5	CTS1# / SSL01		IRQ3	
P19		PT0		TIOCA3 / TIOCB3 / PO25	SCK2	ENCIF07	IRQ0	
P20		PT1		TIOCA2 / TIOCB2 / PO26	RTS2#	ENCIF08		
R1	USB_DP							
R2	USB_DM							
R3		P30			CRXD0 / USB_VBUSIN			
R5		PN0		MTIOC8D	SSL10			
R6		PN2		MTIOC8B	MOSI1		IRQ10	
R7		PG0	A1	PO2				
R8		PG2	A3	PO4 / TOC0	RSPCK1			
R9		PG7	A8	PO9				
R10		PH2	A11	MTIOC2A / PO12				
R11		PH4	A13	PO14			IRQ4	
R12		PH6	A15	MTIOC7D	RTS0#			
R13		P23	A0 / DACK1	MTIC5U	TXD0			
R14		P27	A20	MTIOC8C / TIOCB0	RTS0#			
R15		P47	WE3#/ DQMUU/ AH#	MTIOC6C				

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
V12		P20	A17	MTCLKD				
V13		P21	CS0#	MTIC5V / TIOCB1	CTS0#		IRQ1	
V14	VSS							
V15		P45	CS2#					
V16		P46	CKE					
V17		PS2		MTIOC7C		SSIWS0		
V18		P05	D5	MTIOC3A				
V19		P01	D1	MTIC5W / TIOCA2				
V20		P02	D2	MTIC5V / TIOCA3				
W1		P62			SPBCLK			
W2		P65	DREQ0		SPBIO2			
W3		PN5		MTIOC6A / TIOCD9		ENCIF10	IRQ5	
W4		PN6		MTIOC3C / TIOCC9		MCLK3 / ENCIF11		
W5		PP0	TEND0	POE8#		MCLK2		
W6		PP2		MTIOC0C / TCLKH		MCLK1		
W7		PP4		MTIOC0A		MCLK0		
W8	TRACECTL	PP6		TIOCA11	RXD1	ENCIF06		
W9	TRACECLK	PP7	DACK1	TCLKF / TCLKH	SCK1			
W10	TRACEDATA1	PR1	TEND1	POE4#	CTS1#	ENCIF08	IRQ9	
W11	TRACEDATA3	PR3		TIOCA10 / TIOCB10		ENCIF01		
W12	TRACEDATA5	PR5		TIOCA8 / TIOCB8		ENCIF03		
W13		P24	RD/WR#		RXD0		IRQ12	
W14		P22	RD#	MTIOC7B / TIOCD0	SCK0		IRQ2	
W15		P44	WAIT#	TCLKD	CTS0#		IRQ12	ADTRG0
W16		P43	WE2#/ DQMUL	MTIOC8B	USB_VBUSEN			
W17		PS1		MTIOC7B		SSISCK0	IRQ1	
W18		PS3		MTIOC7A		SSIRXD0		
W19		PS4		MTIOC6D		SSITXD0		
W20		PS5		MTIOC6B				
Y1	VSS							
Y2		P67	TEND0	GTIOC3B	CTXD0 / USB_OVRCUR		IRQ15	
Y3		P66	DACK0	GTIOC3A	CTXD1 / USB_VBUSEN		IRQ14	
Y4		PN7	DREQ0	MTIOC3A / TIOCD6		MDAT3 / ENCIF12		
Y5		PP1	DACK0	MTIOC0D		MDAT2		
Y6		PP3		MTIOC0B / TCLKC		MDAT1		
Y7		PP5		PO22		MDAT0		
Y8	VSS							
Y9	TRACEDATA0	PR0	DREQ1	TCLKE / TCLKG	TXD1	ENCIF07		
Y10	TRACEDATA2	PR2		TIOCA11 / TIOCB11	RTS1#	ENCIF00		

2.2 Power On/Off Sequence

Turn on and off each power supply voltage according to the procedure shown in the figure below.
When turning on the power, be sure to fix TRST# pins and RES# pins to the low level. Otherwise, initialization is not performed successfully.



Timing

		Value		
No.	Item	min	typ	max
(1)	Trisepwr	100 µs	—	50 ms
(2)	Tdly12	0 ms	—	100 ms
(3)	Tdlyana33	0 ms		100 ms
(4)	Tdlyusb33	0 ms		100 ms
(5)	Tdly33	0 ms		100 ms
(6)	Tdlyreset	10 ms	—	—
(7)	Trisereset	—	—	150 µs
(8)	Tdlypwr	0 ms	—	—

Note 1. Turn on all power supply voltages and reset signals with a monotonic increase and turn off with a monotonic decrease.
Note 2. Do not apply a negative voltage to power supply voltages.
Note 3. Before turning on the power, be sure to make reset pins (TRST# and RES#) active (low). Otherwise, inputs and outputs on the pins may be unstable. If this may also be a problem when turning off the power, make reset pins (TRST# and RES#) active (low.)

Note: If the power on/off sequence is not met (out of operation guarantee range), the pin input state and output state may be undefined.

Figure 2.1 Power On/Off Sequence

Table 2.3 DC Characteristics (2) [Power Supply]

Item	Type		Symbol	typ	max	Unit	Test Conditions
Normal operation	VDD	600MHz	Vlcc	330	820	mA	Tj = -40 to 125 °C (R7S910018CBG, R7S910118CBG)
				273	752	mA	Tj = -40 to 125 °C (R7S910017CBG, R7S910117CBG)
				265	740	mA	Tj = -40 to 125°C (R7S910028CBG, R7S910128CBG)
				258	731	mA	Tj = -40 to 125 °C (R7S910013CBG, R7S910113CBG)
				209	673	mA	Tj = -40 to 125 °C (R7S910027CBG, R7S910127CBG)
				201	663	mA	Tj = -40 to 125 °C (R7S910007CBG, R7S910107CBG)
		450MHz		310	798	mA	Tj = -40 to 125 °C (R7S910016CBG, R7S910116CBG)
				253	730	mA	Tj = -40 to 125 °C (R7S910015CBG, R7S910115CBG)
				245	718	mA	Tj = -40 to 125 °C (R7S910026CBG, R7S910126CBG)
				238	709	mA	Tj = -40 to 125 °C (R7S910011CBG, R7S910111CBG)
				189	651	mA	Tj = -40 to 125 °C (R7S910025CBG, R7S910125CBG)
				181	641	mA	Tj = -40 to 125 °C (R7S910002CBG, R7S910006CBG, R7S910102CBG, R7S910106CBG)
				180	640	mA	Tj = -40 to 125 °C (R7S910001CFP, R7S910101CFP)
		300MHz		225	696	mA	Tj = -40 to 125 °C (R7S910036CBG, R7S910136CBG)
				169	629	mA	Tj = -40 to 125 °C (R7S910035CBG, R7S910135CBG)
				220	511	mA	Tj = -40 to 110 °C R7S9100022 R7S910023 R7S910122 R7S910123
	PLLVDD0 + PLLVDD1		PLLIcc	3.2	5	mA	
	VCCQ33		V33Icc	19*1, *2	—	mA	
	AVCC0		AV0Icc	2	5	mA	A/D conversion (unit 0)
	AVCC1		AV1Icc	0.7	1.5	mA	A/D conversion (unit 1)

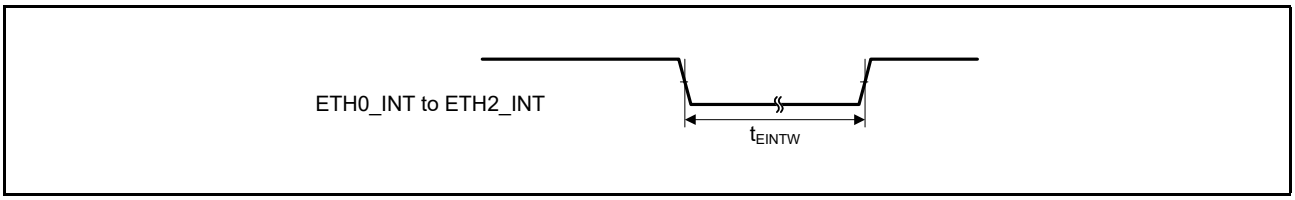
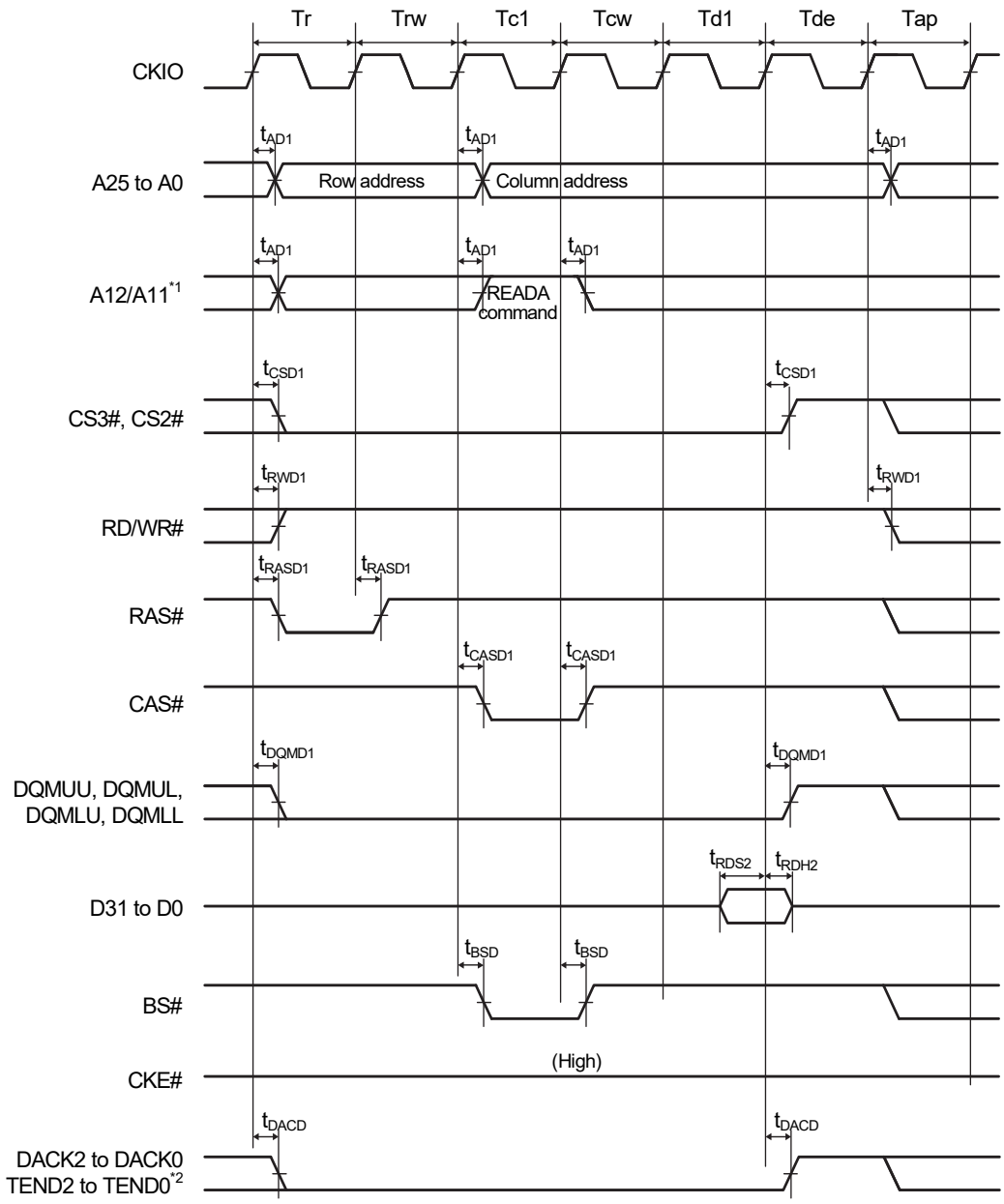
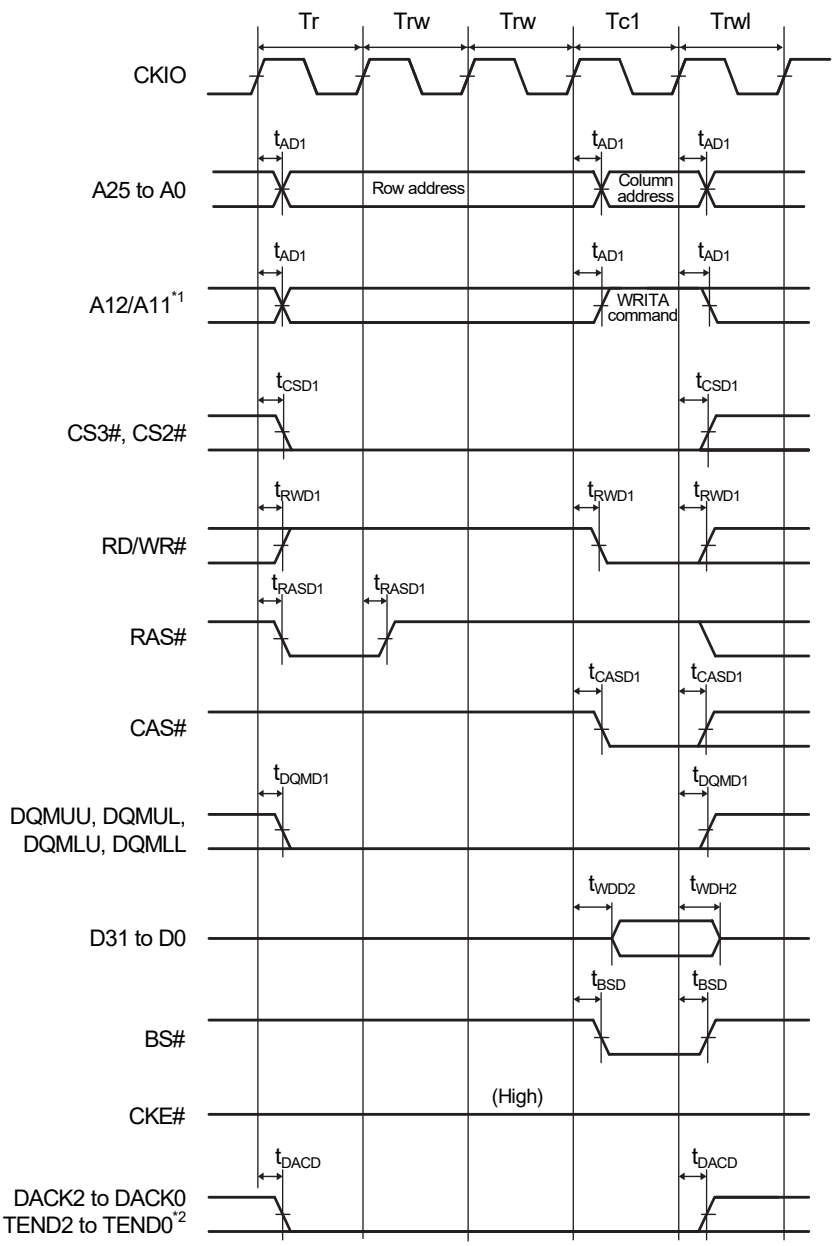


Figure 2.11 ETH_INT Interrupt Input Timing



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.21 Synchronous DRAM Single-Read Bus Cycle (with Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 1 Cycle)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.25 Synchronous DRAM Single-Write Bus Cycle (with Auto Precharge, WTRCD = 2 Cycles, TRWL = 1 Cycle)

2.4.5.3 CMTW Timing

Table 2.21 CMTW Timing

Item			Symbol	min	max	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PDcyc}	Figure 2.42
		Both-edge setting		2.5	—		

Note 1. t_{PDcyc}: PCLKD cycle

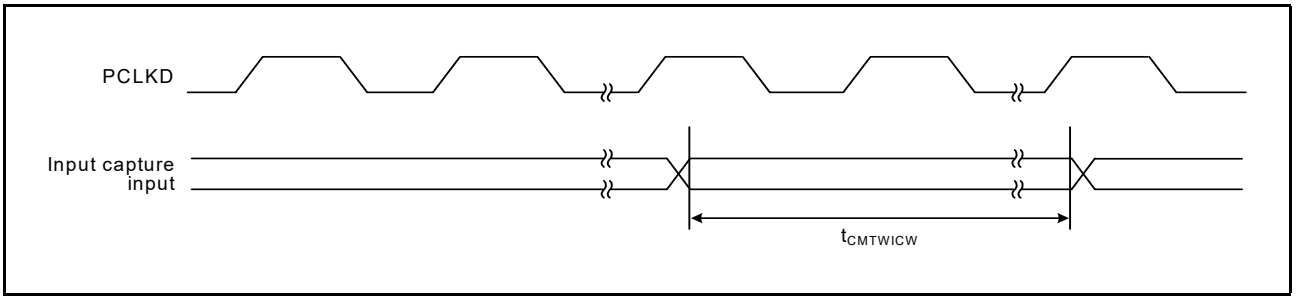


Figure 2.42 CMTW Input Capture Input Timing

2.4.5.4 MTU3a Timing

Table 2.22 MTU3a Timing

Item			Symbol	min	max	Unit*1	Test Conditions
MTU3a	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PCcyc}	Figure 2.43
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PCcyc}	Figure 2.44
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PCcyc}: PCLKC cycle

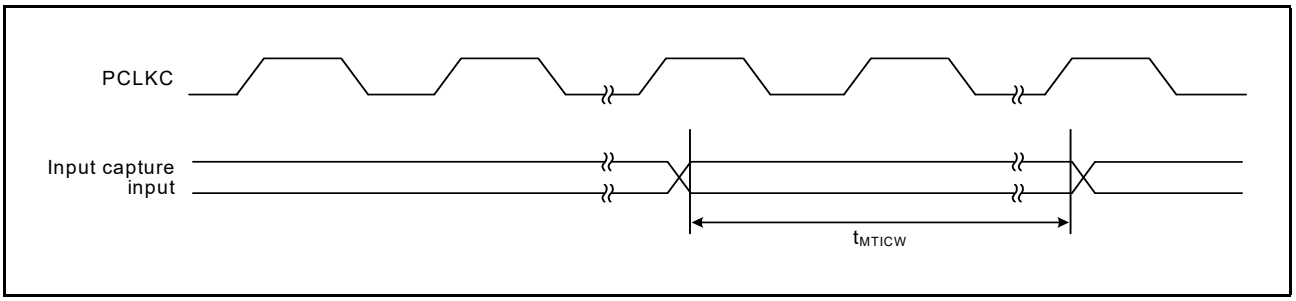


Figure 2.43 MTU3a Input Capture Input Timing

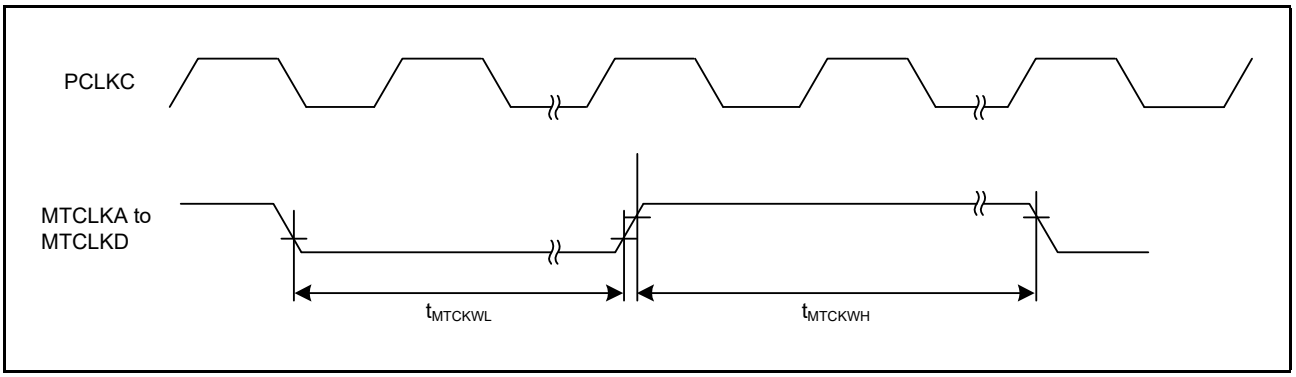


Figure 2.44 MTU3a Clock Input Timing

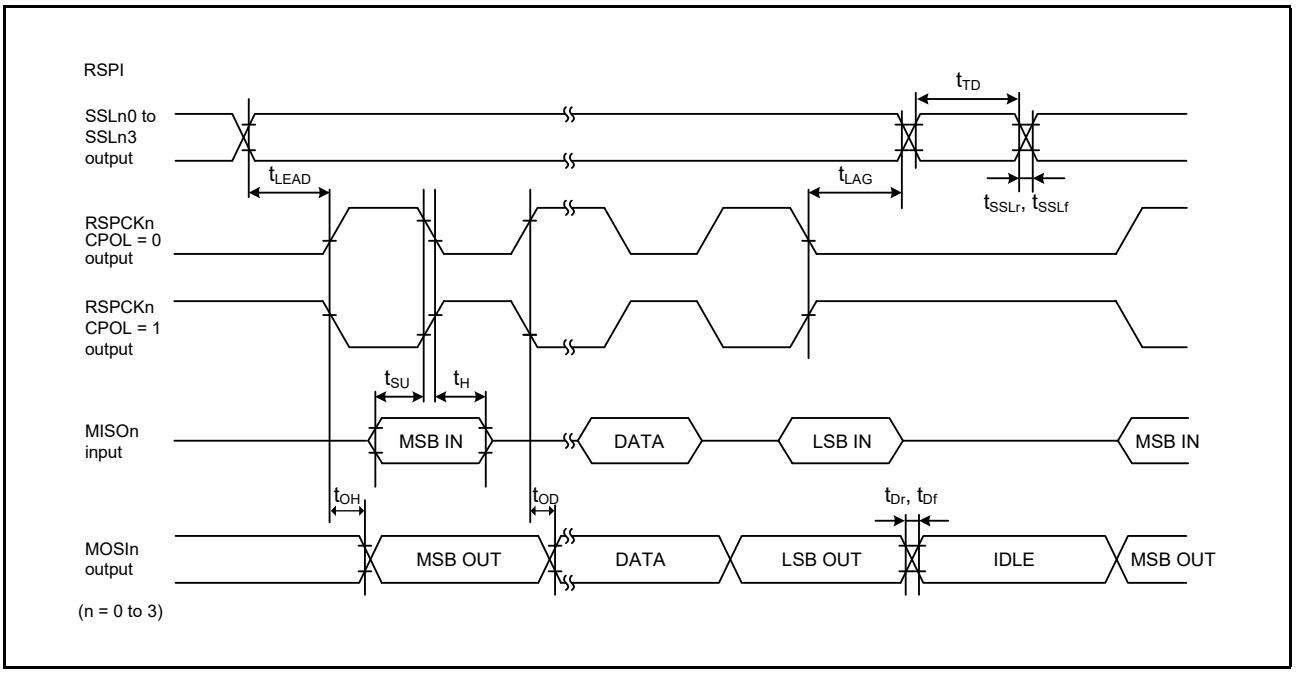


Figure 2.54 RSPIa Timing (Master, CPHA = 1)

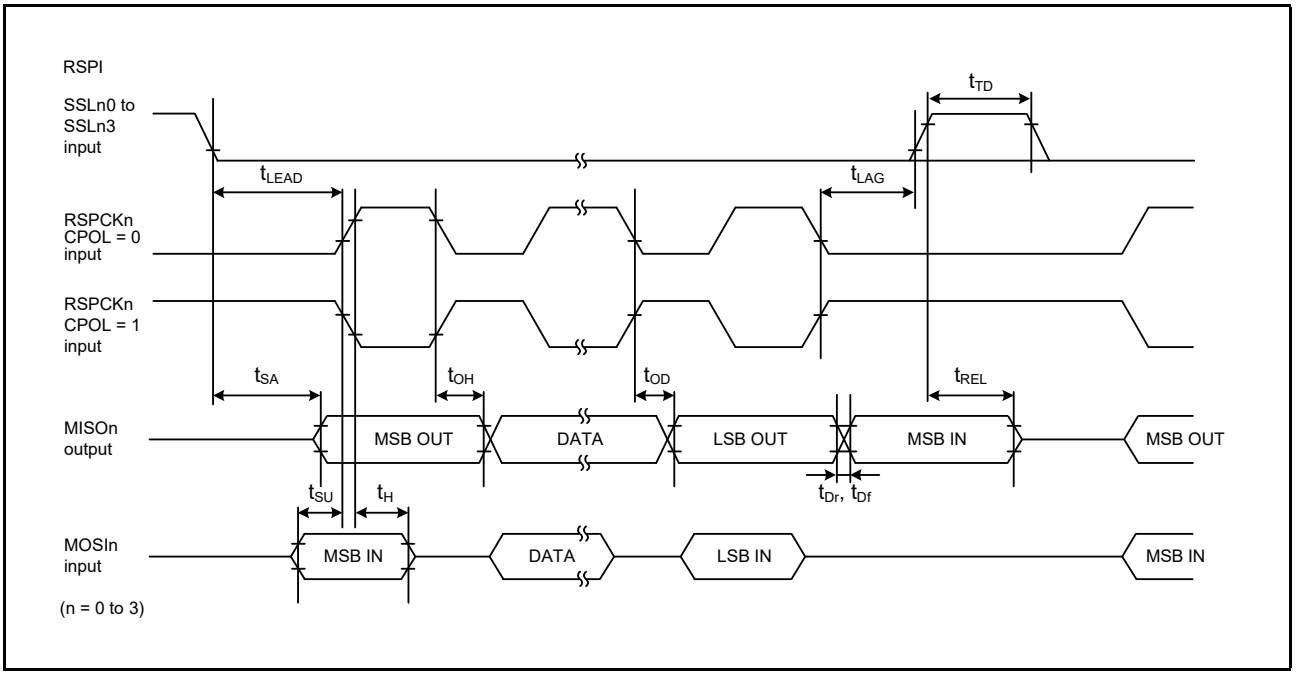


Figure 2.55 RSPI Timing (Slave, CPHA = 0)

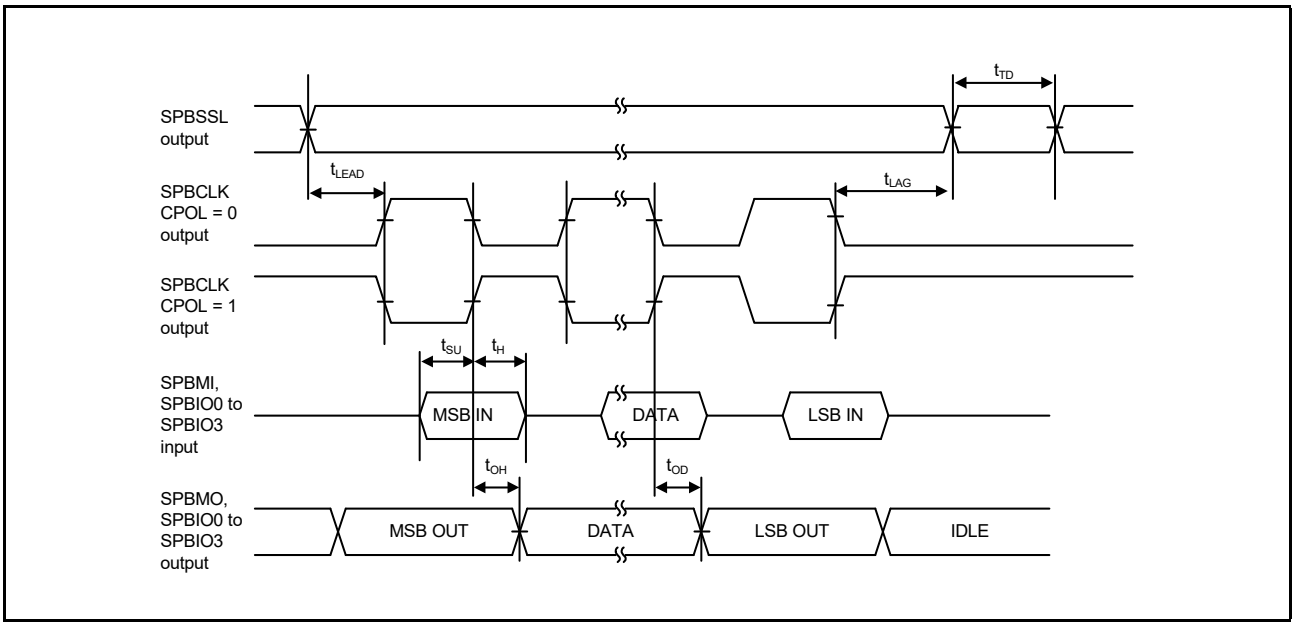


Figure 2.60 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1)

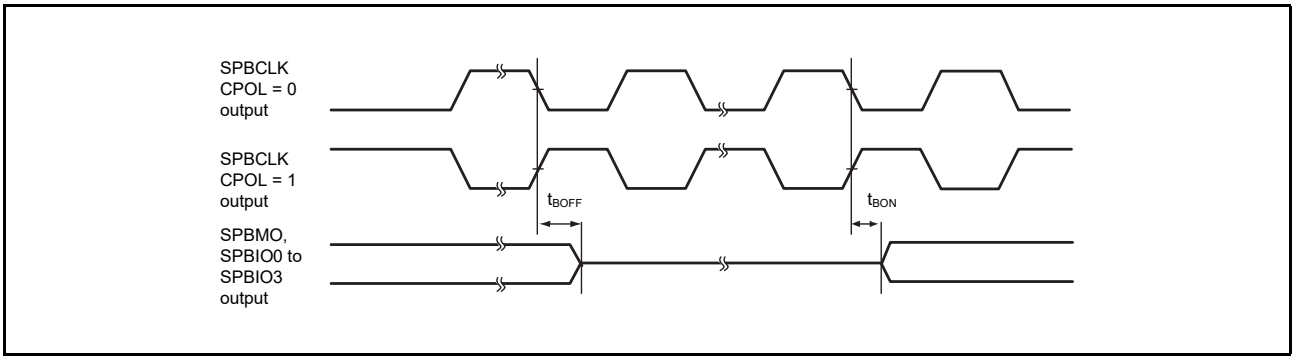


Figure 2.61 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 0)

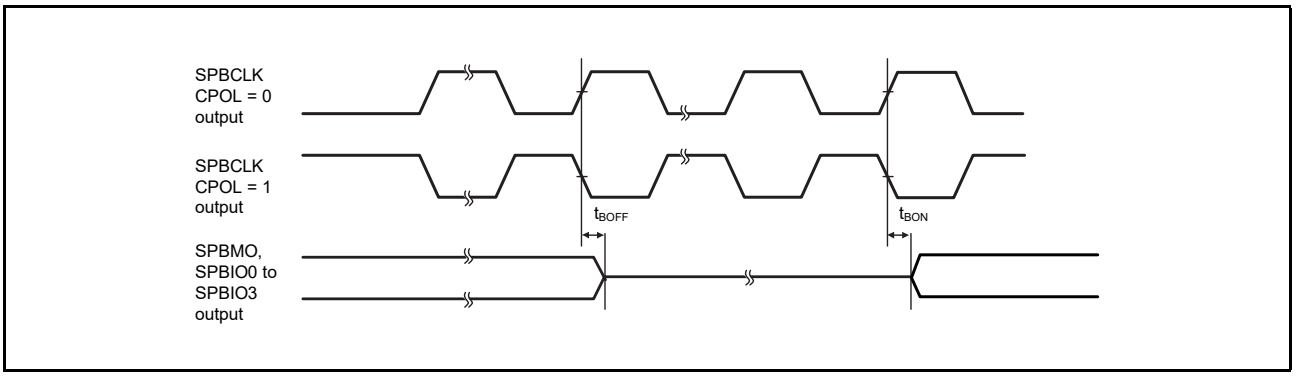


Figure 2.62 SPIBSC Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)

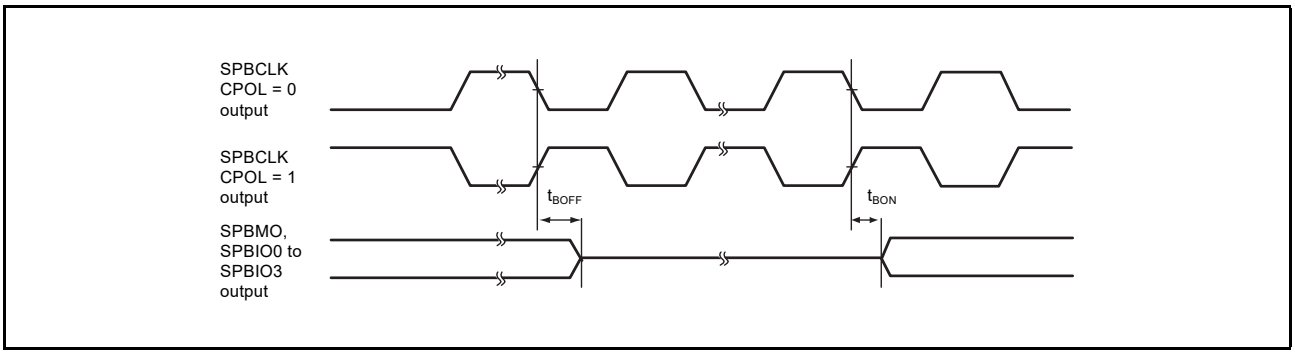


Figure 2.63 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 1)

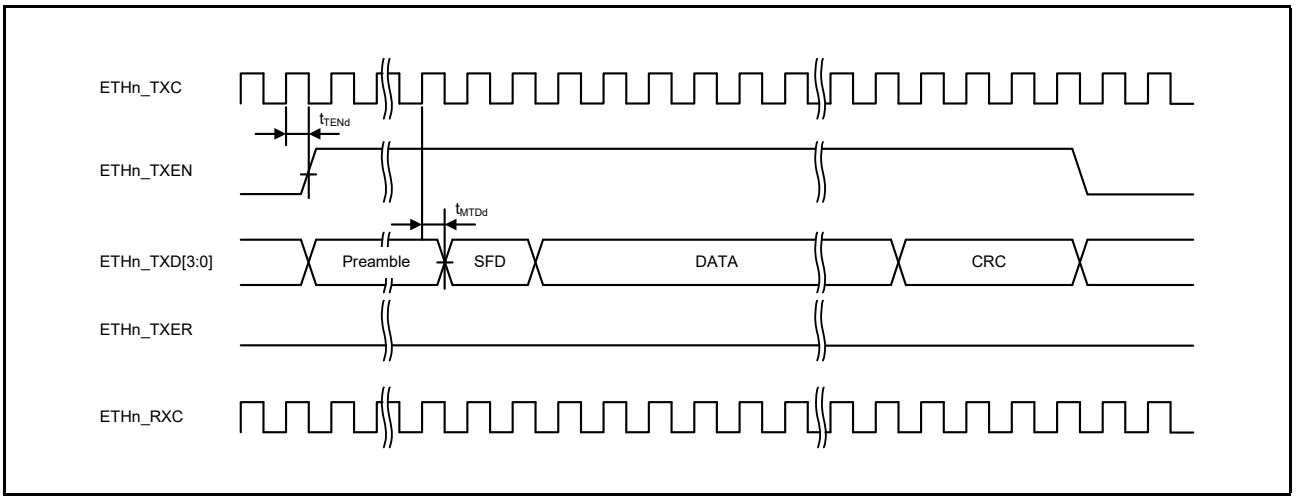


Figure 2.74 MII Transmission Timing

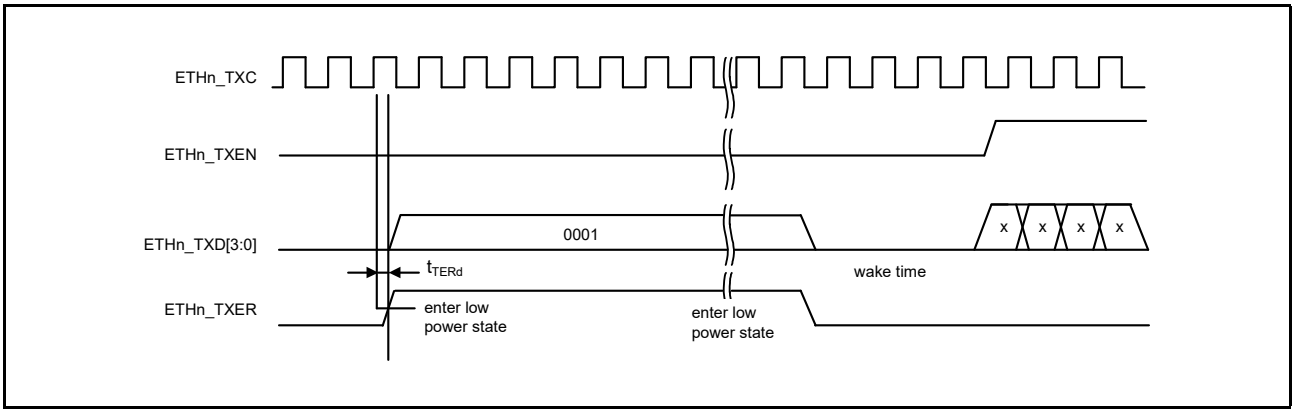


Figure 2.75 MII Transmission Timing

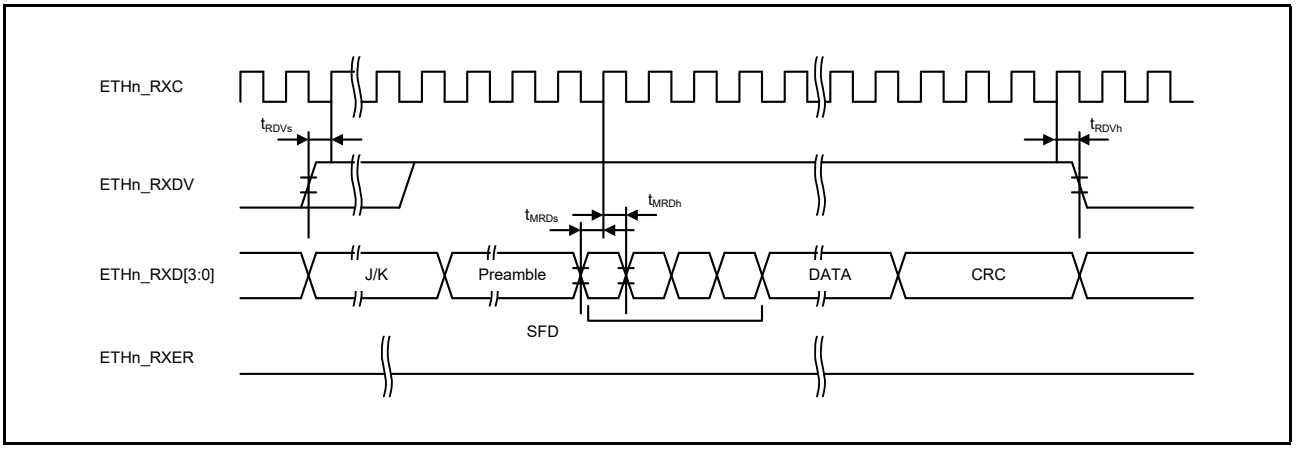


Figure 2.76 MII Reception Timing (Normal Operation)

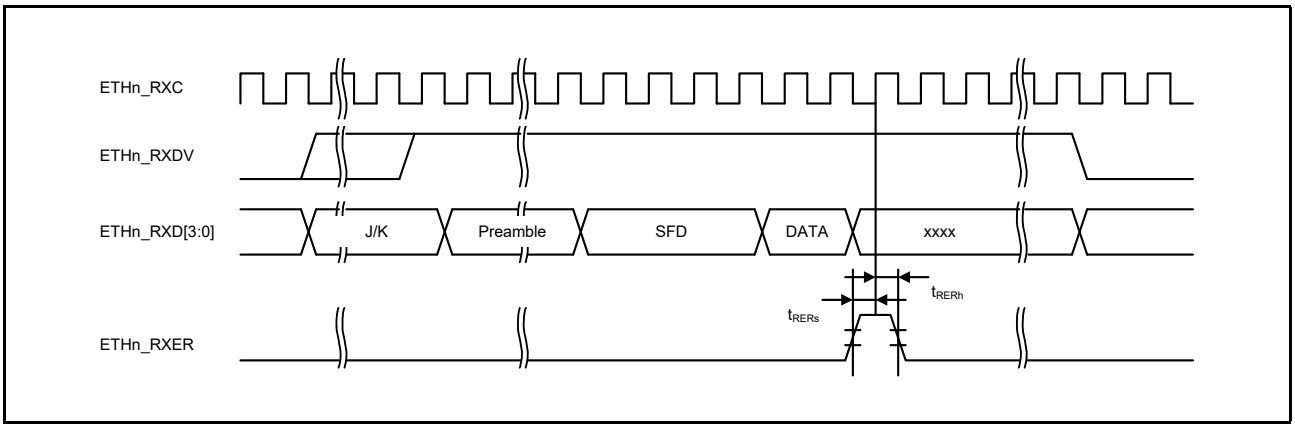


Figure 2.77 MII Reception Timing (Error Occurrence)

2.4.5.15 Serial Management Interface Timing

(1) Timing

Table 2.33 Serial Management Interface

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min	max	Unit	Test Conditions
MDIO	ETHn_MDC output cycle	t_{MDC}	80	—	ns	Figure 2.78
	ETHn_MDIO input setting time (to ETHn_MDC↑)	t_{SMDIO}	10	—	ns	
	ETHn_MDIO input hold time (to ETHn_MDC↑)	t_{HMDIO}	0	—	ns	
	ETHn_MDIO output delay time (to ETHn_MDC↓)	t_{DMDIO}	—	20	ns	

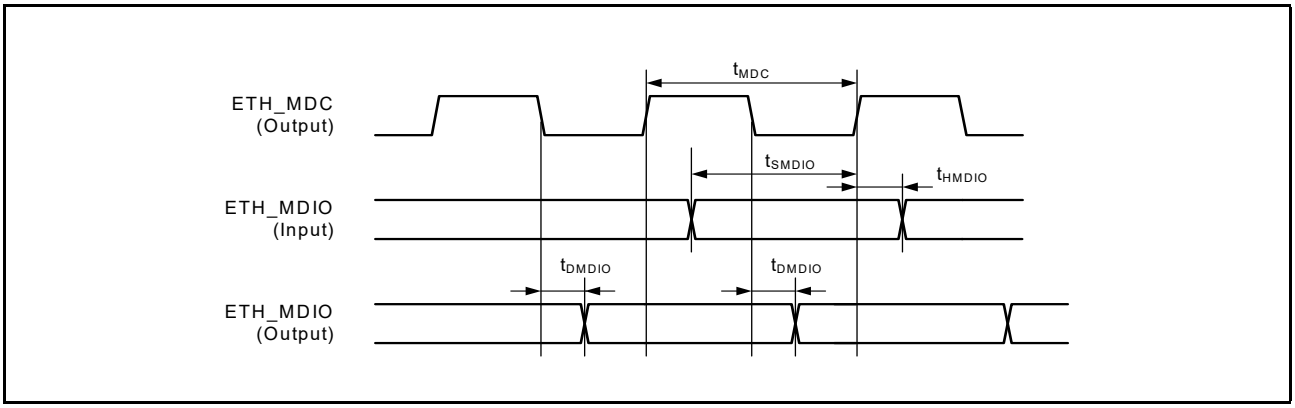


Figure 2.78 Serial Management Access Timing

2.7 Temperature Sensor Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 2.39 Temperature Sensor Characteristics

Item	min	typ	max	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (at 25°C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	µs	
Sampling time	4.25	—	—	µs	ADSSTRT.SST[7:0] = 255 states (when PCLKF [ADC (unit0) sampling CLK] = 60 MHz)

2.8 Oscillation Stop Detection Timing

Table 2.40 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	min	typ	max	Unit	Test Conditions
Clock switching time	t_{dr}	—	—	1	ms	Figure 2.86

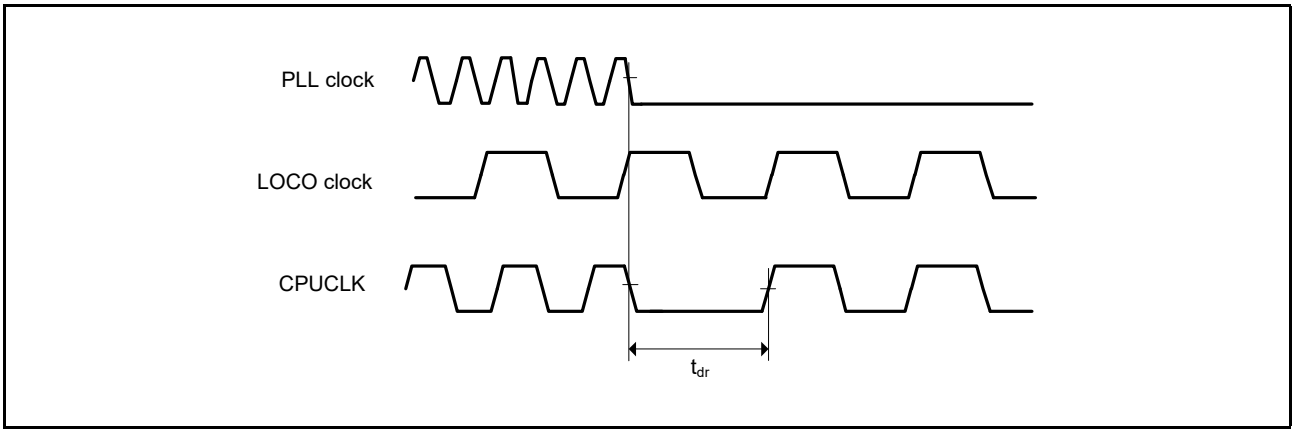


Figure 2.86 Oscillation Stop Detection Timing