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Details

Product Status	Active
Core Processor	ARM® Cortex®-R4F
Core Size	32-Bit Single-Core
Speed	600MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I ² C, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	209
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	320-FBGA
Supplier Device Package	320-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910013cbg-ac0

Table 1.4 Pin Functions (5 / 7)

Classifications	Pin Name	I/O	Description
Ethernet controller (ETHERC)	ETH0_TXC, ETH1_TXC, ETH2_TXC	Input	Input the 10 M/100 M transmission clock (2.5 MHz/25 MHz).
	ETH0_TXEN, ETH1_TXEN, ETH2_TXEN	Output	Output the transmission enable signal.
	ETH0_TXER, ETH1_TXER, ETH2_TXER	Output	Output the transmission error signal.
	ETH0_TXD0 to 3, ETH1_TXD0 to 3, ETH2_TXD0 to 3	Output	Output the transmission data signal.
	ETH0_RXC, ETH1_RXC, ETH2_RXC	I/O	Receive clock I/O pins
	ETH0_RXDV, ETH1_RXDV, ETH2_RXDV	Input	Input the receive data enable signal.
	ETH0_RXER, ETH1_RXER, ETH2_RXER	Input	Input the receive data error signal.
	ETH0_RXD0 to 3, ETH1_RXD0 to 3, ETH2_RXD0 to 3	Input	Input the receive data signal.
	ETH0_CRS, ETH1_CRS, ETH2_CRS	Input	Input the carrier sense signal.
	ETH0_COL, ETH1_COL, ETH2_COL	Input	Input the collision detection signal.
	ETH_MDC, MII2_MDC	Output	Output the management interface clock.
	ETH_MDIO, MII2_MDIO	I/O	Management data signal I/O pins
	PHYLINK0, PHYLINK1	Input	Input the PHY Link signal.
	ETHSWSECOUT	Output	Event output pin for Ethernet switch per second
	PHYRESETOUT#, PHYRESETOUT2#	Output	Output the PHY RESET signal (PHYRESETOUT#: for Ether0 and Ether1, PHYRESETOUT2#: for Ether2)
EtherCAT slave controller (ECATC) (optional)	CATLEDRUN	Output	Outputs the EtherCAT RUN LED signal.
	CATIRQ	Output	Outputs the EtherCAT IRQ signal.
	CATLEDSTER	Output	Outputs the EtherCAT Dual-color state LED signal.
	CATLEDERR	Output	Outputs the EtherCAT error LED signal.
	CATLINKACT0, CATLINKACT1	Output	Output the EtherCAT link/activity LED signal.
	CATSYNC0, CATSYNC1	Output	Output the EtherCAT SYNC signal.
	CATLATCH0, CATLATCH1	Input	Input the EtherCAT LATCH signal.
	CATI2CCLK	Output	Outputs the EtherCAT EEPROM I ² C clock signal.
	CATI2CDATA	I/O	Inputs/outputs the EtherCAT EEPROM I ² C data signal.

Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8)

Pin Number	Pin Name
R8	PG2 / A3 / PO4 / TOC0 / RSPCK1
R9	PG7 / A8 / PO9
R10	PH2 / A11 / MTIOC2A / PO12
R11	PH4 / IRQ4 / A13 / PO14
R12	PH6 / A15 / MTIOC7D / RTS0#
R13	P23 / A0 / MTIC5U / TXD0 / DACK1
R14	P27 / A20 / MTIOC8C / TIOCB0 / RTS0#
R15	P47 / WE3#/DQMUU/AH# / MTIOC6C
R16	VCCQ33
R18	VCCQ33
R19	PS6 / IRQ14 / TIOCA5 / TIOCB5 / PO23 / RXD2 / ENCIF06
R20	PS7 / TIOCA4 / TIOCB4 / PO24 / TXD2
T1	DVDD_USB
T2	VDD33_USB
T3	P32 / IRQ10 / USB_OVRCUR
T5	PC6 / TCLKC / SCL1 / CRXD0 / DREQ0 / USB_VBUSIN
T6	P37 / WE1#/DQMLU / PO1
T7	P36 / WE0#/DQMLL / PO0
T8	PG3 / A4 / PO5 / TIC1 / MISO1
T9	PG6 / A7 / TCLKB / PO8 / SSL11
T10	PH3 / A12 / MTIOC1B / PO13
T11	VCCQ33
T12	PH5 / A14 / PO15
T13	VCCQ33
T14	P26 / A19 / MTIOC8D / DREQ1
T15	VCCQ33
T16	VSS
T18	VSS
T19	PE0 / D8 / MTIOC1B / TIOCB2 / TRACEDATA0
T20	PE1 / D9 / MTCLKD / TIOCB3 / SSL03 / TRACEDATA1
U1	P60 / SPBSSL / CTXD0 / TEND0
U2	P63 / SPBMO/SPBIO0
U3	PN1 / MTIOC8C / PO21 / MISO1 / ENCIF09
U18	P00 / D0 / MTIOC6A / TIOCA1 / ADTRG1 / TRACECTL
U19	P04 / D4 / MTIOC3C / TIOCA5
U20	P03 / D3 / MTIC5U / TIOCA4
V1	P61 / SPBIO3 / CTXD1 / DACK0
V2	P64 / SPBBI/SPBIO1
V3	PN3 / MTIOC8A / RSPCK1
V4	PN4 / IRQ12 / MTIOC6C / TIOCC6 / SSL11
V5	PC7 / TIC0 / SDA1 / CRXD1
V6	PG1 / A2 / PO3
V7	PG4 / A5 / PO6 / TOC1 / MOSI1
V8	PG5 / A6 / TCLKA / PO7 / SSL10
V9	PH0 / A9 / PO10

Table 1.6 Pin Assignments (176-Pin HLQFP) (2 / 4)

Pin Number	Pin Name
45	VSS
46	P63 / SPBMO/SPBIO0
47	P64 / SPBMO/SPBIO1
48	P65 / SPBIO2 / DREQ0
49	VSS
50	VDD
51	P36 / WE0#/DQMLL / PO0
52	P37 / WE1#/DQMLU / PO1
53	PG0 / A1 / PO2
54	PG1 / A2 / PO3
55	VCCQ33
56	PG2 / A3 / PO4 / TOC0 / RSPCK1
57	PG3 / A4 / PO5 / TIC1 / MISO1
58	PG4 / A5 / PO6 / TOC1 / MOSI1
59	PG5 / A6 / TCLKA / PO7 / SSL10
60	PG6 / A7 / TCLKB / PO8 / SSL11
61	PG7 / A8 / PO9
62	PH0 / A9 / PO10
63	PH1 / A10 / MTIOC2B / PO11
64	PH2 / A11 / MTIOC2A / PO12
65	PH3 / A12 / MTIOC1B / PO13
66	VDD
67	VSS
68	PH4 / IRQ4 / A13 / PO14
69	PH5 / A14 / PO15
70	PH6 / A15 / MTIOC7D / RTS0#
71	PH7 / A16 / MTIC5W
72	P24 / IRQ12 / RD/WR# / RXD0
73	P21 / IRQ1 / CS0# / MTIC5V / TIOCB1 / CTS0#
74	P22 / IRQ2 / RD# / MTIOC7B / TIOCD0 / SCK0
75	P23 / A0 / MTIC5U / TXD0 / DACK1
76	P20 / A17 / MTCLKD
77	P25 / A18 / MTCLKC / TEND1
78	P26 / A19 / MTIOC8D / DREQ1
79	P27 / A20 / MTIOC8C / TIOCB0 / RTS0#
80	VDD
81	VSS
82	P42 / MTIOC7C / RXD0
83	P40 / MTIOC8A / TXD0
84	P43 / WE2#/DQMUL / MTIOC8B / USB_VBUSEN
85	P47 / WE3#/DQMUU/AH# / MTIOC6C
86	VCCQ33
87	P10 / IRQ0 / CKIO / TIOCA0 / TRACECLK
88	VSS
89	P00 / D0 / MTIOC6A / TIOCA1 / TRACECTL

Table 1.6 Pin Assignments (176-Pin HLQFP) (4 / 4)

Pin Number	Pin Name
135	VCCQ33
136	VREFH0
137	VREFL0
138	AVSS0
139	AVCC0
140	AN000
141	AN001
142	AN002
143	AN003
144	AN004
145	AN005
146	AN006
147	AN007
148	VDD
149	VSS
150	P51 / IRQ1 / PHYLINK1 / RSPCK2
151	P54 / CLKOUT25M1 / MOSI2
152	P56 / BS# / ETH1_TXER
153	PD5 / A21 / ETH1_TXD3 / ETH0_TXD0 / TIC0 / SSL20 / MCLK3
154	PD6 / A22 / ETH1_TXD2 / ETH0_TXD1 / TIC1 / MISO2 / MCLK2
155	PD7 / ETH1_TXD1 / MTIOC4D / GTIOC2B / TOC0
156	P86 / ETH1_TXD0 / MTIOC4B / GTIOC2A / TOC1 / RSPCK2
157	P87 / A23 / ETH1_TXC / ETH0_RXD0 / MTIOC4C / GTIOC1B / MCLK1
158	PF5 / ETH1_TXEN / MTIOC4A / GTIOC1A / TIC2
159	VCCQ33
160	VDD
161	VSS
162	PF6 / ETH1_RXD0 / MTIOC3D / GTIOC0B / TOC2
163	PB7 / ETH1_RXD1 / MTIOC3B / GTIOC0A / TOC3
164	PC0 / WAIT# / ETH1_RXD2 / GTETRQ / SCL1 / MDAT3
165	PC1 / IRQ9 / ETH1_RXD3 / PHYLINK0 / SDA1 / MDAT2
166	PB0 / ETH1_RXDV / MTCLKB / TCLKD / TIC3
167	PB1 / ETH1_RXER / MTCLKA / TCLKC / CTS4#
168	PB2 / ETH1_RXC / ETH0_RXD1 / MTIOC1A / SSL30 / MDAT1
169	VCCQ33
170	PB3 / IRQ3 / CS1# / ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1 / MCLK0
171	PB4 / A24 / ETH1_COL / ETH0_RXER / RXD3 / MOSI3 / MDAT0
172	PB5 / ETH_MDIO / TCLKB / POE0# / POE10# / CTS3# / RSPCK3
173	VSS
174	VDD
175	PB6 / ETH_MDC / TCLKA / SCK3 / RTS4# / MISO3
176	PC2 / ETH0_TXC / ETH1_RXD2 / SDA0

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10)

Pin Number	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIIa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
C15								AN000
C16	VREFL0							
C17	VREFH0							
C18		PD2	WAIT#					AN110
C19		P14	CAS#	MTIOC4A / GTIOC1A		ENCIF10		
C20		P13	RAS#	MTIOC4C / GTIOC1B				
D1		P81		TIOCC0	ETH0_RXER / CTS4#			
D2		P80		TIOCC3	ETH0_RXDV / RTS4#		IRQ8	
D3		PU3		TIOCD6	ETH2_COL / TXD3			
D18		PD0	CS4#					AN108
D19		P96		POE0# / POE10#		ENCIF09		AN106
D20		P95		MTCLKA	CTS2#		IRQ13	AN105
E1		P84			ETH0_COL / CATLINKACT1 / RXD4			
E2		P82		TIOCD3	ETH0_TXEN / ETH1_CRS / SCK4 / RTS3# / USB_OVRCUR			
E3		PU1		TIOCA11	ETH2_RXC / SCK3			
E5		PU0		TIOCA10	ETH2_RXER			
E6		PL6		TIOCA9	ETH2_RXD3			
E7		PL4			ETH2_RXD1		IRQ4	
E8		PL2		TIOCA6	ETH2_TXEN			ADTRG1
E9		PL0		TIOCB9	ETH2_TXD0			
E10		PK7		TIOCB7	ETH2_TXD2			
E11		PK6		TIOCB6	ETH2_TXD3			
E12		PD5	A21	TIC0	ETH1_TXD3 / ETH0_TXD0 / SSL20	MCLK3		AN113
E13		P56	BS#		ETH1_TXER			
E14		PD4			ETH2_INT			AN112
E15	VCCQ33							
E16		PD1	CS1#					AN109
E18		P97	A25				IRQ7	ADTRG1 / AN107
E19		P94		MTCLKB	RTS2#	ENCIF08	IRQ4	AN104
E20		P93		MTIOC1A / TIC3	SCK2	ENCIF07		AN103
F1		PC4		TCLKH	CAT12CCLK / SCL0			
F2		P83			ETH0_CRS / CATLINKACT0 / TXD4		IRQ11	

Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP) (2 / 6)

Pin Number	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF) Interrupt S12ADCa
36	USB_DM					
37	USB_DP					
38	VDD33_USB					
39	DVDD_USB					
40		P30			CRXD0 / USB_VBUSIN	
41		P60	TEND0		CTXD0 / SPBSSL	
42		P61	DACK0		CTXD1 / SPBIO3	
43	VCCQ33					
44		P62			SPBCLK	
45	VSS					
46		P63			SPBMO/SPBIO0	
47		P64			SPBMO/SPBIO1	
48		P65	DREQ0		SPBIO2	
49	VSS					
50	VDD					
51		P36	WE0#/DQMLL	PO0		
52		P37	WE1#/DQMLU	PO1		
53		PG0	A1	PO2		
54		PG1	A2	PO3		
55	VCCQ33					
56		PG2	A3	PO4 / TOC0	RSPCK1	
57		PG3	A4	PO5 / TIC1	MISO1	
58		PG4	A5	PO6 / TOC1	MOSI1	
59		PG5	A6	TCLKA / PO7	SSL10	
60		PG6	A7	TCLKB / PO8	SSL11	
61		PG7	A8	PO9		
62		PH0	A9	PO10		
63		PH1	A10	MTIOC2B / PO11		
64		PH2	A11	MTIOC2A / PO12		
65		PH3	A12	MTIOC1B / PO13		
66	VDD					
67	VSS					
68		PH4	A13	PO14		IRQ4
69		PH5	A14	PO15		
70		PH6	A15	MTIOC7D	RTS0#	
71		PH7	A16	MTIC5W		
72		P24	RD/WR#		RXD0	IRQ12
73		P21	CS0#	MTIC5V / TIOC7B	CTS0#	IRQ1
74		P22	RD#	MTIOC7B / TIOC7D	SCK0	IRQ2

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V

Item	Symbol	Value	Unit
Power supply voltage (I/O)	VCCQ33	−0.3 to +4.2	V
Power supply voltage (internal)	VDD	−0.3 to +1.6	V
PLL power supply voltage	PLLVD0, PLLVD1	−0.3 to +1.6	V
Input voltage (except for ports for 5-V tolerant*1)	V _{in1}	−0.3 to VCCQ33 + 0.3*5	V
Input voltage (ports for 5-V tolerant*1)	V _{in2}	−0.3 to +5.5*3	V
Analog power supply voltage	AVCC0, AVCC1*2	−0.3 to +4.2	V
Reference power supply voltage	VREFH0, VREFH1	−0.3 to (AVCC0, AVCC1) + 0.3*5	V
USB digital power supply voltage	DVDD_USB	−0.3 to +1.6	V
USB power supply voltage	VDD33_USB*2	−0.3 to +4.2	V
Analog input voltage	V _{AN}	−0.3 to (AVCC0, AVCC1) + 0.3*5	V
Operating temperature (junction temperature)	T _j *4	−40 to +125	°C
Storage temperature	T _{stg}	−55 to +125	°C

[Usage Notes]

- Do not directly connect output pins (I/O pins in output state) of IC products to other output pins (including I/O pins in output state), power pins, or GND pins. However, output pins are directly connectable in an external circuit where timing design is provided to avoid conflict of outputs of high-impedance pins such as I/O pins.
- If even a single item exceeds the absolute maximum rating for even a moment, it may degrade the product's quality. In other words, the absolute maximum rating is a rated value that potentially causes physical damage to products. Use products with a margin of the absolute maximum rating.
Specified values and conditions shown in DC characteristics and AC characteristics are the range of normal operation and quality assurance of products.

Note 1. Ports PC0 to PC7 and P30 are 5-V tolerant.

Note 2. When the A/D converter unit 0 is not to be used, connect the AVCC0 and VREFH0 pins to VCCQ33 and the AVSS0 and VREFL0 pins to VSS, respectively. Do not leave these pins open. In the same way, when the A/D converter unit 1 is not to be used, connect the AVCC1 and VREFH1 pins to VCCQ33 and the AVSS1 and VREFL1 pins to VSS, respectively. Do not leave these pins open. When the USB is not to be used, connect the VDD33_USB pin to VCCQ33, the VSS_USB pin to VSS, and the DVDD_USB pin to VDD, respectively. Do not leave these pins open.

Note 3. When VCCQ33 is less than 3.0 V, the rated value of ports for 5-V tolerant is 3.6 V.

Note 4. For operations at the temperatures over 110°C (junction temperature), refer to the RZ/T1 Group Application Note: Precautions for High-Temperature Operations (R01AN3116).

Note 5. Do not exceed the absolute maximum rating, 4.2 V.

Table 2.5 DC Characteristics (4) [USB2.0 USB_RREF Pin]

Item	Symbol	min	typ	max	Unit	Test Conditions
Reference resistor	R_{REF}	$200\Omega \pm 1\%$				

Table 2.6 DC Characteristics (5) [USB2.0 Host/Function-Related Pins (Items for Both Full Speed and High Speed)*1]

Item	Symbol	min	typ	max	Unit	Test Conditions
DP pull-up resistor (when the function controller operation is selected)	R_{PU}	0.900	—	1.575	k Ω	Idle
		1.425	—	3.090	k Ω	Transmission/ reception
DP/DM pull-down resistors (when the host function is selected)	R_{PD}	14.25	—	24.80	k Ω	

Note 1. USB_DP and USB_DM pins

Table 2.7 DC Characteristics (6) [USB2.0 Host/Function-Related Pins (Full Speed)*1]

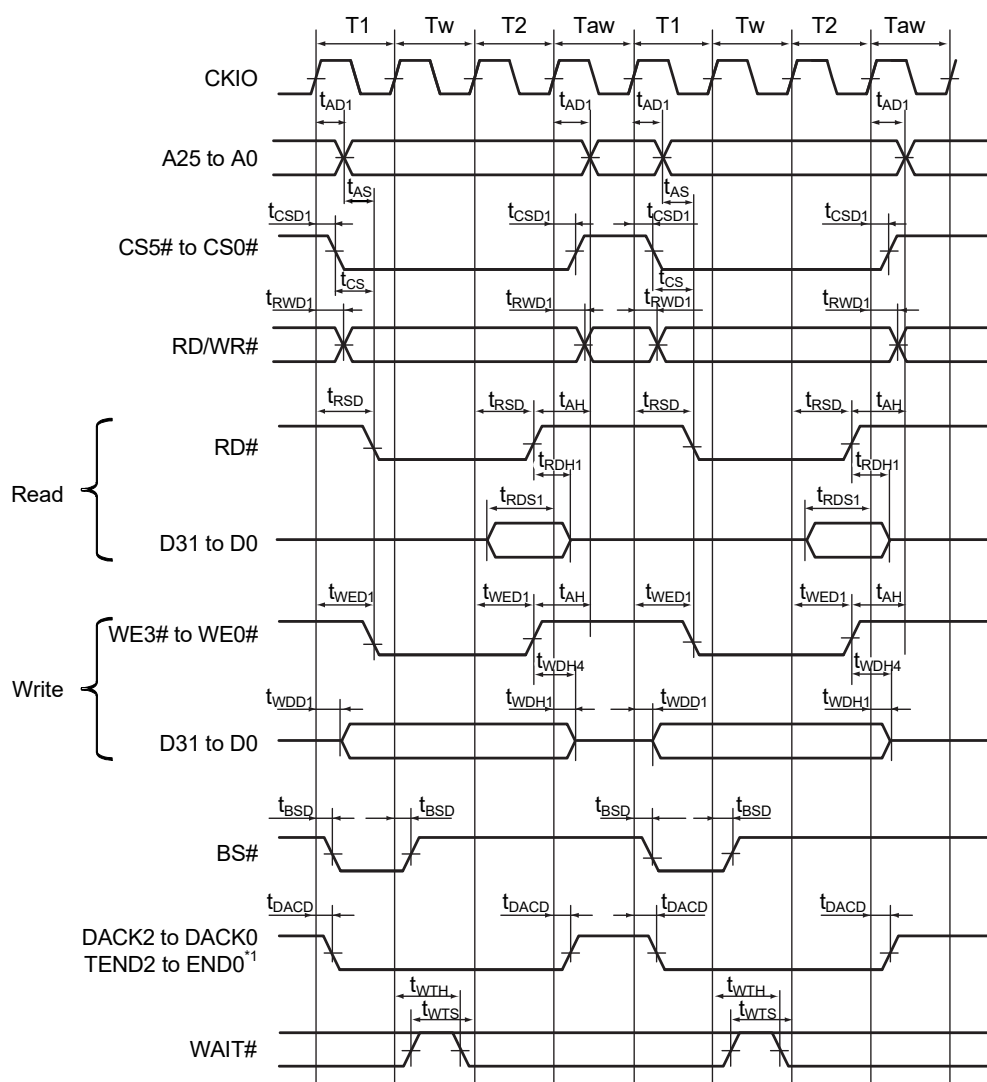
Item	Symbol	min	typ	max	Unit	Measuring Condition
Input high level voltage	V_{FSIH}	2.0	—	—	V	
Input low level voltage	V_{FSIL}	—	—	0.8	V	
Differential input sensitivity	V_{FSDI}	0.2	—	—	V	(USB_DP) – (USB_DM)
Differential common mode range	V_{FSCM}	0.8	—	2.5	V	
Output high level voltage	V_{FSOH}	2.8	—	3.6	V	$I_{FSOH} = -200\mu A$
Output low level voltage	V_{FSOL}	0.0	—	0.3	V	$I_{FSOL} = 2\text{ mA}$
Output signal crossover voltage	V_{FSCRS}	1.3	—	2.0	V	CL = 50 pF (full-speed)

Note 1. USB_DP and USB_DM pins

Table 2.8 DC Characteristics (7) [USB2.0 Host/Function-Related Pins (High Speed)*1]

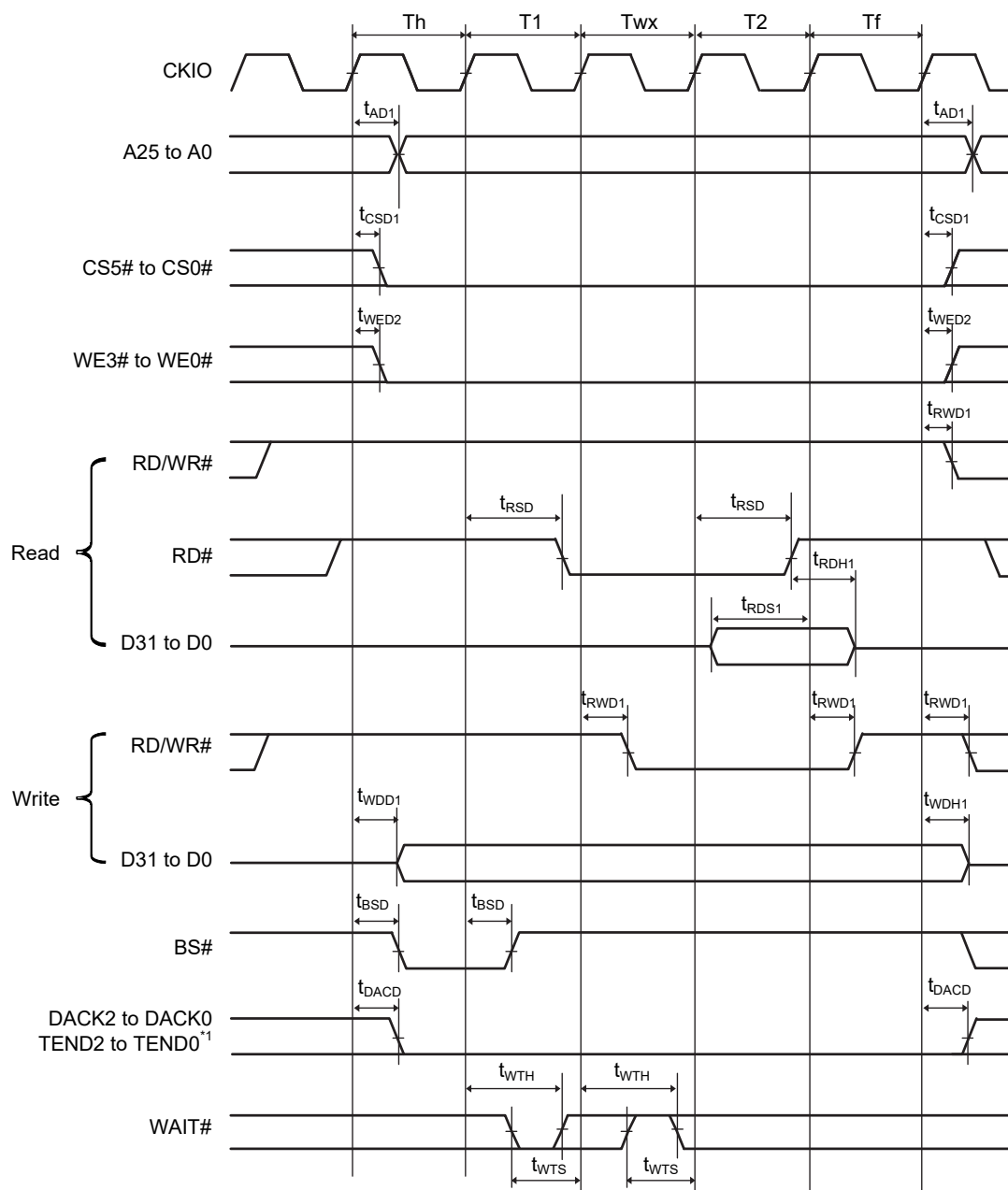
Item	Symbol	min	typ	max	Unit	Test Conditions
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	100	—	150	mV	
Common mode voltage range	V_{HSCM}	-50	—	500	mV	
Idle state	V_{HSOI}	-10.0	—	10.0	mV	
Output high level voltage	V_{HSOH}	360	—	440	mV	
Output low level voltage	V_{HSOL}	-10.0	—	10.0	mV	
Chirp J output voltage (differential)	V_{CHIRPJ}	700	—	1100	mV	
Chirp K output voltage (differential)	V_{CHIRPK}	-900	—	-500	mV	

Note 1. USB_DP and USB_DM pins



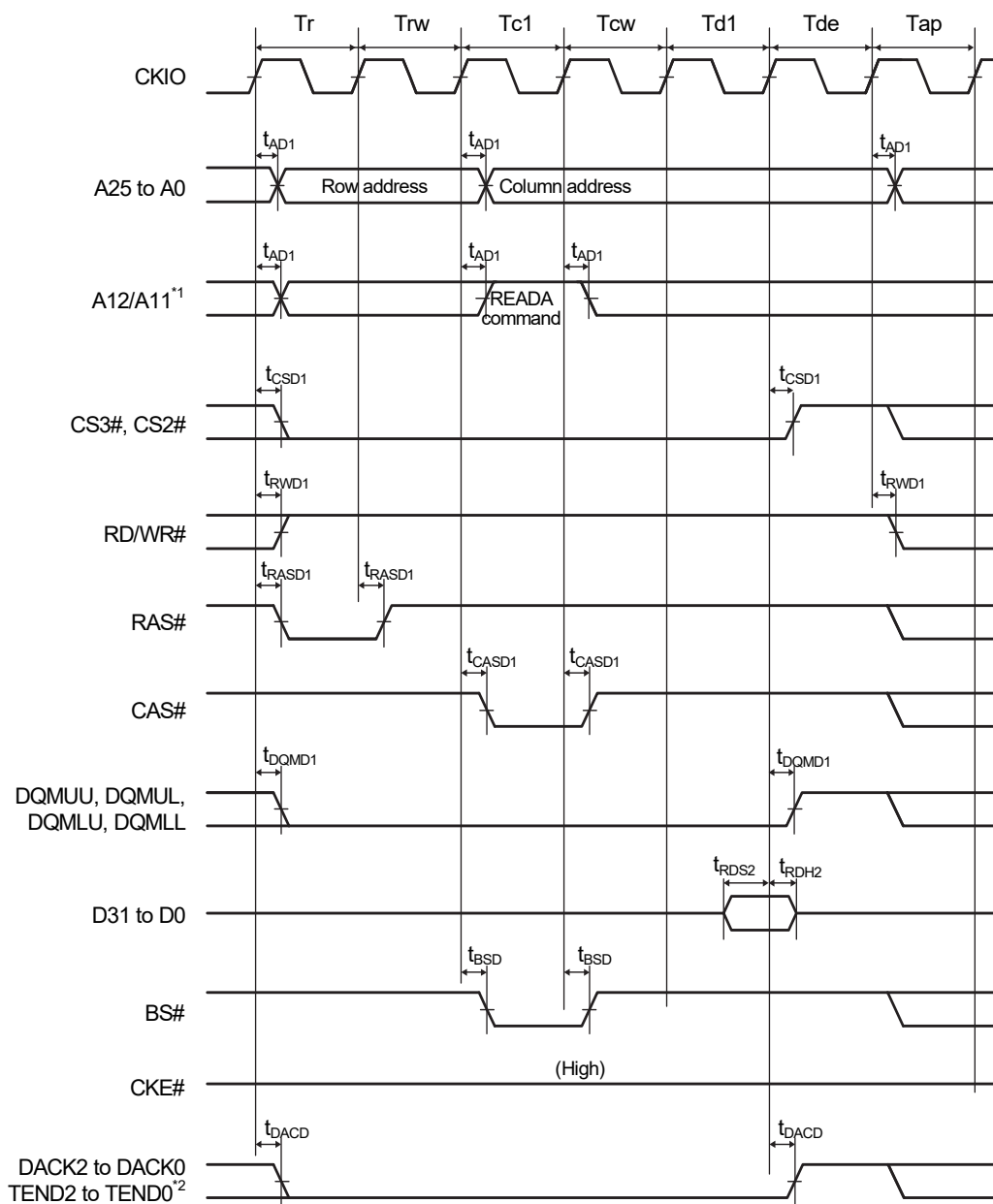
Note 1. DACKn and TENDn are waveforms when "active low" is specified.

Figure 2.15 SRAM Interface Basic Bus Cycle (Software Wait 1, External wait Enabled (WM Bit = 0), No Idle Cycle)



Note 1. DACKn and TENDn are waveforms when "active low" is specified.

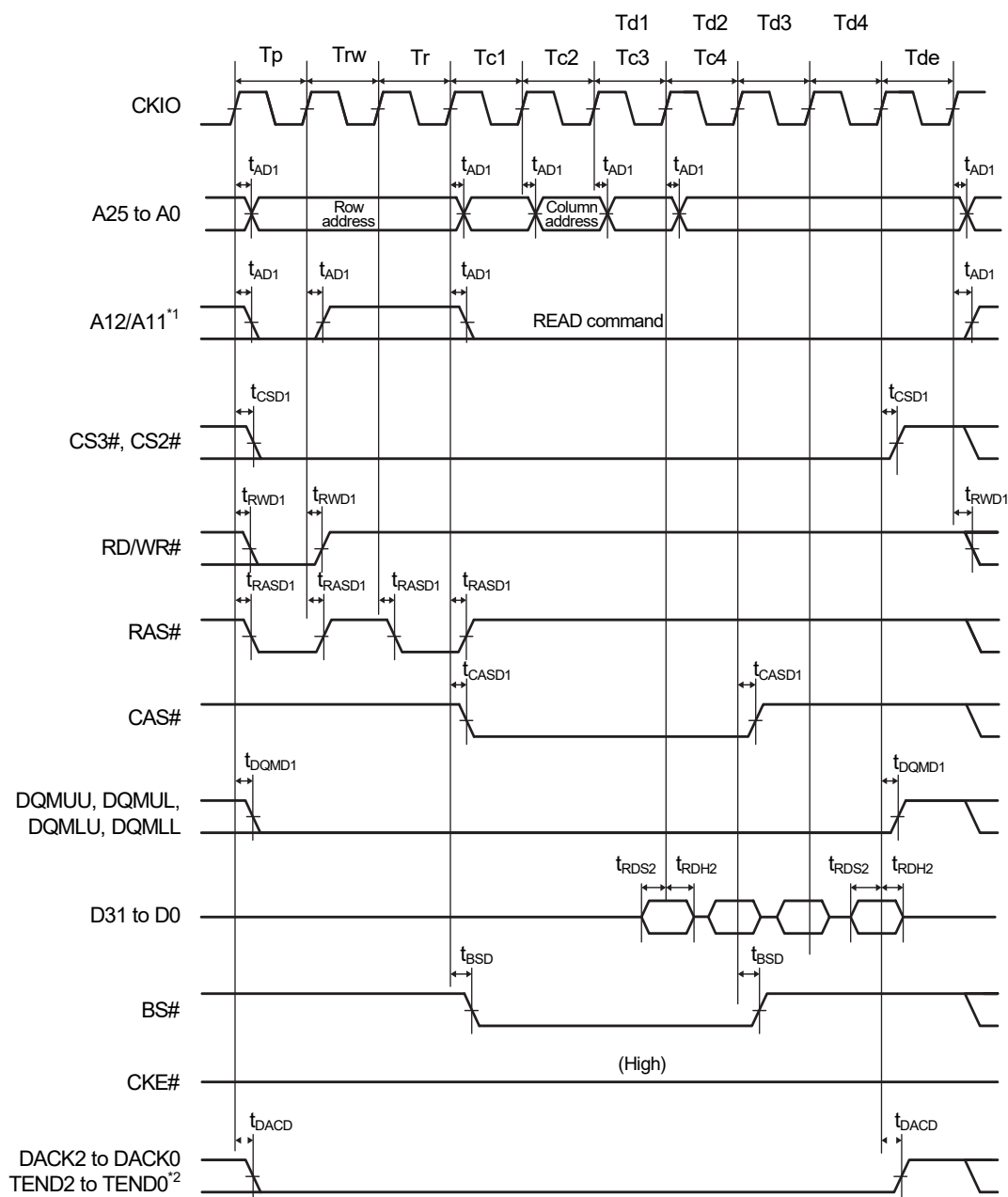
Figure 2.18 SRAM Bus Cycle with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1 Inserted, BAS = 1 (Write Cycle WE Control))



Note 1. Address pin to be connected to A10 of SDRAM

Note 2. DACKn and TENDn are waveforms when "active low" is specified.

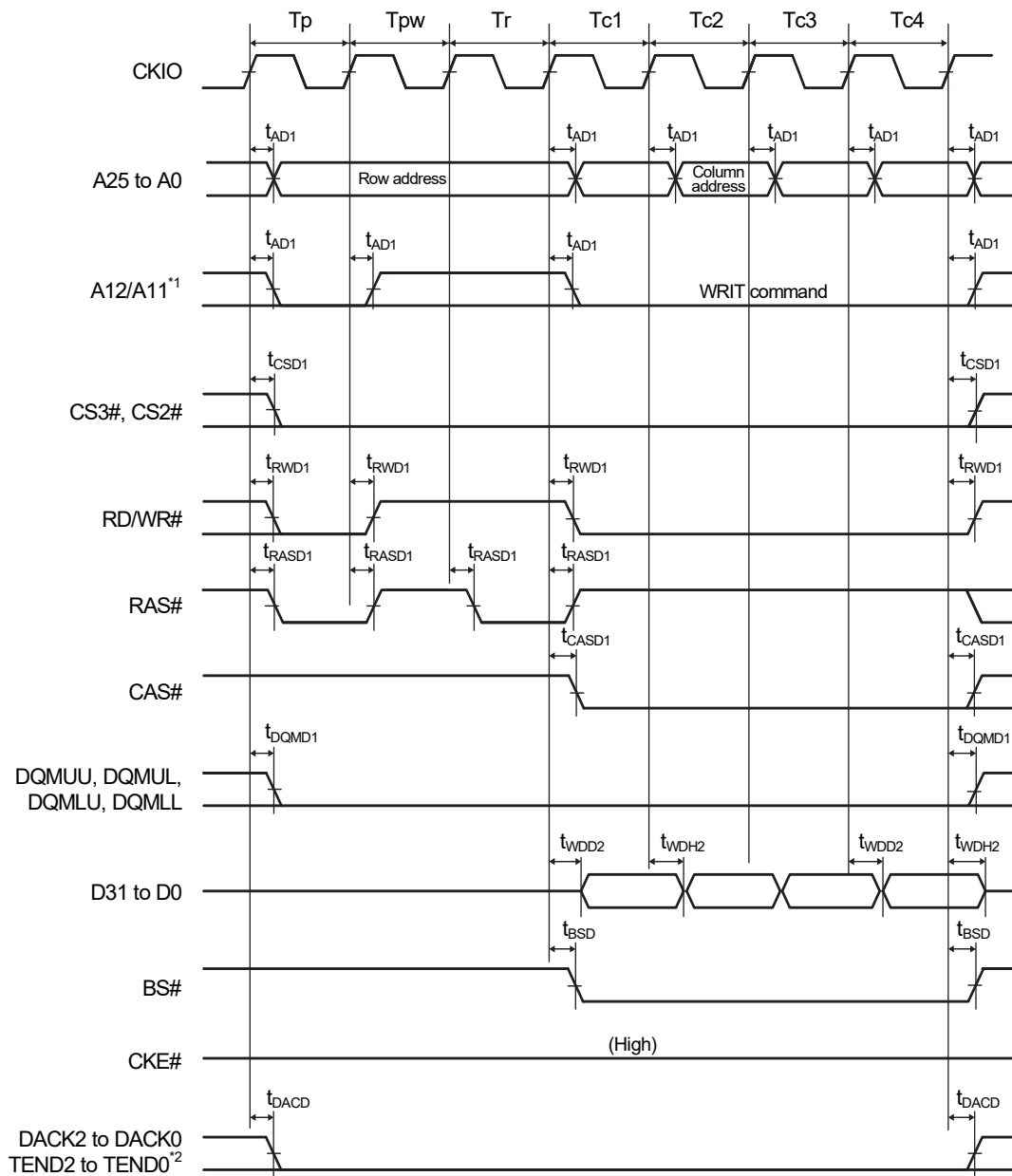
Figure 2.21 Synchronous DRAM Single-Read Bus Cycle (with Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 1 Cycle)



Note 1. Address pin to be connected to A10 of SDRAM

Note 2. DACKn and TENDn are waveforms when "active low" is specified.

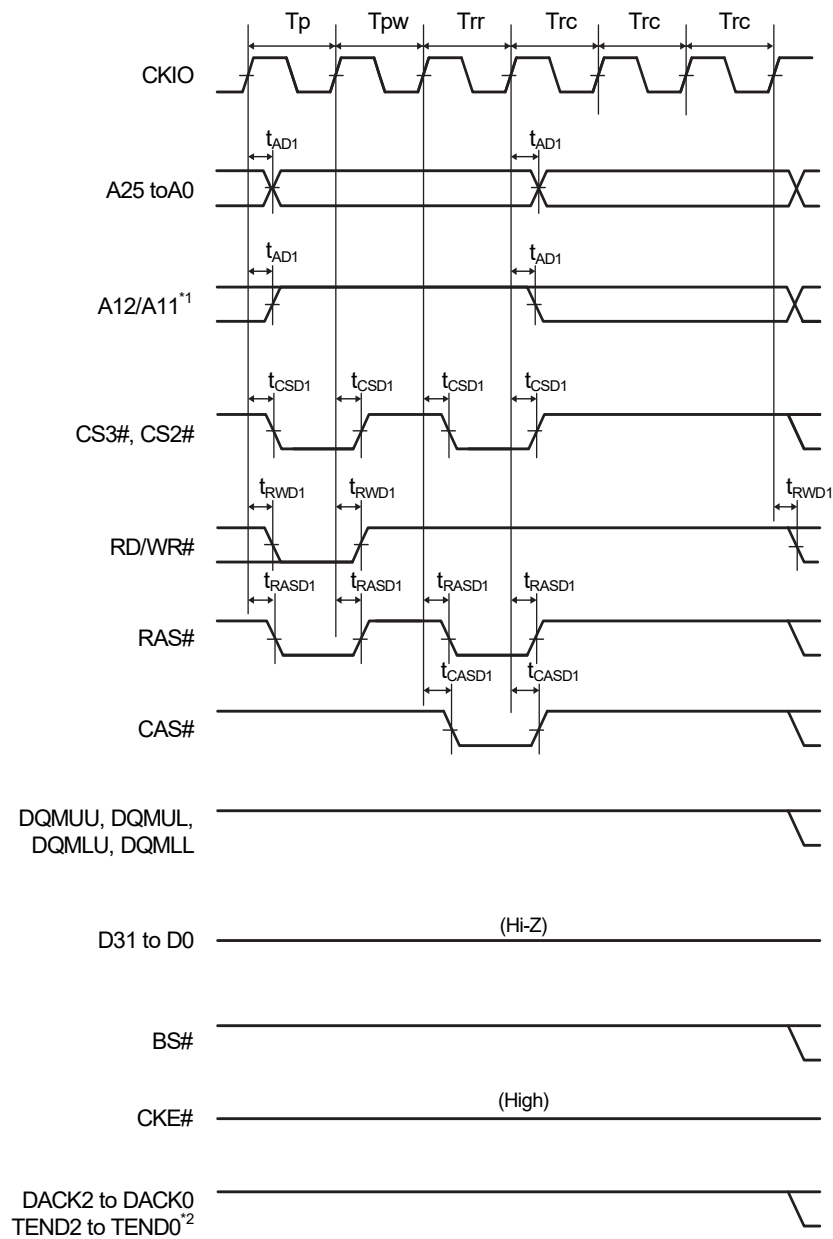
Figure 2.30 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: PRE + ACT + READ Command, Different Row Address, CAS Latency 2, WTRCD = 0 Cycles)



Note 1. Address pin to be connected to A10 of SDRAM

Note 2. DACKn and TENDn are waveforms when "active low" is specified.

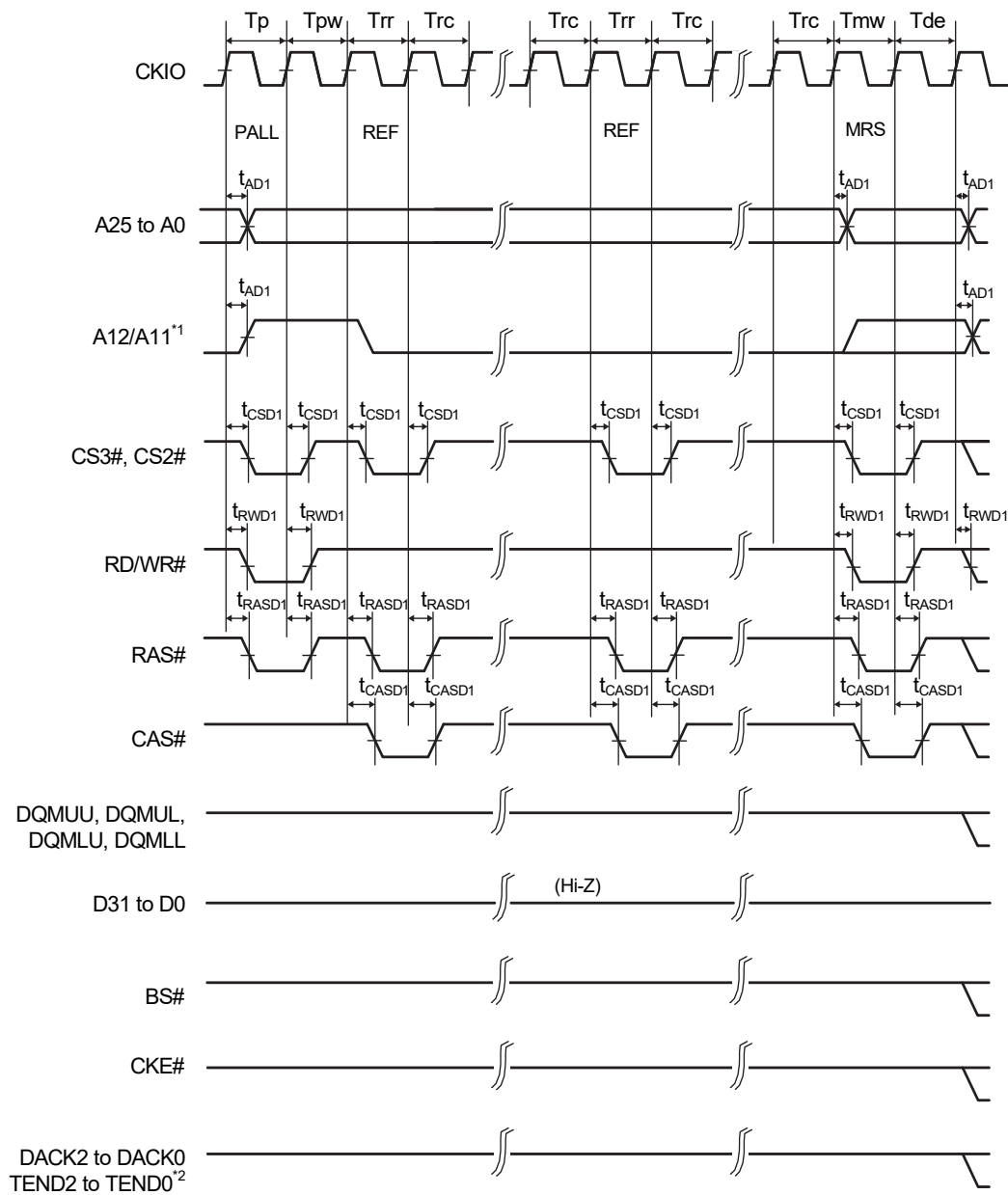
Figure 2.33 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (Bank Active Mode: PRE + ACT + WRITE Command, Different Row Address, WTRCD = 0 Cycles, TRWL = 0 Cycles)



Note 1. Address pin to be connected to A10 of SDRAM

Note 2. DACKn and TENDn are waveforms when "active low" is specified.

Figure 2.34 Synchronous DRAM Auto-Refresh Timing (WTRP = 1 Cycle, WTRC = 3 Cycles)



Note 1. Address pin to be connected to A10 of SDRAM

Note 2. DACKn and TENDn are waveforms when "active low" is specified.

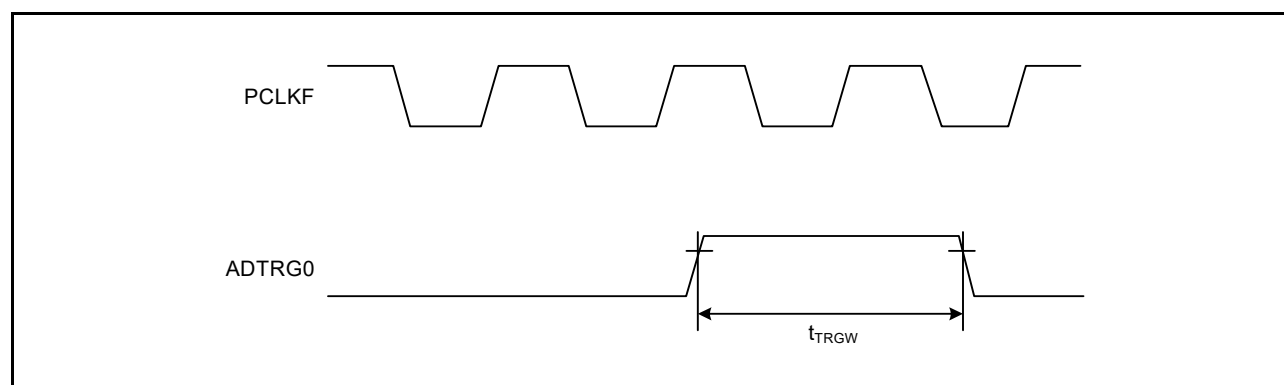
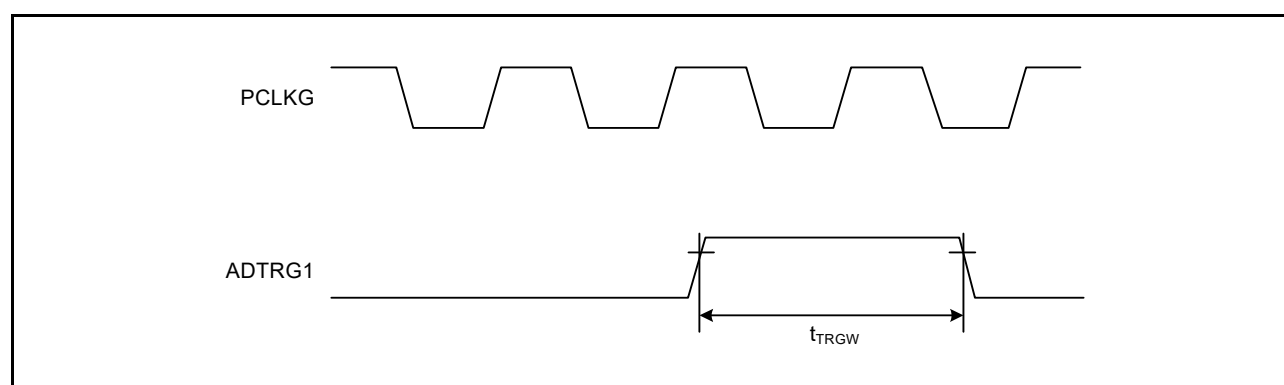
Figure 2.36 Synchronous DRAM Mode Register Write Timing (WTRP = 1 Cycle)

2.4.5.7 A/D Converter Trigger Timing

Table 2.25 A/D Converter Trigger Timing

Item		Symbol	min	max	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	ADTRG0	t_{TRGW}	1.5	—	t_{PFcyc} Figure 2.48
		ADTRG1	t_{TRGW}	1.5	—	t_{PGcyc} Figure 2.49

Note 1. t_{PFcyc} : PCLKF cycle, t_{PGcyc} : PCLKG cycle

**Figure 2.48 A/D Converter Trigger Input Timing (ADTRG0)****Figure 2.49 A/D Converter Trigger Input Timing (ADTRG1)**

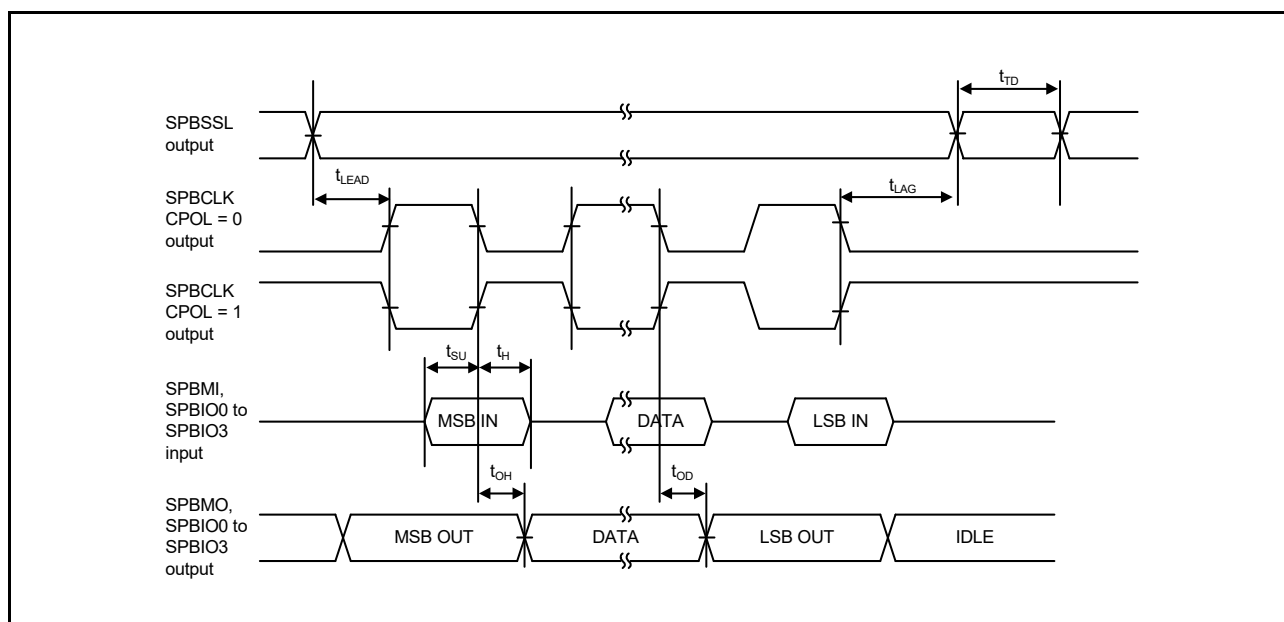


Figure 2.60 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1)

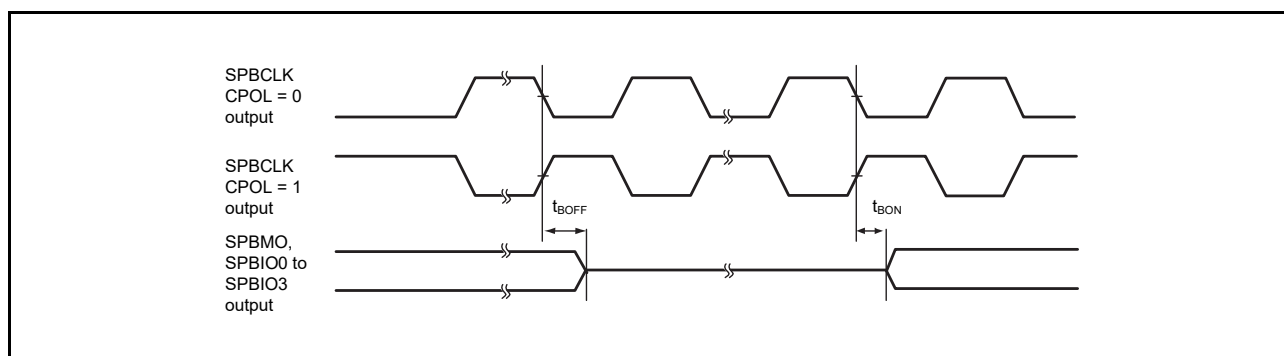


Figure 2.61 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 0)

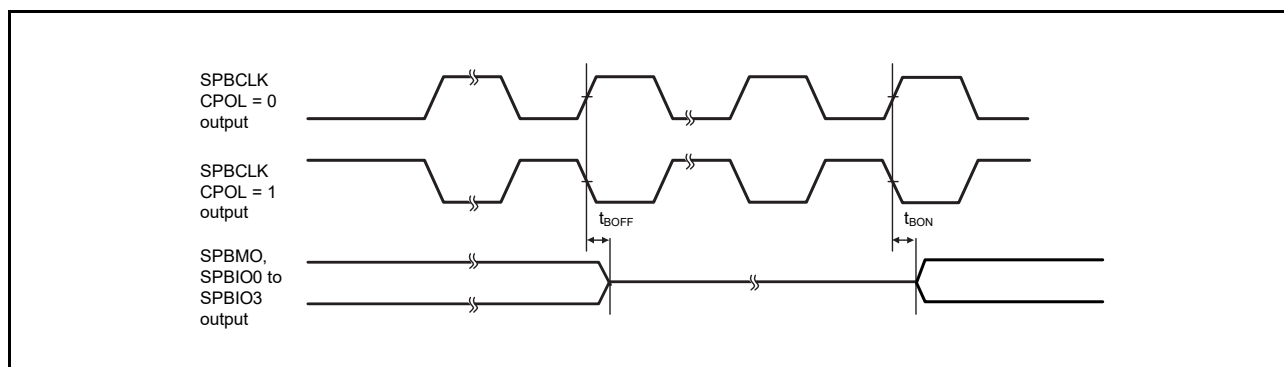


Figure 2.62 SPIBSC Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)

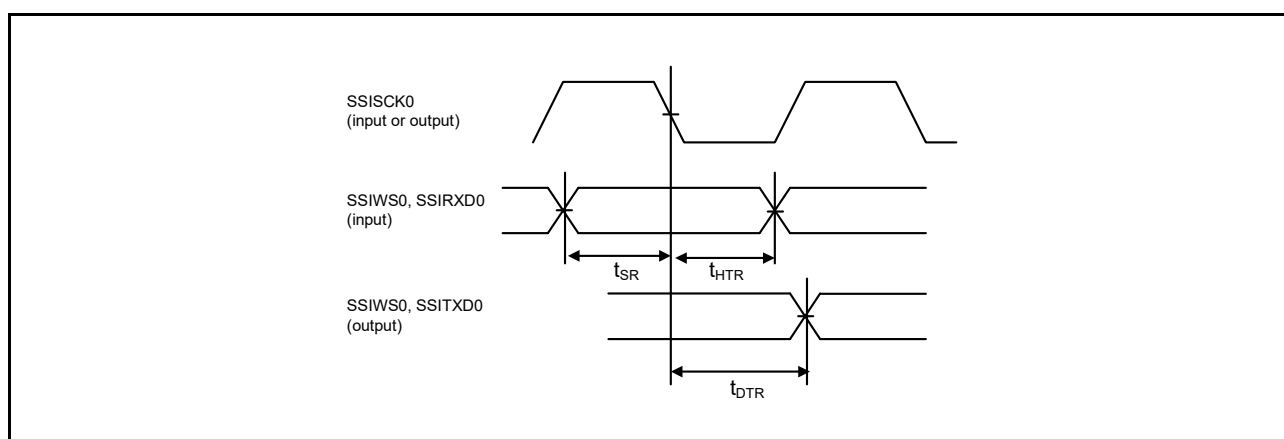


Figure 2.67 Transmit/Receive Timing (SSISCK0 Falling Synchronous)

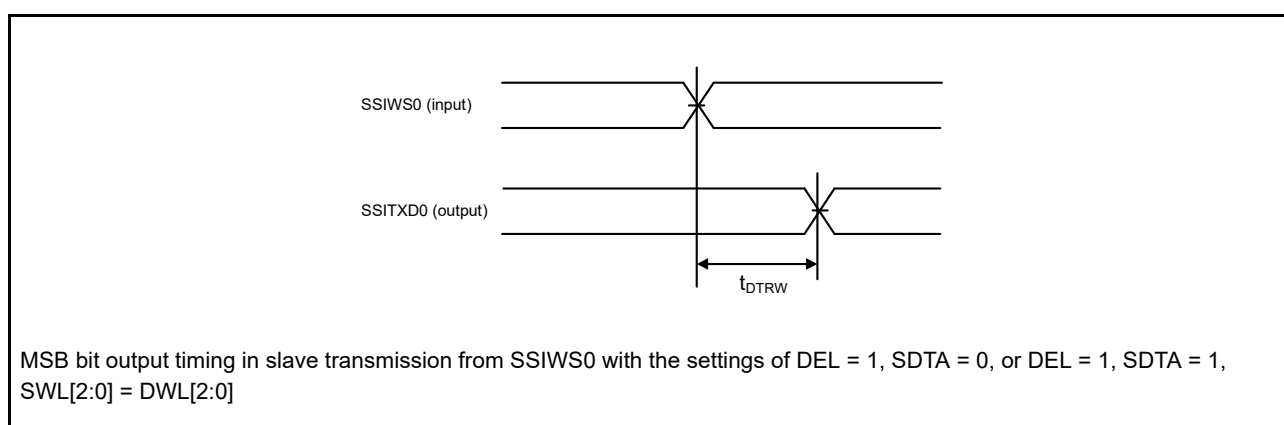


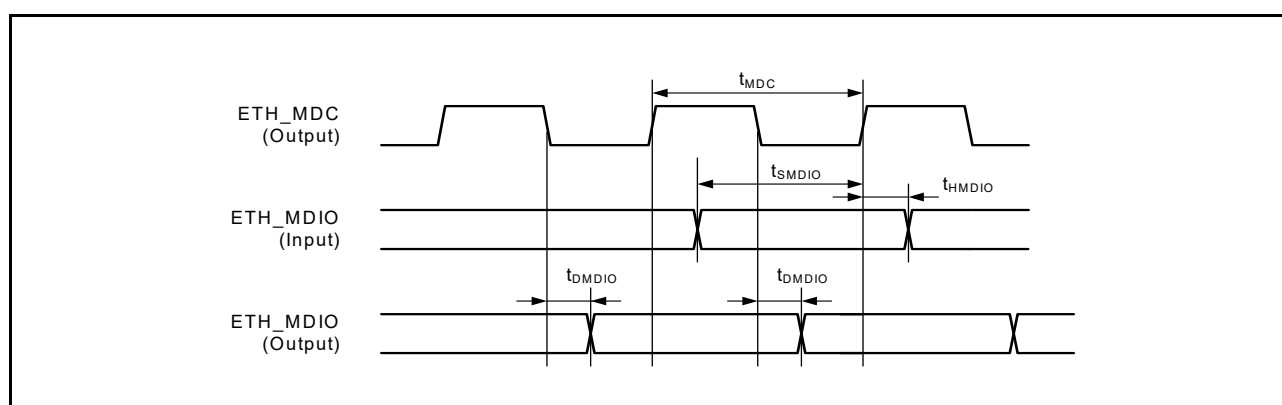
Figure 2.68 SSITXD0 Output Delay from SSIWS0 Change Edge

2.4.5.15 Serial Management Interface Timing

(1) Timing

Table 2.33 Serial Management InterfaceOutput load conditions: $V_{OH} = V_{CCQ33} \times 0.5$, $V_{OL1} = V_{CCQ33} \times 0.5$, $C = 30$ pF

Item	Symbol	min	max	Unit	Test Conditions
MDIO	ETHn_MDC output cycle	t_{MDC}	80	—	ns
	ETHn_MDIO input setting time (to ETHn_MDC↑)	t_{SMDIO}	10	—	ns
	ETHn_MDIO input hold time (to ETHn_MDC↑)	t_{HMDIO}	0	—	ns
	ETHn_MDIO output delay time (to ETHn_MDC↓)	t_{DMDIO}	—	20	ns

**Figure 2.78 Serial Management Access Timing**

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