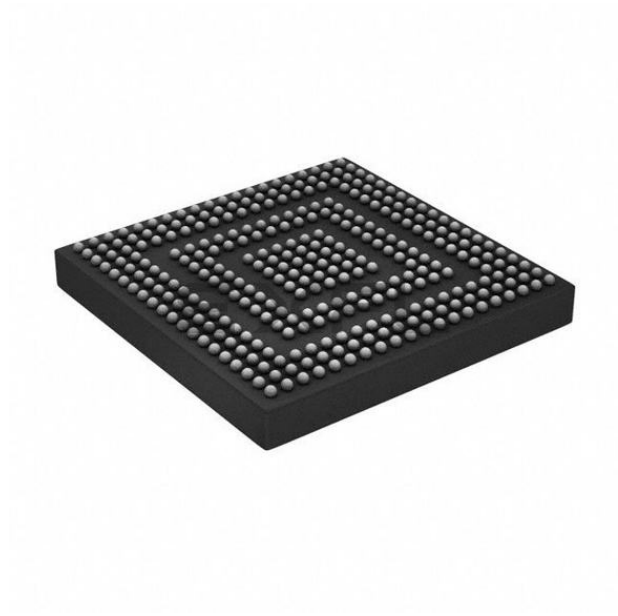
Renesas Electronics America Inc - R7S910017CBG#AC0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R4F
Core Size	32-Bit Single-Core
Speed	450MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	209
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	320-FBGA
Supplier Device Package	320-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910017cbg-ac0

Table 1.3 List of Products (2 / 2)

Part No.	Package	CPU	On-Chip Extended SRAM Capacity	EtherCAT	Operating Frequency (max.)	Security Function *1	Optional Function
R7S910118CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Available	Encoder I/F R-IN Engine (CM3 : 150 MHz)
R7S910025CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	—
R7S910125CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	—
R7S910026CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	Encoder I/F
R7S910126CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	Encoder I/F
R7S910027CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	—
R7S910127CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	—
R7S910028CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	Encoder I/F
R7S910128CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	Encoder I/F
R7S910035CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	—
R7S910135CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	—
R7S910036CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	Encoder I/F
R7S910136CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	Encoder I/F

Note: See the separate documents regarding the encoder I/F.

Note 1. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.

Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8)

Pin Number	Pin Name
C5	PL5 / ETH2_RXD2 / TIOCA8
C6	PB6 / ETH_MDC / TCLKA / SCK3 / RTS4# / MISO3
C7	PB3 / IRQ3 / CS1# / ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1 / MCLK0
C8	PB1 / ETH1_RXER / MTCLKA / TCLKC / CTS4#
C9	PF5 / ETH1_TXEN / MTIOC4A / GTIOC1A / TIC2
C10	P87 / AN1_ANEX1 / A23 / ETH1_TXC / ETH0_RXD0 / MTIOC4C / GTIOC1B / MCLK1
C11	PD6 / AN114 / A22 / ETH1_TXD2 / ETH0_TXD1 / TIC1 / MISO2 / MCLK2
C12	P53 / ETH1_INT / MISO2
C13	P51 / IRQ1 / PHYLINK1 / RSPCK2
C14	AN004
C15	AN000
C16	VREFL0
C17	VREFH0
C18	PD2 / AN110 / WAIT#
C19	P14 / CAS# / MTIOC4A / GTIOC1A / ENCIF10
C20	P13 / RAS# / MTIOC4C / GTIOC1B
D1	P81 / ETH0_RXER / TIOCC0 / CTS4#
D2	P80 / IRQ8 / ETH0_RXDV / TIOCC3 / RTS4#
D3	PU3 / ETH2_COL / TIOCD6 / TXD3
D18	PD0 / AN108 / CS4#
D19	P96 / AN106 / POE0# / POE10# / ENCIF09
D20	P95 / AN105 / IRQ13 / MTCLKA / CTS2#
E1	P84 / ETH0_COL / CATLINKACT1 / RXD4
E2	P82 / ETH0_TXEN / ETH1_CRS / TIOCD3 / SCK4 / RTS3# / USB_OVRCUR
E3	PU1 / ETH2_RXC / TIOCA11 / SCK3
E5	PU0 / ETH2_RXER / TIOCA10
E6	PL6 / ETH2_RXD3 / TIOCA9
E7	PL4 / IRQ4 / ETH2_RXD1
E8	PL2 / ETH2_TXEN / TIOCA6 / ADTRG1
E9	PL0 / ETH2_TXD0 / TIOCB9
E10	PK7 / ETH2_TXD2 / TIOCB7
E11	PK6 / ETH2_TXD3 / TIOCB6
E12	PD5 / AN113 / A21 / ETH1_TXD3 / ETH0_TXD0 / TIC0 / SSL20 / MCLK3
E13	P56 / BS# / ETH1_TXER
E14	PD4 / AN112 / ETH2_INT
E15	VCCQ33
E16	PD1 / AN109 / CS1#
E18	P97 / AN107 / IRQ7 / A25 / ADTRG1
E19	P94 / AN104 / IRQ4 / MTCLKB / RTS2# / ENCIF08
E20	P93 / AN103 / MTIOC1A / TIC3 / SCK2 / ENCIF07
F1	PC4 / CATI2CCLK / TCLKH / SCL0
F2	P83 / IRQ11 / ETH0_CRS / CATLINKACT0 / TXD4
F3	P85 / IRQ5 / CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN
F5	PU4 / MII2_MDC / TIOCC9 / CTS3#
F6	VSS

Table 1.5 Pin Assignments (320-Pin FBGA) (4 / 8)

Pin Number	Pin Name
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VDD
J15	VCCQ33
J16	PA1 / D25 / MTIOC3D / GTIOC0B / MISO0 / AUDIO_CLK / TRACEDATA7 / MCLK3
J18	PA0 / D24 / MTIOC4A / GTIOC1A / MOSI0 / TRACEDATA6 / MDAT3
J19	PT7 / A22 / DACK2 / ENCIF10
J20	PT6 / A21 / DREQ2
K1	PM7 / CATLINKACT1 / PO20
K2	PM5 / CATLEDSTER / PO18
K3	PM4 / CATLEDRUN / PO17
K5	P34 / TDI
K6	PLLVDD1
K8	VDD
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VDD
K15	VSS
K16	P77 / D23 / MTIOC4C / GTIOC1B / RSPCK0 / TRACEDATA5
K18	P76 / D22 / MTIOC4B / GTIOC2A / SSL01 / SSIWS0 / TRACEDATA4
K19	P75 / IRQ13 / D21 / MTIOC4D / GTIOC2B / SSL00 / TRACEDATA3/ ENCIF04
K20	PT5 / BS# / PO30 / TEND2
L1	MD1
L2	MD2
L3	TMS
L5	TCK
L6	PLLVSS1
L8	VDD
L9	VSS
L10	VSS
L11	VSS
L12	VSS
L13	VDD
L15	VSS
L16	PE7 / D15 / MTIOC7A / TIOCD3 / POE8# / SCK1 / RSPCK0 / TRACEDATA7
L18	P72 / D18 / MTIOC1A / TIC2 / TXD1 / SSITXD0 / TRACEDATA0 / ENCIF02
L19	P73 / IRQ3 / D19 / MTCLKB / RXD1 / SSIRXD0 / TRACEDATA1 / ENCIF03
L20	P74 / D20 / MTCLKA / CTS1# / SSL03 / SSISCK0 / TRACEDATA2
M1	XTAL
M2	EXTAL
M3	OSCTH

Table 1.5 Pin Assignments (320-Pin FBGA) (7 / 8)

Pin Number	Pin Name
V10	PH1 / A10 / MTIOC2B / PO11
V11	PH7 / A16 / MTIC5W
V12	P20 / A17 / MTCLKD
V13	P21 / IRQ1 / CS0# / MTIC5V / TIOCB1 / CTS0#
V14	VSS
V15	P45 / CS2#
V16	P46 / CKE
V17	PS2 / MTIOC7C / SSIWS0
V18	P05 / D5 / MTIOC3A
V19	P01 / D1 / MTIC5W / TIOCA2
V20	P02 / D2 / MTIC5V / TIOCA3
W1	P62 / SPBCLK
W2	P65 / SPBIO2 / DREQ0
W3	PN5 / IRQ5 / MTIOC6A / TIOCD9 / ENCIF10
W4	PN6 / MTIOC3C / TIOCC9 / MCLK3 / ENCIF11
W5	PP0 / POE8# / TEND0 / MCLK2
W6	PP2 / MTIOC0C / TCLKH / MCLK1
W7	PP4 / MTIOC0A / MCLK0
W8	PP6 / TIOCA11 / RXD1 / TRACECTL / ENCIF06
W9	PP7 / TCLKF / TCLKH / SCK1 / DACK1 / TRACECLK
W10	PR1 / IRQ9 / POE4# / CTS1# / TEND1 / TRACEDATA1 / ENCIF08
W11	PR3 / TIOCA10 / TIOCB10 / TRACEDATA3 / ENCIF01
W12	PR5 / TIOCA8 / TIOCB8 / TRACEDATA5 / ENCIF03
W13	P24 / IRQ12 / RD/WR# / RXD0
W14	P22 / IRQ2 / RD# / MTIOC7B / TIOCD0 / SCK0
W15	P44 / IRQ12 / WAIT# / TCLKD / ADTRG0 / CTS0#
W16	P43 / WE2#/DQMUL / MTIOC8B / USB_VBUSEN
W17	PS1 / IRQ1 / MTIOC7B / SSISCK0
W18	PS3 / MTIOC7A / SSIRXD0
W19	PS4 / MTIOC6D / SSITXD0
W20	PS5 / MTIOC6B
Y1	VSS
Y2	P67 / IRQ15 / GTIOC3B / CTXD0 / TEND0 / USB_OVRCUR
Y3	P66 / IRQ14 / GTIOC3A / CTXD1 / DACK0 / USB_VBUSEN
Y4	PN7 / MTIOC3A / TIOCD6 / DREQ0 / MDAT3 / ENCIF12
Y5	PP1 / MTIOC0D / DACK0 / MDAT2
Y6	PP3 / MTIOC0B / TCLKC / MDAT1
Y7	PP5 / PO22 / MDAT0
Y8	VSS
Y9	PR0 / TCLKE / TCLKG / TXD1 / DREQ1 / TRACEDATA0 / ENCIF07
Y10	PR2 / TIOCA11 / TIOCB11 / RTS1# / TRACEDATA2 / ENCIF00
Y11	PR4 / TIOCA9 / TIOCB9 / TRACEDATA4 / ENCIF02
Y12	PR6 / TIOCA7 / TIOCB7 / TRACEDATA6 / ENCIF04
Y13	PR7 / TIOCA6 / TIOCB6 / TRACEDATA7 / ENCIF05
Y14	P25 / A18 / MTCLKC / TEND1

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (5 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
H12	VDD							
H13	VSS							
H15		PA6	D30 / A21	GTIOC3A	CTS2#	MDAT0	IRQ6	
H16		PA5	D29	TIOCA4	ETH0_INT / ETH1_TXER / TXD2	MCLK1		
H18		PA2	D26 / DREQ2	MTIOC3B / GTIOC0A	SSL02	MDAT2 / ENCIF05		
H19		PK0	CAS#	PO31		ENCIF11		
H20		PK1	CS5#			ENCIF12		
J1		PM6		PO19	CATLINKACT0		IRQ6	
J2		PM3		PO16	CATSYNC0 / CATLATCH0			
J3		PM2		TCLKE	CATSYNC1 / CATLATCH1 / RTS4#			
J5	TDO	P33						
J6	TRST#							
J8	VDD							
J9	VSS							
J10	VSS							
J11	VSS							
J12	VSS							
J13	VDD							
J15	VCCQ33							
J16	TRACEDATA7	PA1	D25	MTIOC3D / GTIOC0B	MISO0	AUDIO_CLK / MCLK3		
J18	TRACEDATA6	PA0	D24	MTIOC4A / GTIOC1A	MOSI0	MDAT3		
J19		PT7	A22 / DACK2			ENCIF10		
J20		PT6	A21 / DREQ2					
K1		PM7		PO20	CATLINKACT1			
K2		PM5		PO18	CATLEDSTER			
K3		PM4		PO17	CATLEDRUN			
K5	TDI	P34						
K6	PLLVDD1							
K8	VDD							
K9	VSS							
K10	VSS							
K11	VSS							
K12	VSS							
K13	VDD							
K15	VSS							
K16	TRACEDATA5	P77	D23	MTIOC4C / GTIOC1B	RSPCK0			

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
R16	VCCQ33							
R18	VCCQ33							
R19		PS6		TIOCA5 / TIOCB5 / PO23	RXD2	ENCIF06	IRQ14	
R20		PS7		TIOCA4 / TIOCB4 / PO24	TXD2			
T1	DVDD_USB							
T2	VDD33_USB							
T3		P32			USB_OVRCUR		IRQ10	
T5		PC6	DREQ0	TCLKC	SCL1 / CRXD0 / USB_VBUSIN			
T6		P37	WE1#/ DQMLU	PO1				
T7		P36	WE0#/ DQMLL	PO0				
T8		PG3	A4	PO5 / TIC1	MISO1			
T9		PG6	A7	TCLKB / PO8	SSL11			
T10		PH3	A12	MTIOC1B / PO13				
T11	VCCQ33							
T12		PH5	A14	PO15				
T13	VCCQ33							
T14		P26	A19 / DREQ1	MTIOC8D				
T15	VCCQ33							
T16	VSS							
T18	VSS							
T19	TRACEDATA0	PE0	D8	MTIOC1B / TIOCB2				
T20	TRACEDATA1	PE1	D9	MTCLKD / TIOCB3	SSL03			
U1		P60	TEND0		CTXD0 / SPBSSL			
U2		P63			SPBMO/SPBIO0			
U3		PN1		MTIOC8C / PO21	MISO1	ENCIF09		
U18	TRACECTL	P00	D0	MTIOC6A / TIOCA1				ADTRG1
U19		P04	D4	MTIOC3C / TIOCA5				
U20		P03	D3	MTIC5U / TIOCA4				
V1		P61	DACK0		CTXD1 / SPBIO3			
V2		P64			SPBMI/SPBIO1			
V3		PN3		MTIOC8A	RSPCK1			
V4		PN4		MTIOC6C / TIOCC6	SSL11		IRQ12	
V5		PC7		TIC0	SDA1 / CRXD1			
V6		PG1	A2	PO3				
V7		PG4	A5	PO6 / TOC1	MOSI1			
V8		PG5	A6	TCLKA / PO7	SSL10			
V9		PH0	A9	PO10				
V10		PH1	A10	MTIOC2B / PO11				
V11		PH7	A16	MTIC5W				

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
V12		P20	A17	MTCLKD				
V13		P21	CS0#	MTIC5V / TIOCB1	CTS0#		IRQ1	
V14	VSS							
V15		P45	CS2#					
V16		P46	CKE					
V17		PS2		MTIOC7C		SSIWS0		
V18		P05	D5	MTIOC3A				
V19		P01	D1	MTIC5W / TIOCA2				
V20		P02	D2	MTIC5V / TIOCA3				
W1		P62			SPBCLK			
W2		P65	DREQ0		SPBIO2			
W3		PN5		MTIOC6A / TIOCD9		ENCIF10	IRQ5	
W4		PN6		MTIOC3C / TIOCC9		MCLK3 / ENCIF11		
W5		PP0	TEND0	POE8#		MCLK2		
W6		PP2		MTIOC0C / TCLKH		MCLK1		
W7		PP4		MTIOC0A		MCLK0		
W8	TRACECTL	PP6		TIOCA11	RXD1	ENCIF06		
W9	TRACECLK	PP7	DACK1	TCLKF / TCLKH	SCK1			
W10	TRACEDATA1	PR1	TEND1	POE4#	CTS1#	ENCIF08	IRQ9	
W11	TRACEDATA3	PR3		TIOCA10 / TIOCB10		ENCIF01		
W12	TRACEDATA5	PR5		TIOCA8 / TIOCB8		ENCIF03		
W13		P24	RD/WR#		RXD0		IRQ12	
W14		P22	RD#	MTIOC7B / TIOCD0	SCK0		IRQ2	
W15		P44	WAIT#	TCLKD	CTS0#		IRQ12	ADTRG0
W16		P43	WE2#/ DQMUL	MTIOC8B	USB_VBUSEN			
W17		PS1		MTIOC7B		SSISCK0	IRQ1	
W18		PS3		MTIOC7A		SSIRXD0		
W19		PS4		MTIOC6D		SSITXD0		
W20		PS5		MTIOC6B				
Y1	VSS							
Y2		P67	TEND0	GTIOC3B	CTXD0 / USB_OVRCUR		IRQ15	
Y3		P66	DACK0	GTIOC3A	CTXD1 / USB_VBUSEN		IRQ14	
Y4		PN7	DREQ0	MTIOC3A / TIOCD6		MDAT3 / ENCIF12		
Y5		PP1	DACK0	MTIOC0D		MDAT2		
Y6		PP3		MTIOC0B / TCLKC		MDAT1		
Y7		PP5		PO22		MDAT0		
Y8	VSS							
Y9	TRACEDATA0	PR0	DREQ1	TCLKE / TCLKG	TXD1	ENCIF07		
Y10	TRACEDATA2	PR2		TIOCA11 / TIOCB11	RTS1#	ENCIF00		

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (10 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
Y11	TRACEDATA4	PR4		TIOCA9 / TIOCB9		ENCIF02		
Y12	TRACEDATA6	PR6		TIOCA7 / TIOCB7		ENCIF04		
Y13	TRACEDATA7	PR7		TIOCA6 / TIOCB6		ENCIF05		
Y14		P25	A18 / TEND1	MTCLKC				
Y15		P41	BS#		SCK0			
Y16		P42		MTIOC7C	RXD0			
Y17		P40		MTIOC8A	TXD0			
Y18		PS0		MTIOC7D		AUDIO_CLK		
Y19	TRACECLK	P10	CKIO	TIOCA0			IRQ0	
Y20	VSS							

Note 1. Optional

Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP) (4 / 6)

Pin Number 176-Pin HLQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
106	TRACEDATA 7	PE7	D15	MTIOC7A / TIOCD3 / POE8#	SCK1 / RSPCK0			
107	VSS							
108	VDD							
109	TRACECLK	P70	D16	MTIOC6D	RTS1# / USB_OVRCUR		IRQ0	
110	TRACECTL	P71	D17	POE0# / POE10# / TOC2	SCK1			
111	TRACEDATA 0	P72	D18	MTIOC1A / TIC2	TXD1	SSITXD0		
112	TRACEDATA 1	P73	D19	MTCLKB	RXD1	SSIRXD0	IRQ3	
113	TRACEDATA 2	P74	D20	MTCLKA	CTS1# / SSL03	SSISCK0		
114	TRACEDATA 3	P75	D21	MTIOC4D / GTIOC2B	SSL00		IRQ13	
115	TRACEDATA 4	P76	D22	MTIOC4B / GTIOC2A	SSL01	SSIWS0		
116	TRACEDATA 5	P77	D23	MTIOC4C / GTIOC1B	RSPCK0			
117	TRACEDATA 6	PA0	D24	MTIOC4A / GTIOC1A	MOSI0	MDAT3		
118	TRACEDATA 7	PA1	D25	MTIOC3D / GTIOC0B	MISO0	AUDIO_CLK / MCLK3		
119	VSS							
120	VDD							
121		PA2	D26 / DREQ2	MTIOC3B / GTIOC0A	SSL02	MDAT2		
122		PA3	D27 / DACK2	GTETRG / TIOCA2	ETHSWSECOUT / SCK2	MCLK2		
123		PA4	D28 / TEND2	TIOCA3	ETH1_INT / RXD2	MDAT1		ADTRG0
124		PA5	D29	TIOCA4	ETH0_INT / ETH1_TXER / TXD2	MCLK1		
125		PA6	D30 / A21	GTIOC3A	CTS2#	MDAT0	IRQ6	
126	VCCQ33							
127		PA7	D31 / A22	MTIOC6B / GTIOC3B	RTS2#	MCLK0	IRQ7	
128	VDD							
129	VSS							
130		P13	RAS#	MTIOC4C / GTIOC1B				
131		P14	CAS#	MTIOC4A / GTIOC1A				
132		P15	CS3# / CKE	MTIOC3D / GTIOC0B				
133		P16	CS4# / CS2#	MTIOC3B / GTIOC0A				

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V

Item	Symbol	Value	Unit
Power supply voltage (I/O)	VCCQ33	–0.3 to +4.2	V
Power supply voltage (internal)	VDD	–0.3 to +1.6	V
PLL power supply voltage	PLLVDD0, PLLVDD1	–0.3 to +1.6	V
Input voltage (except for ports for 5-V tolerant*1)	V_{in1}	–0.3 to VCCQ33 + 0.3*5	V
Input voltage (ports for 5-V tolerant*1)	V_{in2}	–0.3 to +5.5*3	V
Analog power supply voltage	AVCC0, AVCC1*2	–0.3 to +4.2	V
Reference power supply voltage	VREFH0, VREFH1	–0.3 to (AVCC0, AVCC1) + 0.3*5	V
USB digital power supply voltage	DVDD_USB	–0.3 to +1.6	V
USB power supply voltage	VDD33_USB*2	–0.3 to +4.2	V
Analog input voltage	V_{AN}	–0.3 to (AVCC0, AVCC1) + 0.3*5	V
Operating temperature (junction temperature)	Tj*4	–40 to +125	°C
Storage temperature	T_{stg}	–55 to +125	°C

[Usage Notes]

1. Do not directly connect output pins (I/O pins in output state) of IC products to other output pins (including I/O pins in output state) , power pins, or GND pins. However, output pins are directly connectable in an external circuit where timing design is provided to avoid conflict of outputs of high-impedance pins such as I/O pins.
2. If even a single item exceeds the absolute maximum rating for even a moment, it may degrade the product's quality. In other words, the absolute maximum rating is a rated value that potentially causes physical damage to products. Use products with a margin of the absolute maximum rating.
   Specified values and conditions shown in DC characteristics and AC characteristics are the range of normal operation and quality assurance of products.

Note 1. Ports PC0 to PC7 and P30 are 5-V tolerant.
Note 2. When the A/D converter unit 0 is not to be used, connect the AVCC0 and VREFH0 pins to VCCQ33 and the AVSS0 and VREFL0 pins to VSS, respectively. Do not leave these pins open. In the same way, when the A/D converter unit 1 is not to be used, connect the AVCC1 and VREFH1 pins to VCCQ33 and the AVSS1 and VREFL1 pins to VSS, respectively. Do not leave these pins open. When the USB is not to be used, connect the VDD33_USB pin to VCCQ33, the VSS_USB pin to VSS, and the DVDD_USB pin to VDD, respectively. Do not leave these pins open.
Note 3. When VCCQ33 is less than 3.0 V, the rated value of ports for 5-V tolerant is 3.6 V.
Note 4. For operations at the temperatures over 110°C (junction temperature), refer to the RZ/T1 Group Application Note: Precautions for High-Temperature Operations (R01AN3116).
Note 5. Do not exceed the absolute maximum rating, 4.2 V.

2.3 DC Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125°C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 2.2 DC Characteristics (1)

Item	Symbol	min	typ	max	Unit	Test Conditions
Power supply voltage (I/O)	VCCQ33	3.0	3.3	3.6	V	
Power supply voltage (internal)	VDD	1.14	1.2	1.26	V	
PLL power supply voltage	PLLVDD0, PLLVDD1	1.14	1.2	1.26	V	
USB digital power supply voltage	DVDD_USB	1.14	1.2	1.26	V	
Analog power supply voltage	AVCC0, AVCC1	3.0	3.3	3.6	V	
USB power supply voltage	VDD33_USB	3.0	3.3	3.6	V	

Table 2.13 EXTAL Clock Timing

Item	Symbol	min	typ	max	Unit
EXTAL external clock input cycle time	t_{EXcyc}	40.00 + 50 ppm			ns
		25.00 ± 25ppm*1			MHz

Note 1. When EtherCAT is in use

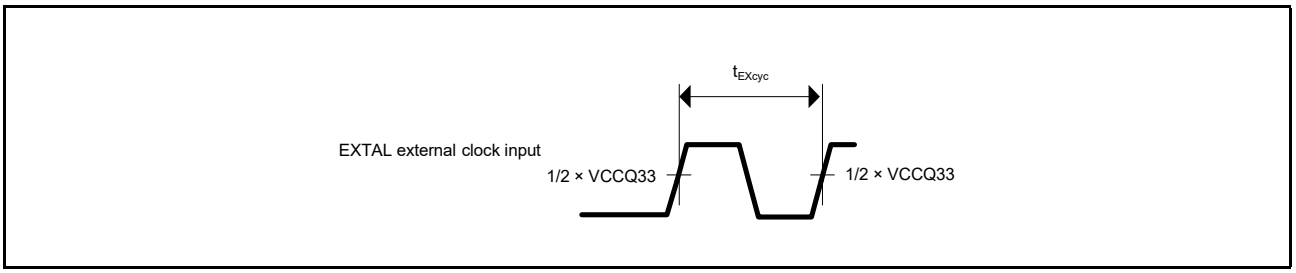


Figure 2.5 EXTAL External Clock Input Timing

Table 2.14 XTAL Clock Timing

Item	Symbol	min	typ	max	Unit
XTAL clock oscillator output cycle*1	$t_{XTALcyc}$		40.00 + 50 ppm*2		ns

Note 1. When using the XTAL clock, ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.
Note 2. When using the EtherCAT, make sure that the clock timing satisfies 25.00 MHz ± 25 ppm.

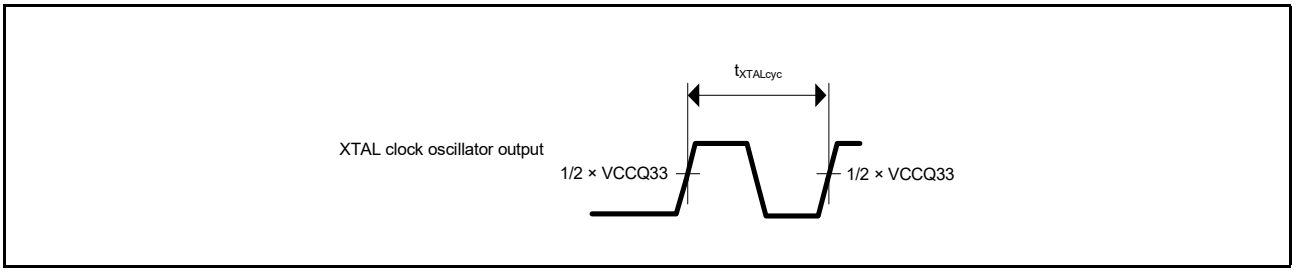


Figure 2.6 XTAL Clock Oscillator Output Timing

Table 2.15 LOCO Clock Timing

Item	Symbol	min	typ	max	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.62	4.17	3.79	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	40	µs	Figure 2.7

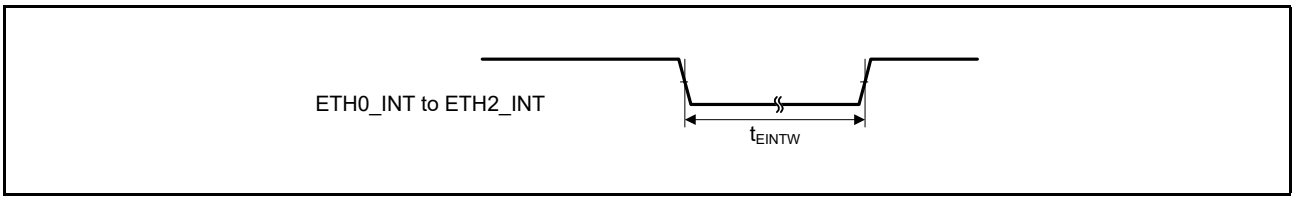
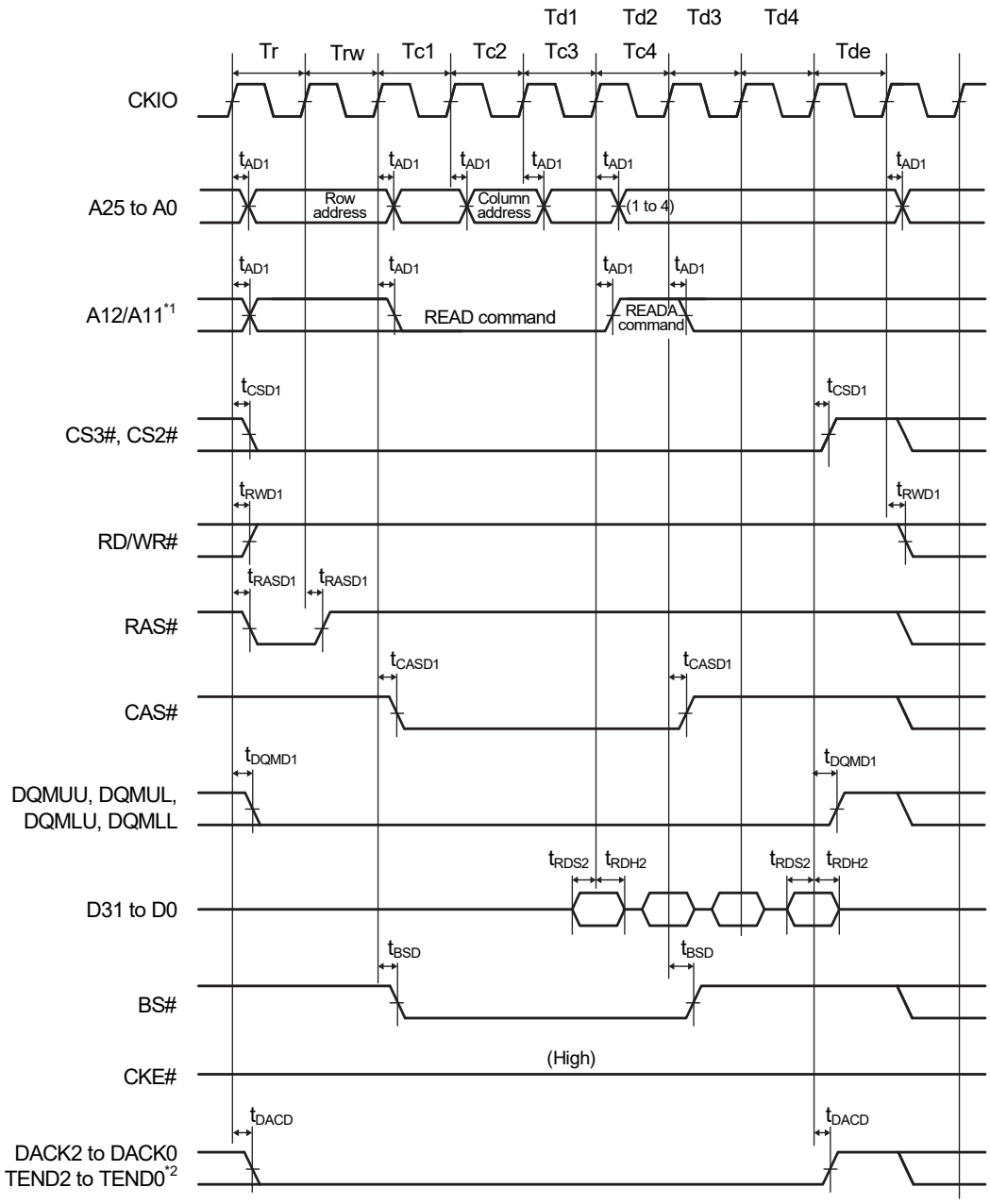
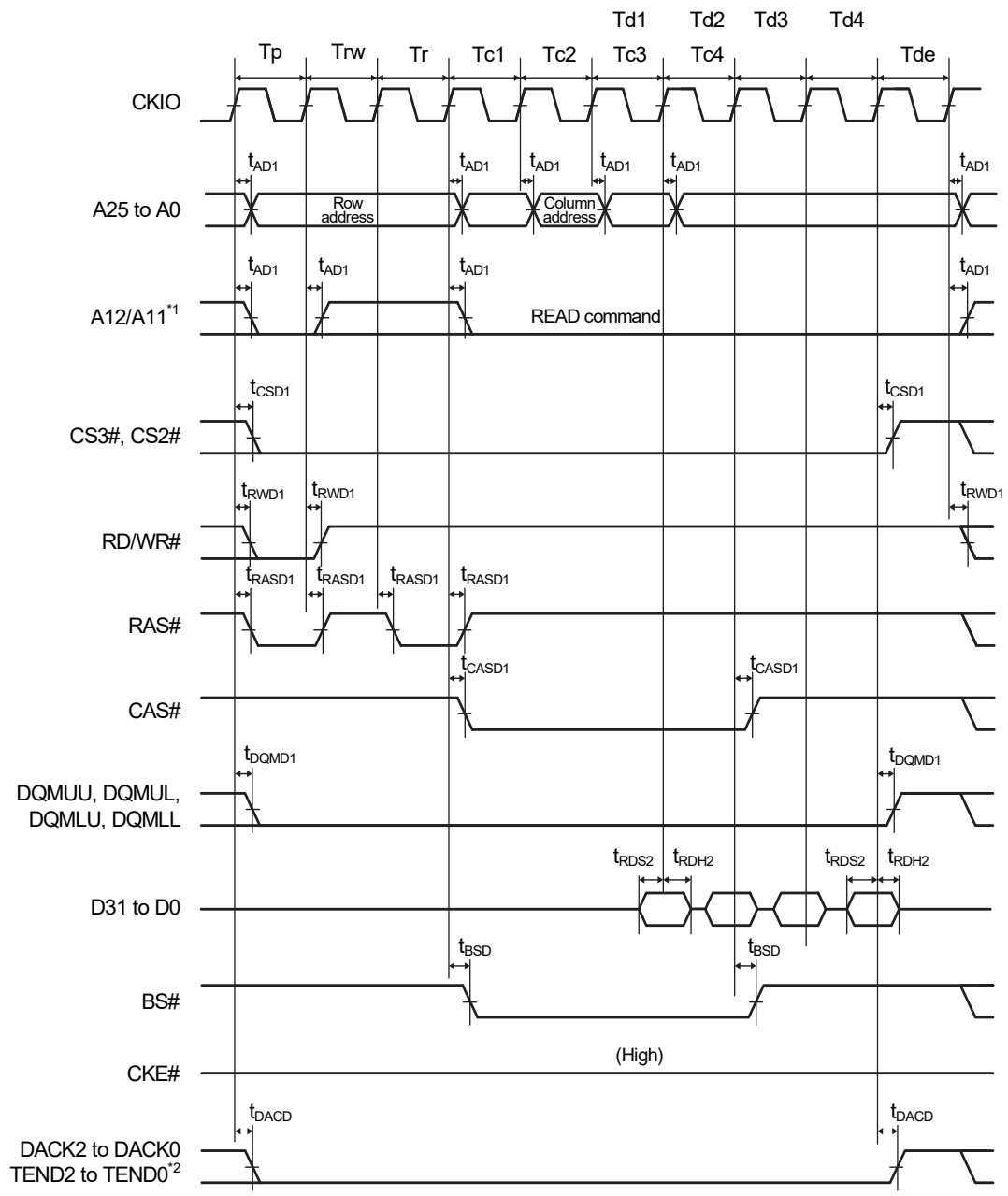


Figure 2.11 ETH_INT Interrupt Input Timing



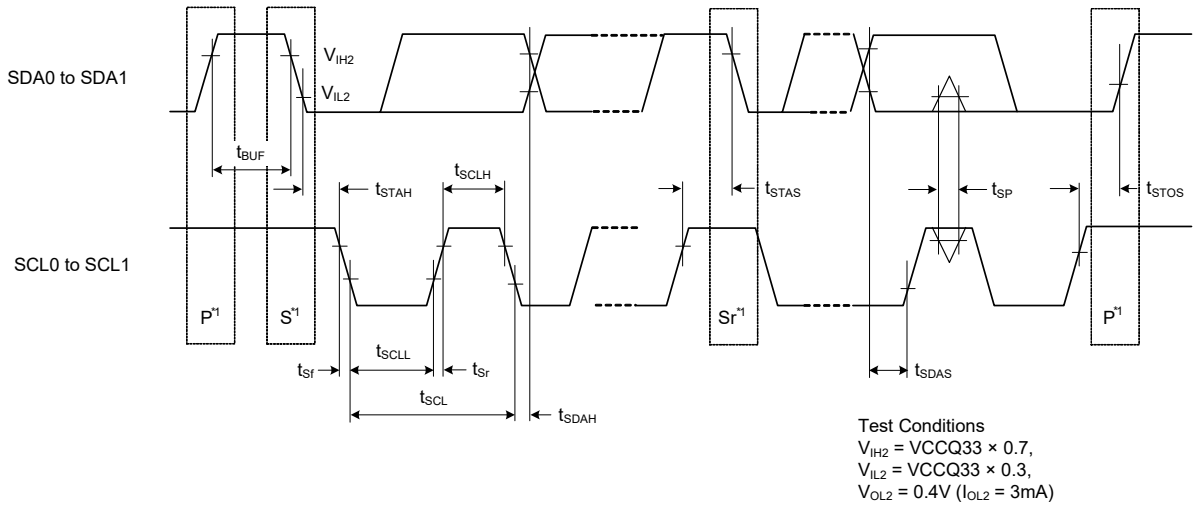
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.23 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (with Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 0 Cycles)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.30 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: PRE + ACT + READ Command, Different Row Address, CAS Latency 2, WTRCD = 0 Cycles)



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.64 RIICa Bus Interface Input/Output Timing

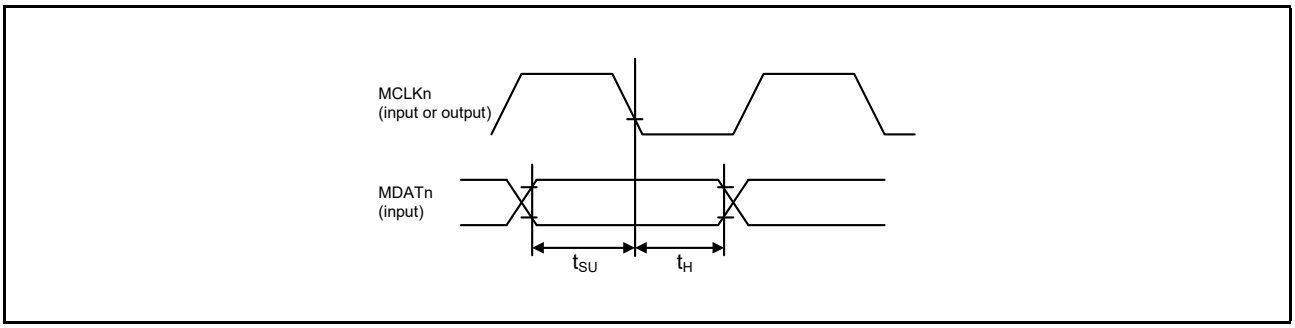


Figure 2.81 Reception Timing (MCLKn Falling Synchronous)

2.5 USB Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 2.35 On-chip USB Full-Speed Characteristics (USB_DP, USB_DM Pin Characteristics)

Item	Symbol	min	typ	max	Unit	Test Conditions
Rising time	t_{FR}	4	—	20	ns	Figure 2.82
Falling time	t_{FF}	4	—	20	ns	
Rising/falling time ratio	t_{FR} / t_{FF}	90	—	111.11	%	t_{FR} / t_{FF}

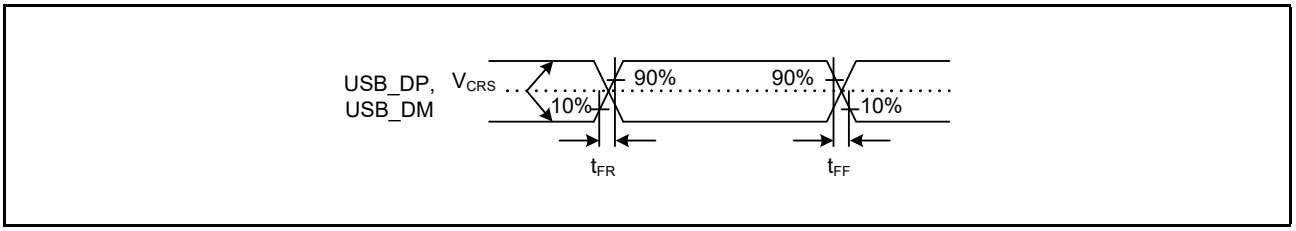


Figure 2.82 USB_DP, USB_DM Output Timing (Full Speed)

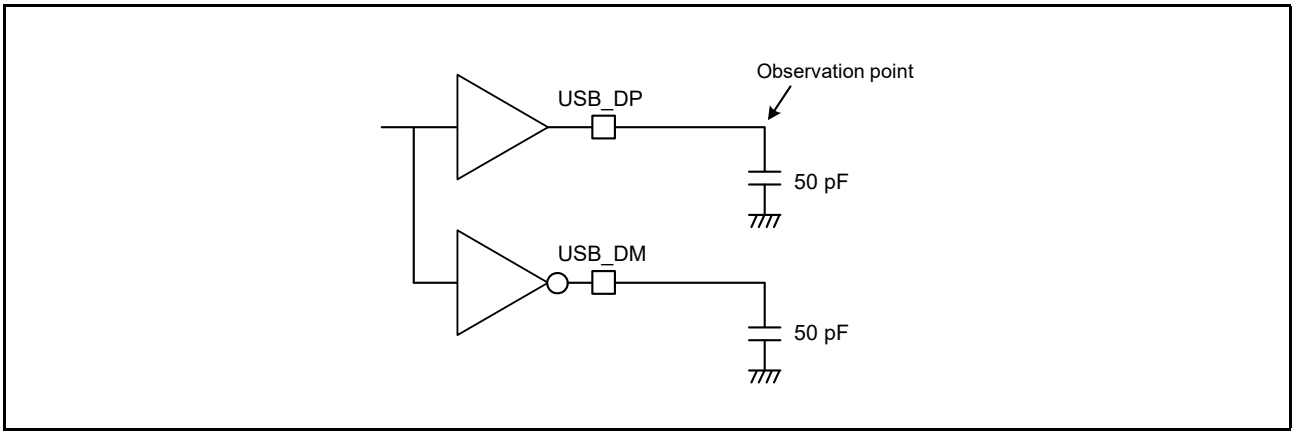


Figure 2.83 Measurement Circuit (Full Speed)

2.7 Temperature Sensor Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = –40 to 125 °C

Note: The 176-pin HLQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 2.39 Temperature Sensor Characteristics

Item	min	typ	max	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (at 25°C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	µs	
Sampling time	4.25	—	—	µs	ADSSTRT.SST[7:0] = 255 states (when PCLKF [ADC (unit0) sampling CLK] = 60 MHz)

2.8 Oscillation Stop Detection Timing

Table 2.40 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	min	typ	max	Unit	Test Conditions
Clock switching time	t_{dr}	—	—	1	ms	Figure 2.86

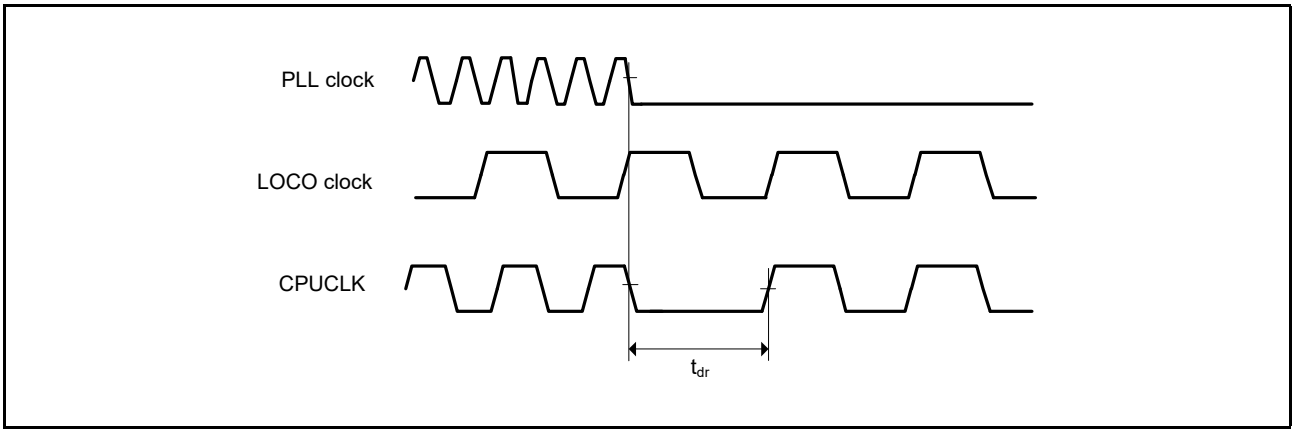


Figure 2.86 Oscillation Stop Detection Timing

Rev.	Date	Description	
		Page	Summary
1.40	Jan. 19, 2018	All	Cortex-R4F changed to Cortex-R4
			Terms corrected (Ether Switch → Ethernet switch; Ether Mac → Ethernet Mac; Ether PHY → Ethernet PHY; Ether clock(s) → Ethernet clock(s); receive buffer(s) → reception buffer(s); transmit buffer(s) → transmission buffer(s); transmit/receive buffer(s) → transmission/reception buffer(s); transmit mode → transmission mode; receive mode → reception mode; compare match counter (CMCNT) → compare match timer counter (CMCNT); compare match constant register (CMCOR) → compare match timer constant register (CMCOR); low active → active low; high active → active high; valley → trough)
		Features	
		1	■ Encoder interfaces, changed ■ Various communications interfaces: Features of Ethernet changed
		1. Overview	
		2	1.1 Outline of Specifications: "Cortex®-R4F processor" changed to "Cortex®-R4 processor with FPU"
		2	Table 1.1 Outline of Specifications (1 / 7): Registered trademark symbol added to "Thumb"; description of "Clock" changed
		8	Table 1.1 Outline of Specifications (7 / 7): Description of the encoder interfaces changed
		16	Table 1.4 Pin Functions (4 / 7): CTS0# to CTS4#: I/O and functional description changed; RTS0# to RTS4#: Functional description changed
		19	Table 1.4 Pin Functions (7 / 7): ENCIF07 to ENCIF12 changed to ENCIF00 to ENCIF12
		22	Table 1.5 Pin Assignments (320-Pin FBGA) (1 / 8): ENCIF12 added to B19; ENCIF11 added to B20
		23	Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8): ENCIF10 added to C19; ENCIF09 added to D19; ENCIF08 added to E19
		24	Table 1.5 Pin Assignments (320-Pin FBGA) (3 / 8): ENCIF11 added to H19; ENCIF12 added to H20
		25	Table 1.5 Pin Assignments (320-Pin FBGA) (4 / 8): ENCIF10 added to J19
		26	Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8): ENCIF09 added to N20; ENCIF08 added to P20
		27	Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8): ENCIF09 added to U3
		28	Table 1.5 Pin Assignments (320-Pin FBGA) (7 / 8): ENCIF10 added to W3; ENCIF11 added to W4; ENCIF08 added to W10; ENCIF12 added to Y4
		35	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (2 / 10): ENCIF12 added to B19 under "Others"; ENCIF11 added to B20 under "Others"
		36	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10): ENCIF10 added to C19 under "Others"; ENCIF09 added to D19 under "Others"; ENCIF08 added to E19 under "Others"
		38	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (5 / 10); ENCIF11 added to H19 under "Others"; ENCIF12 added to H20 under "Others"; ENCIF10 added to J19 under "Others"
		40	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10): ENCIF09 added to N20 under "Others"; ENCIF08 added to P20 under "Others"
		41	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10): ENCIF09 added to U3 under "Others"
		42	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10): ENCIF10 added to W3 under "Others"; ENCIF11 added to W4 under "Others"; ENCIF08 added to W10 under "Others; ENCIF12 added to Y4
		2. Electrical Characteristics	
		54	Table 2.3 DC Characteristics (2) [Power Supply]: Entries added to the "300MHz" row of VDD
		65, 66	Table 2.17 Bus Timing: "CKIO = 75MHz" changed to "CKIO = 1/tCKcyc; "tcyc" changed to "tCKcyc"; entries for "Address delay time 1", "CS# delay time 1", "Read/write delay time 1", "Read data setup time 1 to 3" and "WAIT# setup time" changed; Notes 1, 3, and 4 changed
		102	Table 2.27 RSPIa Timing: Note 2 changed (SSLND → SPCKD): Note 3 added
		111	Figure 2.64 RIICa Bus Interface Input/Output Timing: SDA0 to SDA3 and SCL0 to SCL3 deleted