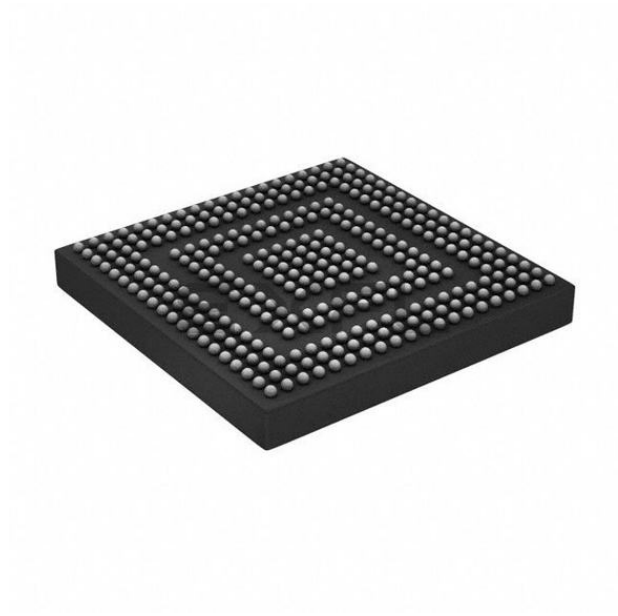
Renesas Electronics America Inc - R7S910018CBG#AC0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R4F
Core Size	32-Bit Single-Core
Speed	600MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	209
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	320-FBGA
Supplier Device Package	320-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s910018cbg-ac0

Table 1.1 Outline of Specifications (5 / 7)

Classification	Module/Function	Description
Communication function	Ethernet MAC (ETHERC)	• 1 port • IEEE802.3 is supported • 10BASE and 100BASE are supported • Full duplex and half duplex are supported • Automatic pause packet transmission function • Auto broadcast suspension function by the pause packet reception • MII/RMII interface is supported
	Ethernet switch	• 2-port PHY interfaces • IEEE802.3 • 10BASE, 100BASE • Full and half duplex • Hardware switching, lookup, and filtering • QoS with frame prioritization • Priority control based on VLAN Priority (IEEE802.1q), which enables priority reassignment • Classification and priority assignment based on IPv4 DiffServ Code Point Field, IPv6 Class of Service • Queue with four priority levels • Multicasting and broadcasting • VLAN frame • IEEE1588 timer module • Cut-through and hub features • Device level ring (DLR)
	EtherCAT Slave Controller (ECATC) *2	• 1 channel (2 ports) *3 • EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented
	USB 2.0 HS host/ function module	• 1 port • Compliance with the USB 2.0 specification • Transfer rate High speed (480 Mbps), full speed (12 Mbps) • Communications buffer Incorporates 1 Kbyte of RAM for host mode Incorporates 8 Kbytes of RAM for function mode
	Serial communication interface with FIFO (SCIFA)	• 5 channels • Serial communications modes: Asynchronous, clock synchronous • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Both the transmission and reception sections are equipped with 16-byte FIFO buffers, allowing continuous transmission and reception. • Bit rate modulation
	I^2C bus interface (RIICa)	• 2 channels I^2C bus format Supports the multi-master Max. transfer rate: 400 kbps • Event linking by the ELC
	CAN module (RSCAN)	• 2 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • Message buffers Max. 64 × 2 channels of reception message buffers, which are used by all channels 16 transmission message buffers per channel • Max. transfer rate: 1 Mbps

1.2 List of Products

Table 1.3 is a list of products.

Table 1.3 List of Products (1 / 2)

Part No.	Package	CPU	On-Chip Extended SRAM Capacity	EtherCAT	Operating Frequency (max.)	Security Function *1	Optional Function
R7S910001CFP	176 pins (PLQP0176LD-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	—
R7S910101CFP	176 pins (PLQP0176LD-A)	Cortex-R4	Not supported	Not supported	450 MHz	Available	—
R7S910002CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	—
R7S910102CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Available	—
R7S910006CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	450 MHz	Not supported	—
R7S910106CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	450 MHz	Available	—
R7S910007CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Not supported	—
R7S910107CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Available	—
R7S910011CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	Encoder I/F
R7S910111CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Available	Encoder I/F
R7S910013CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Not supported	Encoder I/F
R7S910113CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Available	Encoder I/F
R7S910015CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Not supported	R-IN Engine (CM3 : 150MHz)
R7S910115CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Available	R-IN Engine (CM3 : 150MHz)
R7S910016CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Not supported	Encoder I/F R-IN Engine (CM3 : 150MHz)
R7S910116CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Available	Encoder I/F R-IN Engine (CM3 : 150MHz)
R7S910017CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Not supported	R-IN Engine (CM3 : 150MHz)
R7S910117CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Available	R-IN Engine (CM3 : 150MHz)
R7S910018CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Not supported	Encoder I/F R-IN Engine (CM3 : 150MHz)

Table 1.3 List of Products (2 / 2)

Part No.	Package	CPU	On-Chip Extended SRAM Capacity	EtherCAT	Operating Frequency (max.)	Security Function *1	Optional Function
R7S910118CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Available	Encoder I/F R-IN Engine (CM3 : 150 MHz)
R7S910025CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	—
R7S910125CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	—
R7S910026CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	Encoder I/F
R7S910126CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	Encoder I/F
R7S910027CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	—
R7S910127CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	—
R7S910028CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	Encoder I/F
R7S910128CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	Encoder I/F
R7S910035CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	—
R7S910135CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	—
R7S910036CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	Encoder I/F
R7S910136CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	Encoder I/F

Note: See the separate documents regarding the encoder I/F.

Note 1. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.

Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8)

Pin Number	Pin Name
C5	PL5 / ETH2_RXD2 / TIOCA8
C6	PB6 / ETH_MDC / TCLKA / SCK3 / RTS4# / MISO3
C7	PB3 / IRQ3 / CS1# / ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1 / MCLK0
C8	PB1 / ETH1_RXER / MTCLKA / TCLKC / CTS4#
C9	PF5 / ETH1_TXEN / MTIOC4A / GTIOC1A / TIC2
C10	P87 / AN1_ANEX1 / A23 / ETH1_TXC / ETH0_RXD0 / MTIOC4C / GTIOC1B / MCLK1
C11	PD6 / AN114 / A22 / ETH1_TXD2 / ETH0_TXD1 / TIC1 / MISO2 / MCLK2
C12	P53 / ETH1_INT / MISO2
C13	P51 / IRQ1 / PHYLINK1 / RSPCK2
C14	AN004
C15	AN000
C16	VREFL0
C17	VREFH0
C18	PD2 / AN110 / WAIT#
C19	P14 / CAS# / MTIOC4A / GTIOC1A / ENCIF10
C20	P13 / RAS# / MTIOC4C / GTIOC1B
D1	P81 / ETH0_RXER / TIOCC0 / CTS4#
D2	P80 / IRQ8 / ETH0_RXDV / TIOCC3 / RTS4#
D3	PU3 / ETH2_COL / TIOCD6 / TXD3
D18	PD0 / AN108 / CS4#
D19	P96 / AN106 / POE0# / POE10# / ENCIF09
D20	P95 / AN105 / IRQ13 / MTCLKA / CTS2#
E1	P84 / ETH0_COL / CATLINKACT1 / RXD4
E2	P82 / ETH0_TXEN / ETH1_CRS / TIOCD3 / SCK4 / RTS3# / USB_OVRCUR
E3	PU1 / ETH2_RXC / TIOCA11 / SCK3
E5	PU0 / ETH2_RXER / TIOCA10
E6	PL6 / ETH2_RXD3 / TIOCA9
E7	PL4 / IRQ4 / ETH2_RXD1
E8	PL2 / ETH2_TXEN / TIOCA6 / ADTRG1
E9	PL0 / ETH2_TXD0 / TIOCB9
E10	PK7 / ETH2_TXD2 / TIOCB7
E11	PK6 / ETH2_TXD3 / TIOCB6
E12	PD5 / AN113 / A21 / ETH1_TXD3 / ETH0_TXD0 / TIC0 / SSL20 / MCLK3
E13	P56 / BS# / ETH1_TXER
E14	PD4 / AN112 / ETH2_INT
E15	VCCQ33
E16	PD1 / AN109 / CS1#
E18	P97 / AN107 / IRQ7 / A25 / ADTRG1
E19	P94 / AN104 / IRQ4 / MTCLKB / RTS2# / ENCIF08
E20	P93 / AN103 / MTIOC1A / TIC3 / SCK2 / ENCIF07
F1	PC4 / CATI2CCLK / TCLKH / SCL0
F2	P83 / IRQ11 / ETH0_CRS / CATLINKACT0 / TXD4
F3	P85 / IRQ5 / CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN
F5	PU4 / MII2_MDC / TIOCC9 / CTS3#
F6	VSS

Table 1.6 Pin Assignments (176-Pin HLQFP) (3 / 4)

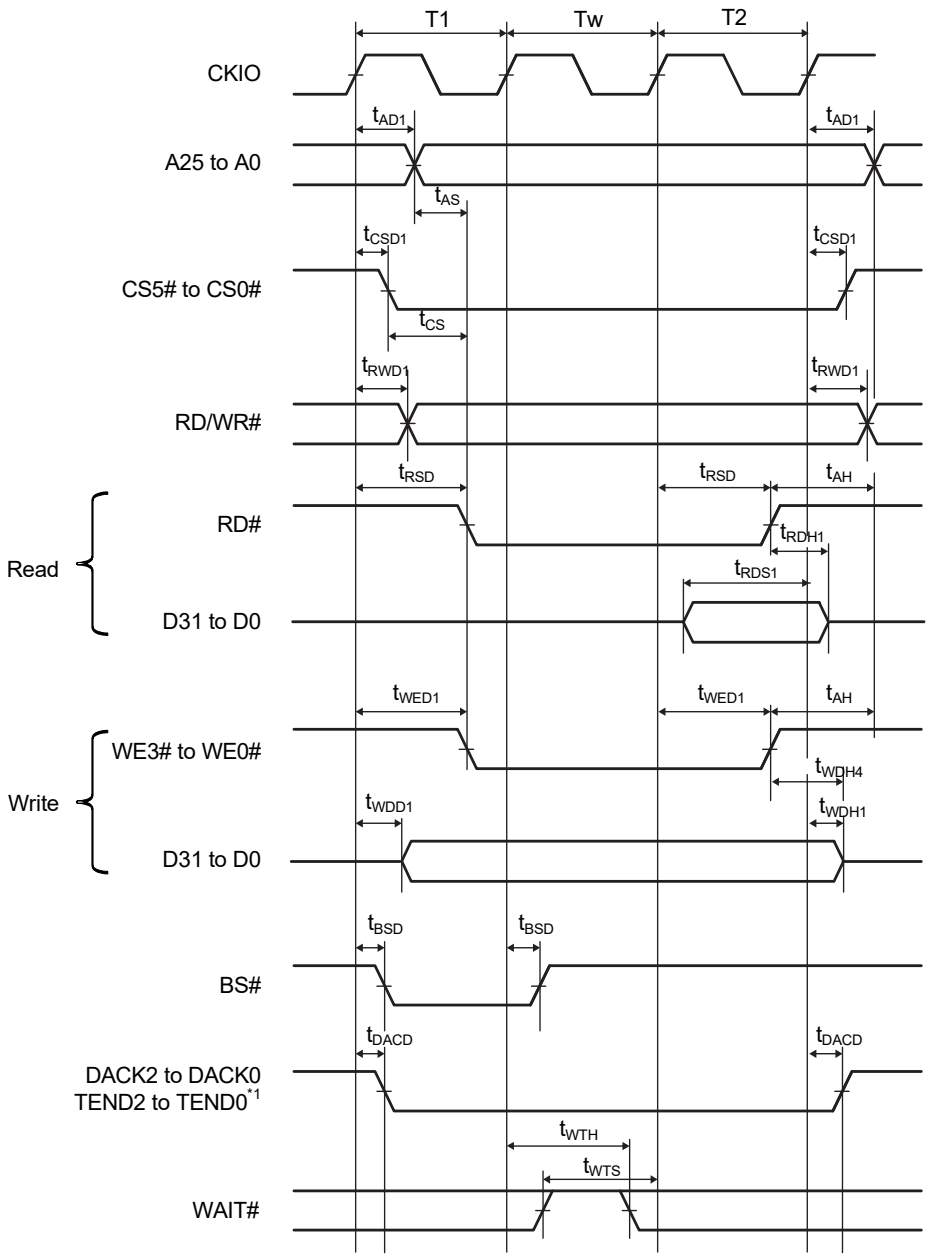
Pin Number	Pin Name
90	P01 / D1 / MTIC5W / TIOCA2
91	P02 / D2 / MTIC5V / TIOCA3
92	VCCQ33
93	P03 / D3 / MTIC5U / TIOCA4
94	P04 / D4 / MTIOC3C / TIOCA5
95	P05 / D5 / MTIOC3A
96	P06 / D6 / MTIOC2B / TIOCB0
97	P07 / D7 / MTIOC2A / TIOCB1
98	PE0 / D8 / MTIOC1B / TIOCB2 / TRACEDATA0
99	PE1 / D9 / MTCLKD / TIOCB3 / SSL03 / TRACEDATA1
100	VSS
101	PE2 / IRQ2 / D10 / MTCLKC / TIOCB4 / SSL02 / TRACEDATA2
102	PE3 / IRQ3 / D11 / MTIOC0D / TIOCB5 / CTS1# / SSL01 / TRACEDATA3
103	PE4 / D12 / MTIOC0B / TIOCC0 / RTS1# / SSL00 / TRACEDATA4
104	PE5 / D13 / MTIOC0C / TIOCC3 / TXD1 / MOSI0 / TRACEDATA5
105	PE6 / IRQ6 / D14 / MTIOC0A / TIOCD0 / RXD1 / MISO0 / TRACEDATA6
106	PE7 / D15 / MTIOC7A / TIOCD3 / POE8# / SCK1 / RSPCK0 / TRACEDATA7
107	VSS
108	VDD
109	P70 / IRQ0 / D16 / MTIOC6D / RTS1# / USB_OVRCUR / TRACECLK
110	P71 / D17 / POE0# / POE10# / TOC2 / SCK1 / TRACECTL
111	P72 / D18 / MTIOC1A / TIC2 / TXD1 / SSITXD0 / TRACEDATA0
112	P73 / IRQ3 / D19 / MTCLKB / RXD1 / SSIRXD0 / TRACEDATA1
113	P74 / D20 / MTCLKA / CTS1# / SSL03 / SSISCK0 / TRACEDATA2
114	P75 / IRQ13 / D21 / MTIOC4D / GTIOC2B / SSL00 / TRACEDATA3
115	P76 / D22 / MTIOC4B / GTIOC2A / SSL01 / SSIWS0 / TRACEDATA4
116	P77 / D23 / MTIOC4C / GTIOC1B / RSPCK0 / TRACEDATA5
117	PA0 / D24 / MTIOC4A / GTIOC1A / MOSI0 / TRACEDATA6 / MDAT3
118	PA1 / D25 / MTIOC3D / GTIOC0B / MISO0 / AUDIO_CLK / TRACEDATA7 / MCLK3
119	VSS
120	VDD
121	PA2 / D26 / MTIOC3B / GTIOC0A / SSL02 / DREQ2 / MDAT2
122	PA3 / D27 / ETHSWSECOUT / GTETRG / TIOCA2 / SCK2 / DACK2 / MCLK2
123	PA4 / D28 / ETH1_INT / TIOCA3 / ADTRG0 / RXD2 / TEND2 / MDAT1
124	PA5 / D29 / ETH0_INT / ETH1_TXER / TIOCA4 / TXD2 / MCLK1
125	PA6 / IRQ6 / D30 / A21 / GTIOC3A / CTS2# / MDAT0
126	VCCQ33
127	PA7 / IRQ7 / D31 / A22 / MTIOC6B / GTIOC3B / RTS2# / MCLK0
128	VDD
129	VSS
130	P13 / RAS# / MTIOC4C / GTIOC1B
131	P14 / CAS# / MTIOC4A / GTIOC1A
132	P15 / CS3# / CKE / MTIOC3D / GTIOC0B
133	P16 / CS4# / CS2# / MTIOC3B / GTIOC0A
134	P17 / CS5# / ETH1_TXER / PHYRESETOUT# / ADTRG0

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
C15								AN000
C16	VREFL0							
C17	VREFH0							
C18		PD2	WAIT#					AN110
C19		P14	CAS#	MTIOC4A / GTIOC1A		ENCIF10		
C20		P13	RAS#	MTIOC4C / GTIOC1B				
D1		P81		TIOCC0	ETH0_RXER / CTS4#			
D2		P80		TIOCC3	ETH0_RXDV / RTS4#		IRQ8	
D3		PU3		TIOCD6	ETH2_COL / TXD3			
D18		PD0	CS4#					AN108
D19		P96		POE0# / POE10#		ENCIF09		AN106
D20		P95		MTCLKA	CTS2#		IRQ13	AN105
E1		P84			ETH0_COL / CATLINKACT1 / RXD4			
E2		P82		TIOCD3	ETH0_TXEN / ETH1_CRS / SCK4 / RTS3# / USB_OVRCUR			
E3		PU1		TIOCA11	ETH2_RXC / SCK3			
E5		PU0		TIOCA10	ETH2_RXER			
E6		PL6		TIOCA9	ETH2_RXD3			
E7		PL4			ETH2_RXD1		IRQ4	
E8		PL2		TIOCA6	ETH2_TXEN			ADTRG1
E9		PL0		TIOCB9	ETH2_TXD0			
E10		PK7		TIOCB7	ETH2_TXD2			
E11		PK6		TIOCB6	ETH2_TXD3			
E12		PD5	A21	TIC0	ETH1_TXD3 / ETH0_TXD0 / SSL20	MCLK3		AN113
E13		P56	BS#		ETH1_TXER			
E14		PD4			ETH2_INT			AN112
E15	VCCQ33							
E16		PD1	CS1#					AN109
E18		P97	A25				IRQ7	ADTRG1 / AN107
E19		P94		MTCLKB	RTS2#	ENCIF08	IRQ4	AN104
E20		P93		MTIOC1A / TIC3	SCK2	ENCIF07		AN103
F1		PC4		TCLKH	CATI2CCLK / SCL0			
F2		P83			ETH0_CRS / CATLINKACT0 / TXD4		IRQ11	

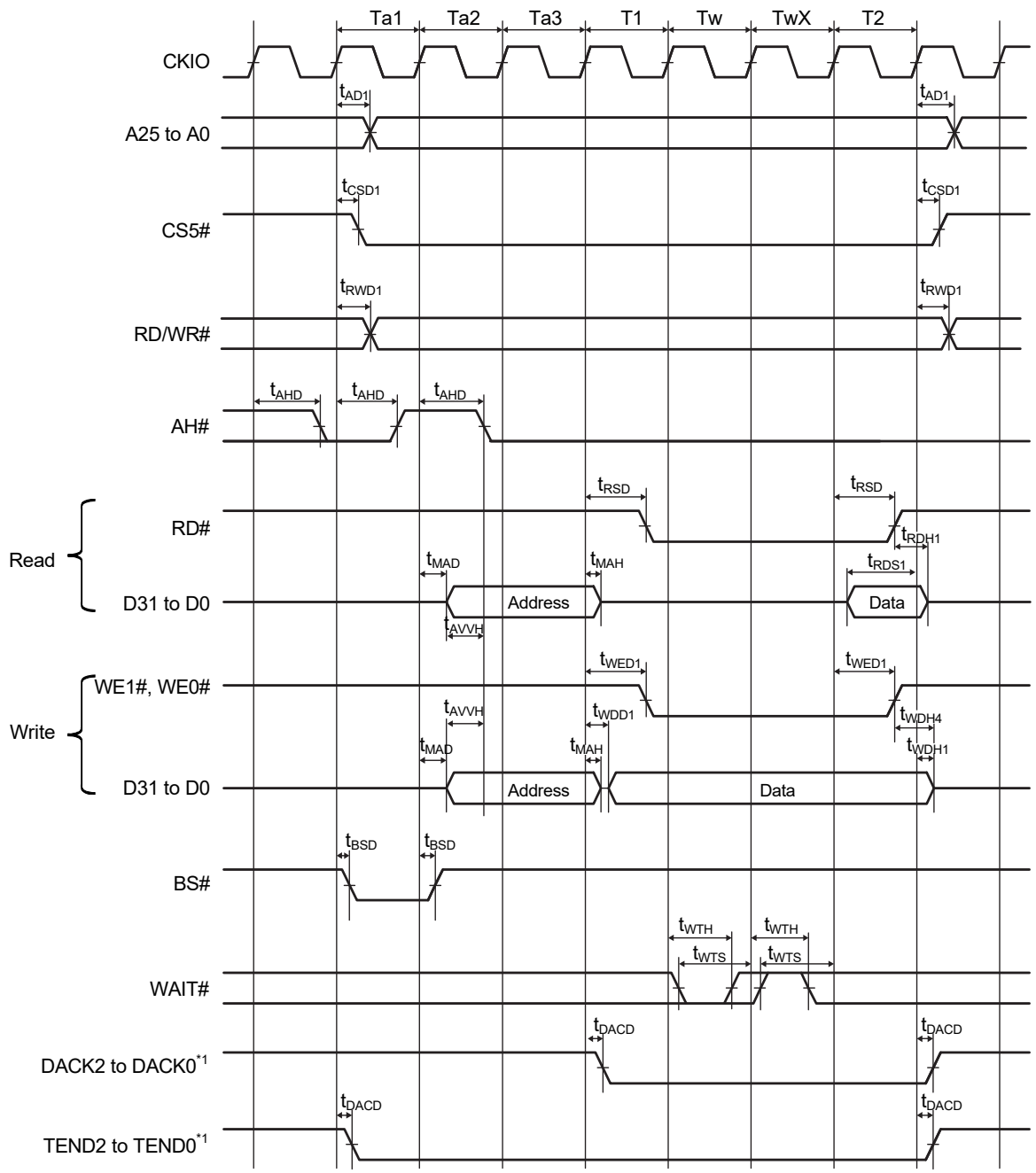
Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
R16	VCCQ33							
R18	VCCQ33							
R19		PS6		TIOCA5 / TIOCB5 / PO23	RXD2	ENCIF06	IRQ14	
R20		PS7		TIOCA4 / TIOCB4 / PO24	TXD2			
T1	DVDD_USB							
T2	VDD33_USB							
T3		P32			USB_OVRCUR		IRQ10	
T5		PC6	DREQ0	TCLKC	SCL1 / CRXD0 / USB_VBUSIN			
T6		P37	WE1#/ DQMLU	PO1				
T7		P36	WE0#/ DQMLL	PO0				
T8		PG3	A4	PO5 / TIC1	MISO1			
T9		PG6	A7	TCLKB / PO8	SSL11			
T10		PH3	A12	MTIOC1B / PO13				
T11	VCCQ33							
T12		PH5	A14	PO15				
T13	VCCQ33							
T14		P26	A19 / DREQ1	MTIOC8D				
T15	VCCQ33							
T16	VSS							
T18	VSS							
T19	TRACEDATA0	PE0	D8	MTIOC1B / TIOCB2				
T20	TRACEDATA1	PE1	D9	MTCLKD / TIOCB3	SSL03			
U1		P60	TEND0		CTXD0 / SPBSSL			
U2		P63			SPBMO/SPBIO0			
U3		PN1		MTIOC8C / PO21	MISO1	ENCIF09		
U18	TRACECTL	P00	D0	MTIOC6A / TIOCA1				ADTRG1
U19		P04	D4	MTIOC3C / TIOCA5				
U20		P03	D3	MTIC5U / TIOCA4				
V1		P61	DACK0		CTXD1 / SPBIO3			
V2		P64			SPBMI/SPBIO1			
V3		PN3		MTIOC8A	RSPCK1			
V4		PN4		MTIOC6C / TIOCC6	SSL11		IRQ12	
V5		PC7		TIC0	SDA1 / CRXD1			
V6		PG1	A2	PO3				
V7		PG4	A5	PO6 / TOC1	MOSI1			
V8		PG5	A6	TCLKA / PO7	SSL10			
V9		PH0	A9	PO10				
V10		PH1	A10	MTIOC2B / PO11				
V11		PH7	A16	MTIC5W				



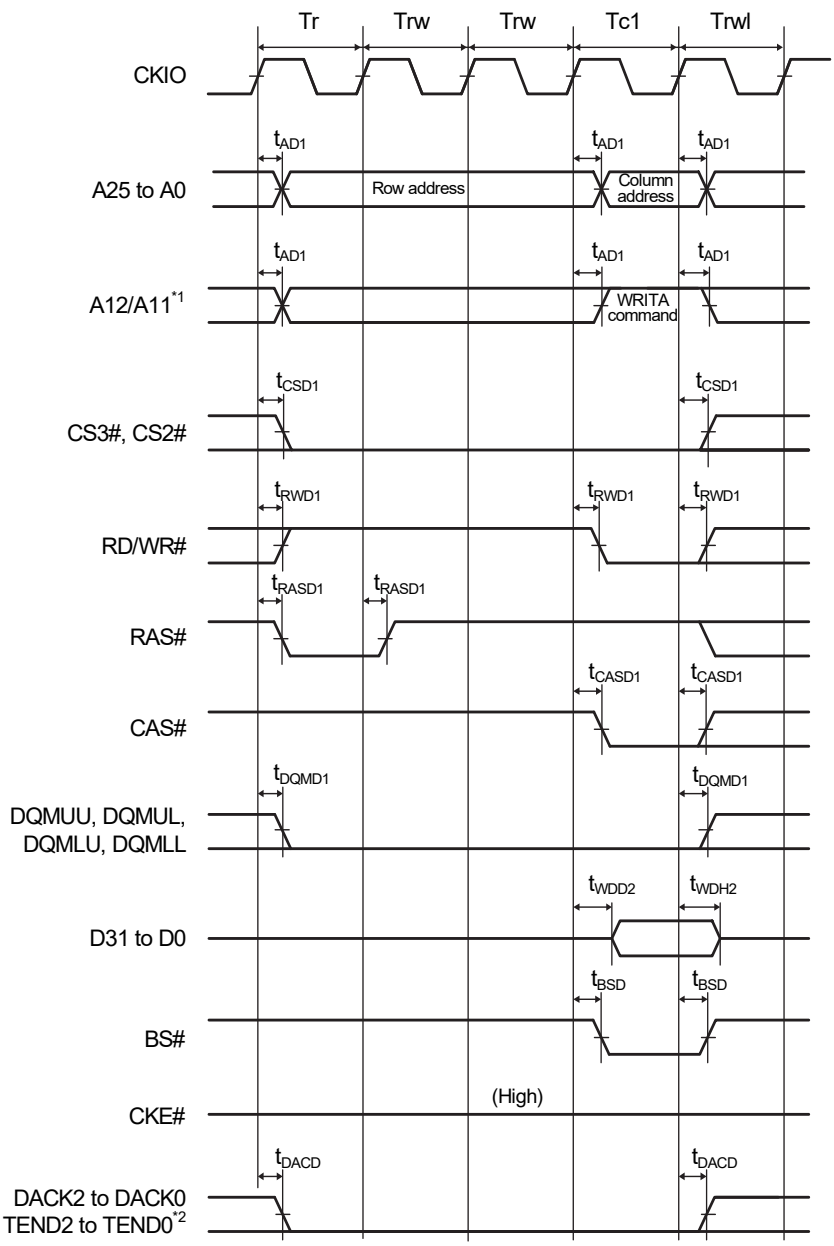
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.13 SRAM Interface Basic Bus Cycle (Software Wait 1)



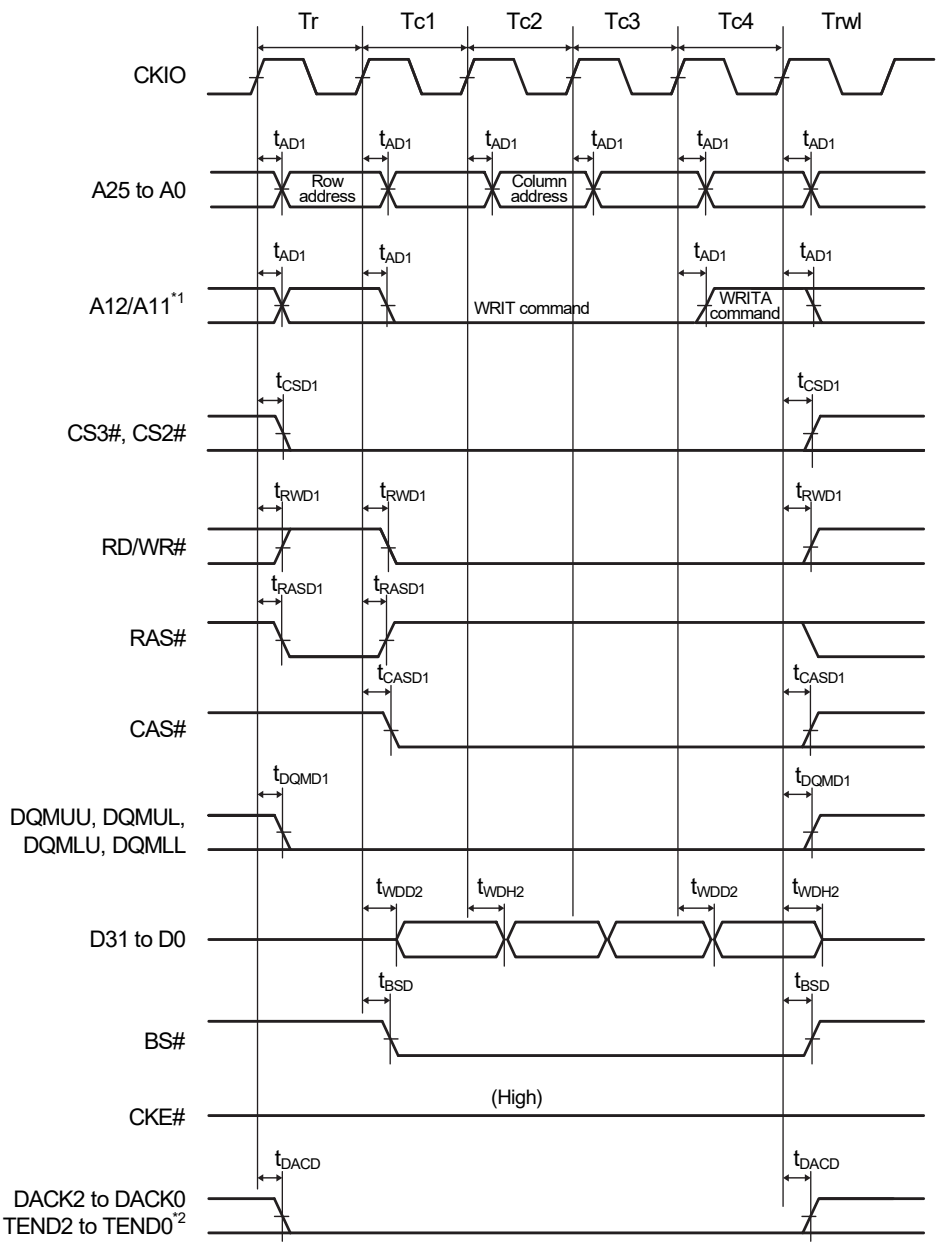
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.16 MPX-I/O Interface Bus Cycle (Address Cycle 3, Software Wait 1, External Wait 1 Inserted)



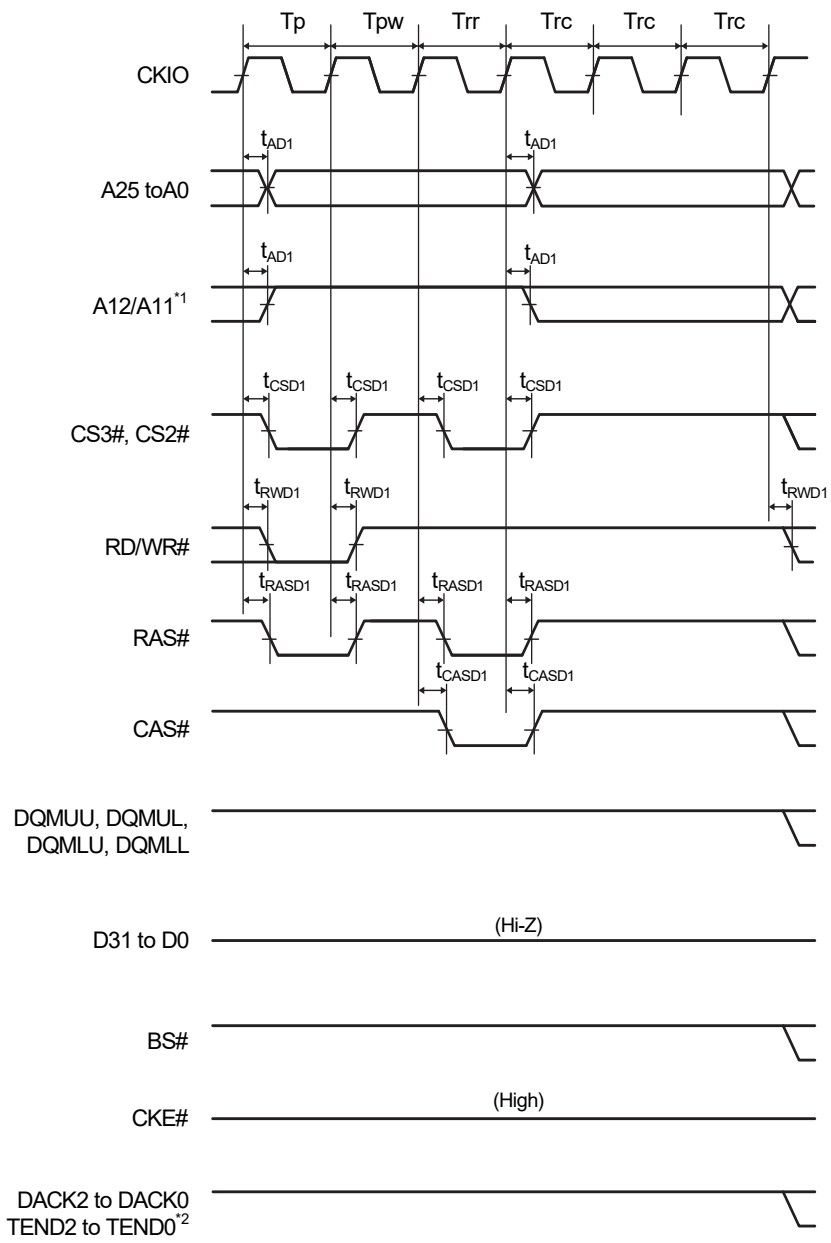
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.25 Synchronous DRAM Single-Write Bus Cycle (with Auto Precharge, WTRCD = 2 Cycles, TRWL = 1 Cycle)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.26 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (with Auto Precharge, WTRCD = 0 Cycles, TRWL = 1 Cycle)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 2.34 Synchronous DRAM Auto-Refresh Timing (WTRP = 1 Cycle, WTRC = 3 Cycles)

2.4.5.7 A/D Converter Trigger Timing

Table 2.25 A/D Converter Trigger Timing

Item			Symbol	min	max	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	ADTRG0	t_{TRGW}	1.5	—	t_{PFcyc}	Figure 2.48
		ADTRG1		1.5		t_{PGcyc}	Figure 2.49

Note 1. t_{PFcyc}: PCLKF cycle, t_{PGcyc}: PCLKG cycle

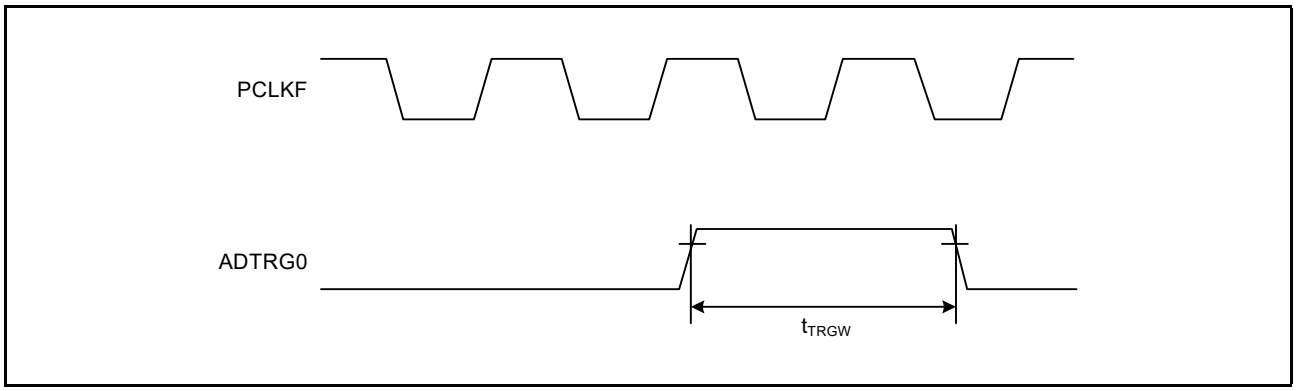


Figure 2.48 A/D Converter Trigger Input Timing (ADTRG0)

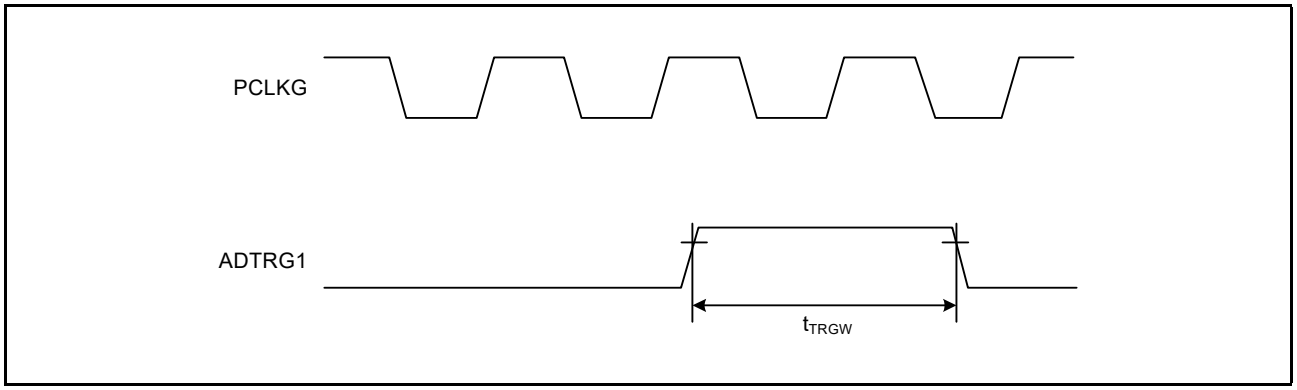


Figure 2.49 A/D Converter Trigger Input Timing (ADTRG1)

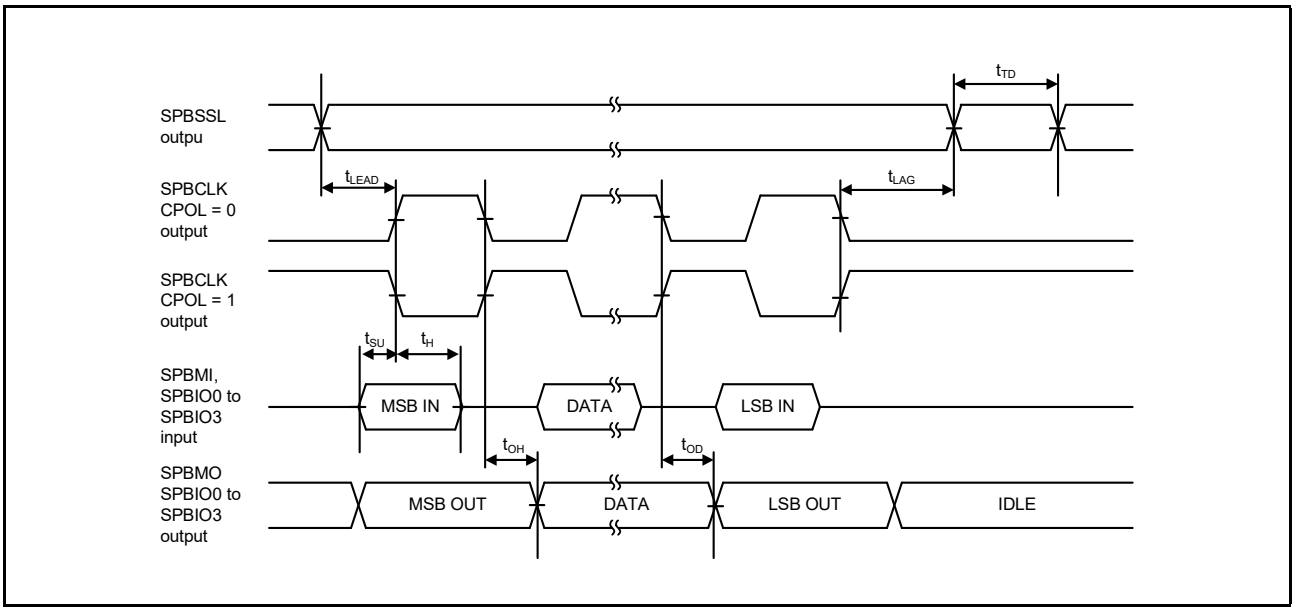


Figure 2.58 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 0)

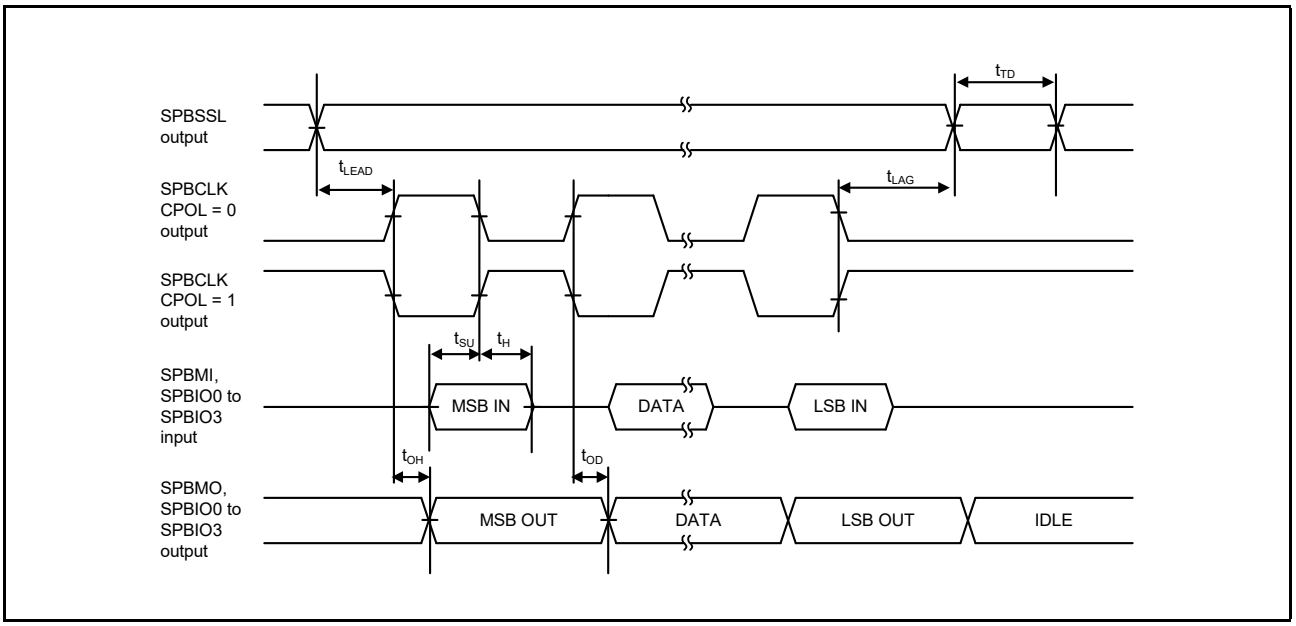


Figure 2.59 SPIBSC Transmit/Receive Timing (CPHAT = 1, CPHAR = 1)

2.4.5.13 CAN Interface Timing

Table 2.31 CAN Interface Timing

Item	Symbol	min	max	Unit	Test Conditions
Internal delay time	tnode	—	100	ns	Figure 2.69
Transmission rate		—	1	Mbps	

Internal delay time (tnode) = Internal transmission delay time (toutput) + Internal reception delay time (tinput)

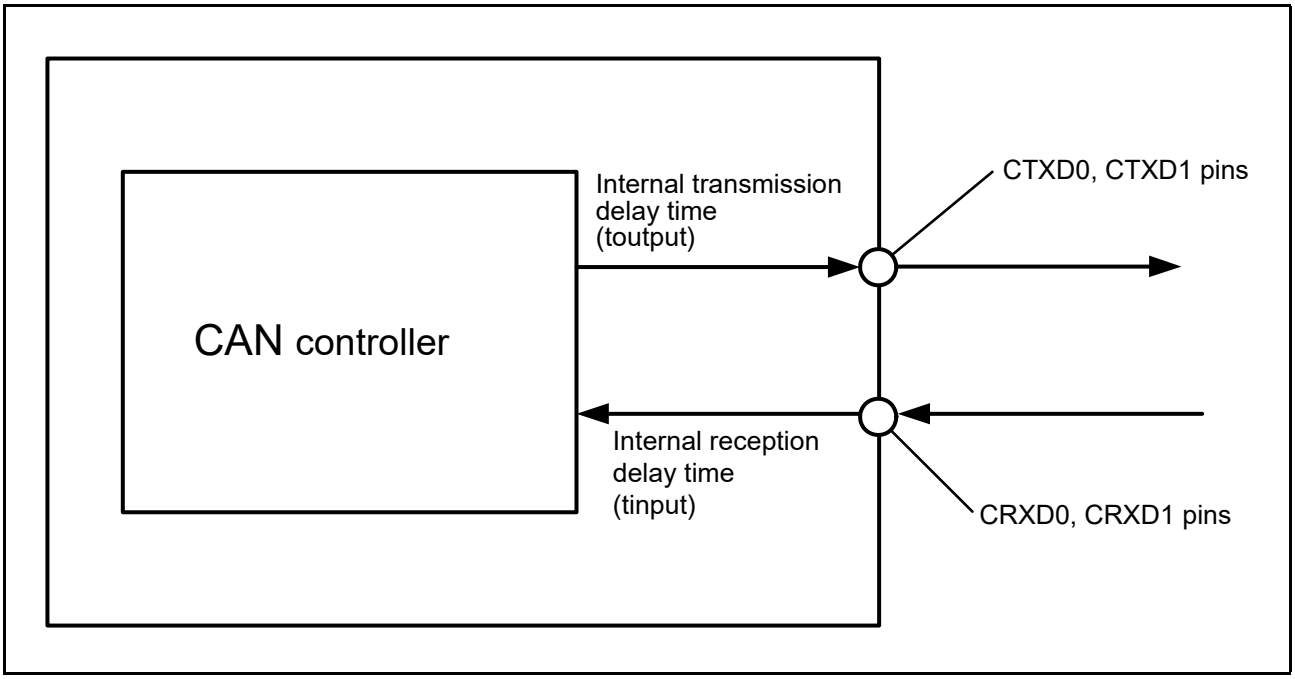


Figure 2.69 CAN Interface Conditions

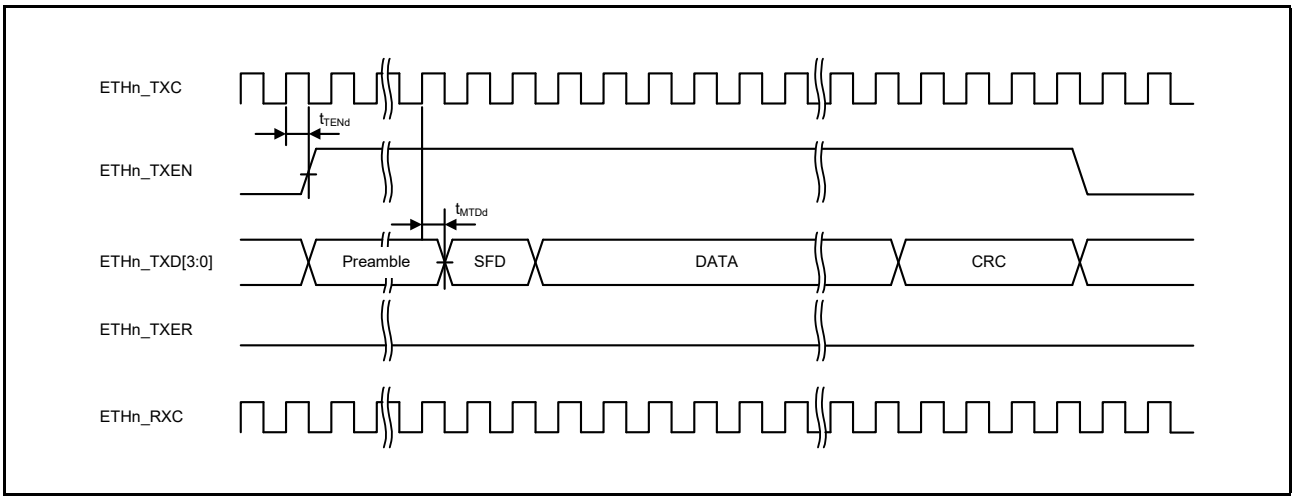


Figure 2.74 MII Transmission Timing

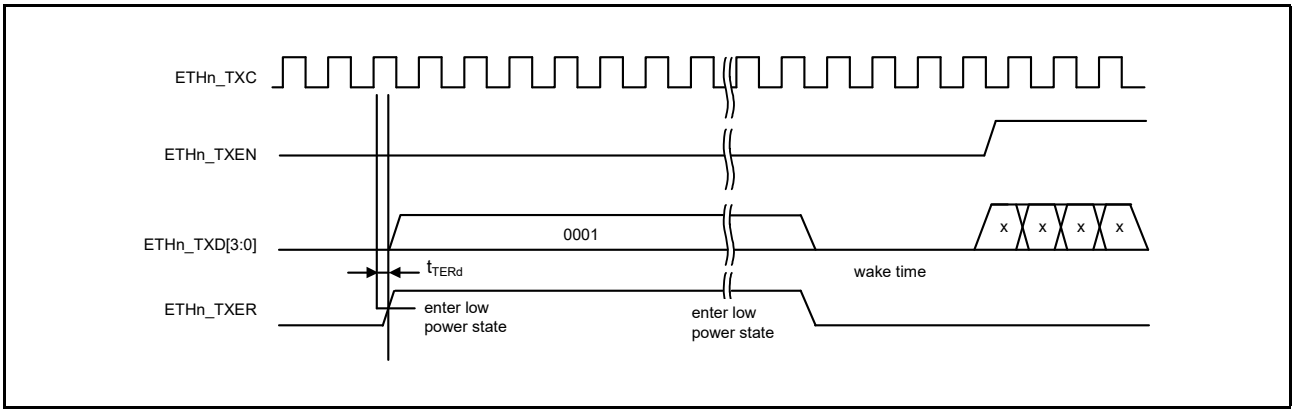


Figure 2.75 MII Transmission Timing

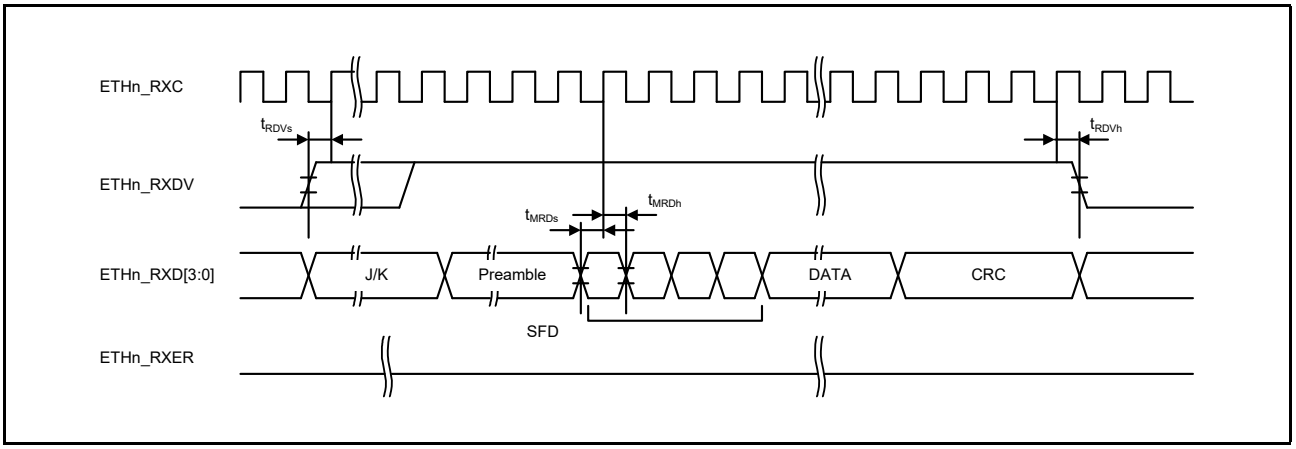


Figure 2.76 MII Reception Timing (Normal Operation)

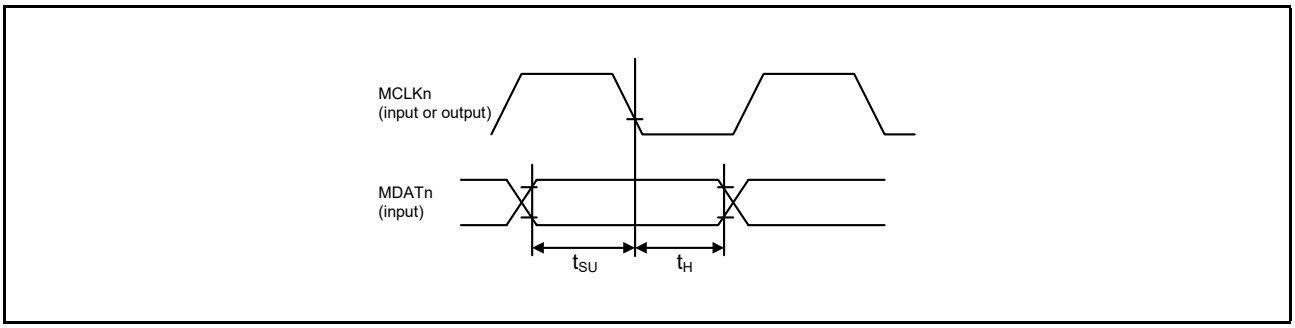


Figure 2.81 Reception Timing (MCLKn Falling Synchronous)

2.9 Debug Interface Timing

Table 2.41 Debug Interface Timing

Output load conditions: V_{OH} = VCCQ33 – 0.5 V, V_{OL1} = 0.4 V

Item	Symbol	Min.	Max.	Unit	Reference Figure
TCK cycle time	t_{TCKcyc}	30	—	ns	Figure 2.87
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	5	—	ns	Figure 2.88 Output load: 30 pF
TDI hold time	t_{TDIH}	5	—	ns	
TMS/SWDIO setup time	t_{TMSS}	5	—	ns	
TMS/SWDIO hold time	t_{TMSH}	5	—	ns	
SWDIO delay time	t_{SWDO}	—	15	ns	
TDO delay time	t_{TDOD}	—	15	ns	
Capture register setup time	t_{CAPTS}	5	—	ns	Figure 2.89
Capture register hold time	t_{CAPTH}	5	—	ns	
Update register delay time	$t_{UPDATED}$	—	15	ns	
Trace clock cycle	t_{TCYC}	26.6	—	ns	Figure 2.90 Output load: 15 pF
Trace data delay time	t_{TDT}	0.25 × t_{TCYC} – 2	0.25 × t_{TCYC} + 2	ns	

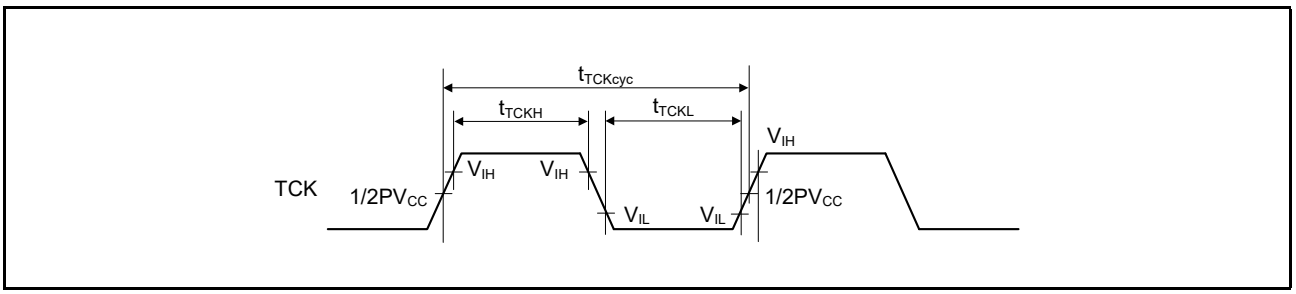


Figure 2.87 TCK Input Timing

Rev.	Date	Description	
		Page	Summary
1.30	Apr. 25, 2017	1. Overview	
		49	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP) (6/6): The communication function of pin 171, modified
		2. Electrical Characteristics	
		107	Figure 2.60 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1): Modified
1.40	Nov. 15, 2017	All	Cortex-R4F changed to Cortex-R4
		Features	
		1	■ Encoder interfaces, changed ■ Various communications interfaces: Features of Ethernet changed
		1. Overview	
		2	1.1 Outline of Specifications: "Cortex®-R4F processor" changed to "Cortex®-R4 processor with FPU"
		8	Table 1.1 Outline of Specifications (7 / 7): Description of the encoder interfaces changed
		16	Table 1.4 Pin Functions (4 / 7): CTS0# to CTS4#: I/O and functional description changed; RTS0# to RTS4#: Functional description changed
		19	Table 1.4 Pin Functions (7 / 7): ENCIF07 to ENCIF12 changed to ENCIF00 to ENCIF12
		22	Table 1.5 Pin Assignments (320-Pin FBGA) (1 / 8): ENCIF12 added to B19; ENCIF11 added to B20
		23	Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8): ENCIF10 added to C19; ENCIF09 added to D19; ENCIF08 added to E19
		24	Table 1.5 Pin Assignments (320-Pin FBGA) (3 / 8): ENCIF11 added to H19; ENCIF12 added to H20
		25	Table 1.5 Pin Assignments (320-Pin FBGA) (4 / 8): ENCIF10 added to J19
		26	Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8): ENCIF09 added to N20; ENCIF08 added to P20
		27	Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8): ENCIF09 added to U3
		28	Table 1.5 Pin Assignments (320-Pin FBGA) (7 / 8): ENCIF10 added to W3; ENCIF11 added to W4; ENCIF08 added to W10; ENCIF12 added to Y4
		35	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (2 / 10): ENCIF12 added to B19 under "Others"; ENCIF11 added to B20 under "Others"
		36	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10): ENCIF10 added to C19 under "Others"; ENCIF09 added to D19 under "Others"; ENCIF08 added to E19 under "Others"
		38	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (5 / 10); ENCIF11 added to H19 under "Others"; ENCIF12 added to H20 under "Others"; ENCIF10 added to J19 under "Others"
		40	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10): ENCIF09 added to N20 under "Others"; ENCIF08 added to P20 under "Others"
		41	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10): ENCIF09 added to U3 under "Others"
		42	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10): ENCIF10 added to W3 under "Others"; ENCIF11 added to W4 under "Others"; ENCIF08 added to W10 under "Others; ENCIF12 added to Y4
		2. Electrical Characteristics	
		65, 66	Table 2.17 Bus Timing: "CKIO = 75MHz" changed to "CKIO = 1/tCKcyc; "tcyc" changed to "tCKcyc"; entries for "Address delay time 1", "CS# delay time 1", "Read/write delay time 1", "Read data setup time 1 to 3" and "WAIT# setup time" changed; Notes 1, 3, and 4 changed
		102	Table 2.27 RSPIa Timing: Note 2 changed (SSLND → SPCKD): Note 3 added
		111	Figure 2.64 RIICa Bus Interface Input/Output Timing: SDA0 to SDA3 and SCL0 to SCL3 deleted

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.