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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	44
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70j19a-an

1. Configuration Summary

The SAM E70/S70/V70/V71 devices differ in memory size, package and features. The following tables summarize the different configurations.

Table 1-1. SAM V71 Family Features (With CAN-FD, Ethernet AVB and Media LB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																					Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Ethernet AVB	Media LB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
SAMV71Q19	512	256	144	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	Y	12 - bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAMV71Q20	1024	384																										
SAMV71Q21	2048																											
SAMV71N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	Y	12 - bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAMV71N20	1024	384																										
SAMV71N21	2048																											
SAMV71J19	512	256	64	LQFP	FS	2/3	SPI only	0	2	N	1	RMII	Y	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAMV71J20	1024	384																										
SAMV71J21	2048																											

Note: HS = High-Speed; FS = Full-Speed.

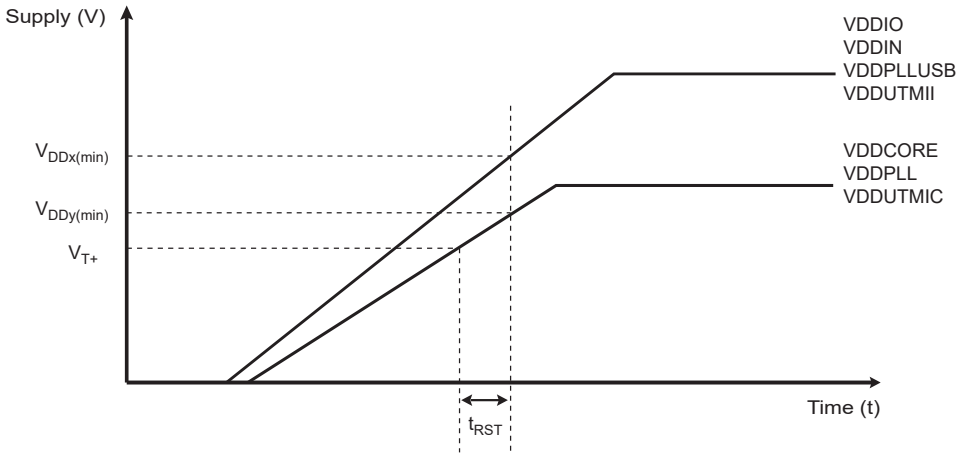
Table 1-2. SAM E70 Family Features (With CAN-FD and Ethernet AVB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																				Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Ethernet AVB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
SAME70Q19	512	256	144	LQFP, LFBGA, UFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAME70Q20	1024	384																									
SAME70Q21	2048																										
SAME70N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAME70N20	1024	384																									
SAME70N21	2048																										
SAME70J19	512	256	64	LQFP	FS	2/3	SPI only	0	2	N	1	RMII	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAME70J20	1024	384																									
SAME70J21	2048																										

Note: HS = High-Speed; FS = Full-Speed.

In order to prevent any overcurrent at powerup, it is required that VREFP rises simultaneously with VDDIO and VDDIN.

Figure 7-1. Powerup Sequence



Related Links

58.2 DC Characteristics

23.4.6 Backup Power Supply Reset

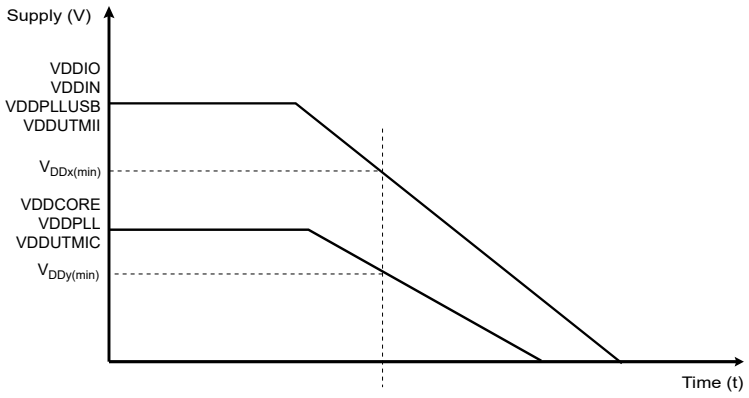
23.4.6.1 Raising the Backup Power Supply

7.2.2 Powerdown

If VDDCORE, VDDPLL and VDDUTMIC are not supplied by the embedded voltage regulator, VDDIO, VDDIN, VDDPLLUSB and VDDUTMII should fall simultaneously, prior to VDDCORE, VDDPLL and VDDUTMIC falling. The VDDCORE falling slope must not be faster than 20V/ms.

In order to prevent any overcurrent at powerdown, it is required that VREFP falls simultaneously with VDDIO and VDDIN.

Figure 7-2. Powerdown Sequence



7.3 Voltage Regulator

The SAM E70/S70/V70/V71 embeds a voltage regulator that is managed by the Supply Controller.

For adequate input and output power supply decoupling/bypassing, refer to 58.2 DC Characteristics in the Electrical Characteristics chapter.

Value	Name	Description
4	16BEAT_BURST	16-beat Burst—The undefined length burst or bursts sequence is split into 16-beat bursts or less, allowing re-arbitration every 16 beats.
5	32BEAT_BURST	32-beat Burst —The undefined length burst or bursts sequence is split into 32-beat bursts or less, allowing re-arbitration every 32 beats.
6	64BEAT_BURST	64-beat Burst—The undefined length burst or bursts sequence is split into 64-beat bursts or less, allowing re-arbitration every 64 beats.
7	128BEAT_BURST	128-beat Burst—The undefined length burst or bursts sequence is split into 128-beat bursts or less, allowing re-arbitration every 128 beats. Note: Unless duly needed, the ULBT should be left at its default 0 value for power saving.

Bit 5 – SYSIO5 PB5 or TDO/TRACESWO Assignment

Value	Description
0	TDO/TRACESWO function selected.
1	PB5 function selected.

Bit 4 – SYSIO4 PB4 or TDI Assignment

Value	Description
0	TDI function selected.
1	PB4 function selected.

31.20.20 PMC Fault Output Clear Register

Name: PMC_FOCR
Offset: 0x0078
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

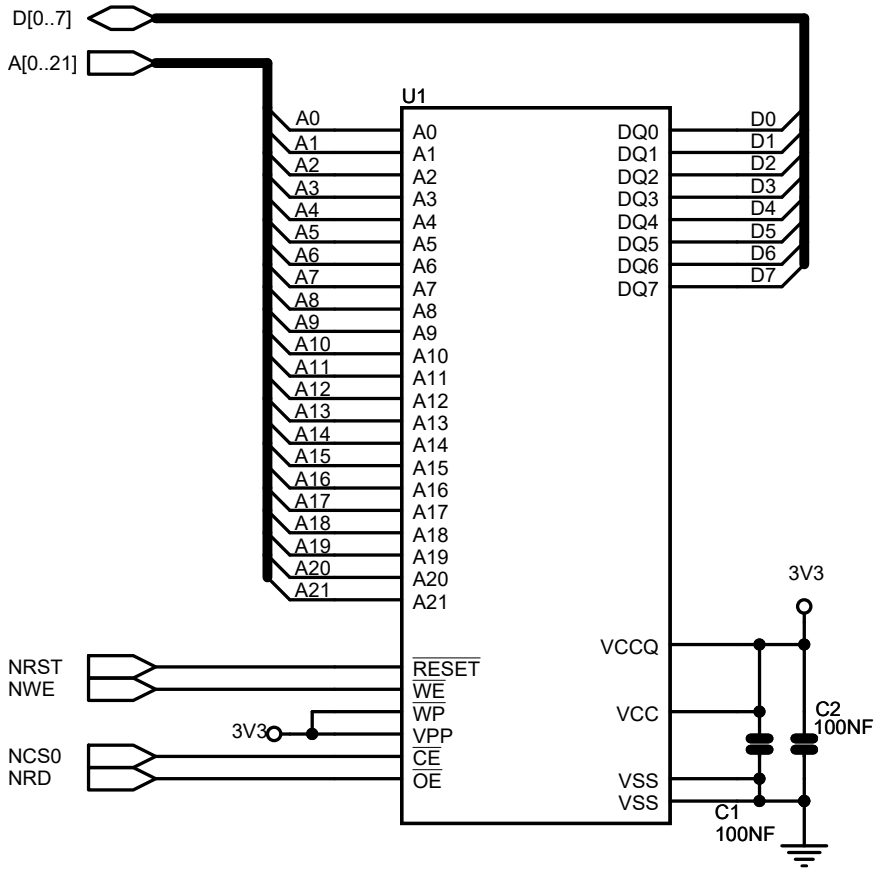
Bit	7	6	5	4	3	2	1	0
Access								
Reset								FOCLR

Bit 0 – FOCLR Fault Output Clear
Clears the clock failure detector fault output.

35.8.1.2 NOR Flash

Hardware Configuration

Figure 35-8. NOR Flash



Software Configuration

Configure the SMC CS0 Setup, Pulse, Cycle, and Mode, depending on Flash timings and system bus frequency.

35.9 Standard Read and Write Protocols

In the following sections, the byte access type is not considered. Byte select lines (NBS0 to NBS1) always have the same timing as the A address bus. NWE represents either the NWE signal in byte select access type or one of the byte write lines (NWR0 to NWR1) in byte write access type. NWR0 to NWR1 have the same timings and protocol as NWE. If D[15:8] are used, they have the same timing as D[7:0]. In the same way, NCS represents one of the NCS[0..3] chip select lines.

35.9.1 Read Waveforms

The read cycle is shown in the following figure.

The read cycle starts with the address setting on the memory address bus.

Offset	Name	Bit Pos.								
		15:8								
		23:16								
		31:24								
0x05D8	XDMAC_CIM22	7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
		23:16								
		31:24								
0x05DC	XDMAC_CIS22	7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
		23:16								
		31:24								
0x05E0	XDMAC_CSA22	7:0	SA[7:0]							
		15:8	SA[15:8]							
		23:16	SA[23:16]							
		31:24	SA[31:24]							
0x05E4	XDMAC_CDA22	7:0	DA[7:0]							
		15:8	DA[15:8]							
		23:16	DA[23:16]							
		31:24	DA[31:24]							
0x05E8	XDMAC_CNDA22	7:0	NDA[5:0]							NDAIF
		15:8	NDA[13:6]							
		23:16	NDA[21:14]							
		31:24	NDA[29:22]							
0x05EC	XDMAC_CNDC22	7:0				NDVIEW[1:0]		NDDUP	NDSUP	NDE
		15:8								
		23:16								
		31:24								
0x05F0	XDMAC_CUBC22	7:0	UBLEN[7:0]							
		15:8	UBLEN[15:8]							
		23:16	UBLEN[23:16]							
		31:24								
0x05F4	XDMAC_CBC22	7:0	BLEN[7:0]							
		15:8					BLEN[11:8]			
		23:16								
		31:24								
0x05F8	XDMAC_CC22	7:0	MEMSET	SWREQ		DSYNC		MBSIZE[1:0]		TYPE
		15:8		DIF	SIF	DWIDTH[1:0]		CSIZE[2:0]		
		23:16	WRIP	RDIP	INITD		DAM[1:0]		SAM[1:0]	
		31:24		PERID[6:0]						
0x05FC	XDMAC_CDS_MSP22	7:0	SDS_MSP[7:0]							
		15:8	SDS_MSP[15:8]							
		23:16	DDS_MSP[7:0]							
		31:24	DDS_MSP[15:8]							
0x0600	XDMAC_CSUS22	7:0	SUBS[7:0]							
		15:8	SUBS[15:8]							
		23:16	SUBS[23:16]							

36.9.10 XDMAC Global Channel Status Register

Name: XDMAC_GS
Offset: 0x24
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – ST XDMAC Channel x Status

Value	Description
0	This bit indicates that the channel x is disabled.
1	This bit indicates that the channel x is enabled. If a channel disable request is issued, this bit remains asserted until pending transaction is completed.

36.9.23 XDMAC Channel x Destination Address Register [x = 0..23]

Name: XDMAC_CDA
Offset: 0x64 + n*0x40 [n=0..23]
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	DA[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DA[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DA[31:0] Channel x Destination Address
Program this register with the destination address of the DMA transfer.

A configuration error is generated when this address is not aligned with the transfer data size.

Offset	Name	Bit Pos.								
0x07A8	GMAC_ST2CW021	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x07AC	GMAC_ST2CW121	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x07B0	GMAC_ST2CW022	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x07B4	GMAC_ST2CW122	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x07B8	GMAC_ST2CW023	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x07BC	GMAC_ST2CW123	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								

38.8.91 GMAC PTP Event Frame Received Seconds Low Register

Name: GMAC_EFRSL
Offset: 0x1E8
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	RUD[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RUD[31:0] Register Update
The register is updated with the value that the IEEE 1588 Timer Seconds Register holds when the SFD of a PTP receive primary event crosses the MII interface. An interrupt is issued when the register is updated.

Source Clock (MHz)	Expected Baud Rate (bit/s)	Calculation Result	CD	Actual Baud Rate (bit/s)	Error
8,000,000	38,400	13.02	13	38,461.54	0.16%
12,000,000	38,400	19.53	20	37,500.00	2.40%
12,288,000	38,400	20.00	20	38,400.00	0.00%
14,318,180	38,400	23.30	23	38,908.10	1.31%
14,745,600	38,400	24.00	24	38,400.00	0.00%
18,432,000	38,400	30.00	30	38,400.00	0.00%
24,000,000	38,400	39.06	39	38,461.54	0.16%
24,576,000	38,400	40.00	40	38,400.00	0.00%
25,000,000	38,400	40.69	40	38,109.76	0.76%
32,000,000	38,400	52.08	52	38,461.54	0.16%
32,768,000	38,400	53.33	53	38,641.51	0.63%
33,000,000	38,400	53.71	54	38,194.44	0.54%
40,000,000	38,400	65.10	65	38,461.54	0.16%
50,000,000	38,400	81.38	81	38,580.25	0.47%
60,000,000	38,400	97.66	98	38,265.31	0.35%
70,000,000	38,400	113.93	114	38,377.19	0.06%

In this example, the baud rate is calculated with the following formula:

$$\text{Baud Rate} = \text{Selected Clock}/\text{CD} \times 16$$

The baud rate error is calculated with the following formula. It is not recommended to work with an error higher than 5%.

$$\text{Error} = 1 - \left(\frac{\text{Expected Baud Rate}}{\text{Actual Baud Rate}}\right)$$

46.6.1.2 Fractional Baud Rate in Asynchronous Mode

The baud rate generator is subject to the following limitation: the output frequency changes only by integer multiples of the reference frequency. An approach to this problem is to integrate a fractional N clock generator that has a high resolution. The generator architecture is modified to obtain baud rate changes by a fraction of the reference source clock. This fractional part is programmed using US_BRGR.FP. If FP is not 0, the fractional part is activated. The resolution is one-eighth of the clock divider. The fractional baud rate is calculated using the following formula:

$$\text{Baud Rate} = \frac{\text{Selected Clock}}{\left(8(2 - \text{OVER})\left(\text{CD} + \frac{\text{FP}}{8}\right)\right)}$$

The modified architecture is presented in the following figure.

46.7.19 USART Channel Status Register (LIN_MODE)

Name: US_CSR (LIN_MODE)
Offset: 0x0014
Reset: 0x0
Property: Read-only

This configuration is relevant only if USART_MODE = 0xA or 0xB in the USART Mode Register.

Bit	31	30	29	28	27	26	25	24
	LINHTE	LINSTE	LINSNRE	LINCE	LINIPE	LINISFE	LINBE	
Access								
Reset	0	0	0	0	0	0	0	

Bit	23	22	21	20	19	18	17	16
	LINBLS							
Access								
Reset	0							

Bit	15	14	13	12	11	10	9	8
	LINTC	LINID	LINBK				TXEMPTY	TIMEOUT
Access								
Reset	0	0	0				0	0

Bit	7	6	5	4	3	2	1	0
	PARE	FRAME	OVRE				TXRDY	RXRDY
Access								
Reset	0	0	0				0	0

Bit 31 – LINHTE LIN Header Timeout Error (cleared by writing a one to bit US_CR.RSTSTA)

Value	Description
0	No LIN header timeout error has been detected since the last RSTSTA.
1	A LIN header timeout error has been detected since the last RSTSTA.

Bit 30 – LINSTE LIN Synch Tolerance Error (cleared by writing a one to bit US_CR.RSTSTA)

Value	Description
0	No LIN synch tolerance error has been detected since the last RSTSTA.
1	A LIN synch tolerance error has been detected since the last RSTSTA.

Bit 29 – LINSNRE LIN Slave Not Responding Error (cleared by writing a one to bit US_CR.RSTSTA)

Value	Description
0	No LIN slave not responding error has been detected since the last RSTSTA.
1	A LIN slave not responding error has been detected since the last RSTSTA.

Bit 28 – LINCE LIN Checksum Error (cleared by writing a one to bit US_CR.RSTSTA)

0: Received frame matching filter index FIDX.

1: Received frame did not match any Rx filter element.

• R1 Bits 30:24 FIDX[6:0]: Filter Index

0-127: Index of matching Rx acceptance filter element (invalid if ANMF = '1').
Range is 0 to MCAN_SIDFC.LSS - 1 resp. MCAN_XIDFC.LSE - 1.

• R1 Bit 21 FDF: FD Format

0: Standard frame format.

1: CAN FD frame format (new DLC-coding and CRC).

• R1 Bit 20 BRS: Bit Rate Switch

0: Frame received without bit rate switching.

1: Frame received with bit rate switching.

Note:
Bits ESI, FDF, and BRS are only evaluated when CAN FD operation is enabled (MCAN_CCCR.FDOE = 1). Bit BRS is only evaluated when in addition MCAN_CCCR.BRSE = 1.

• R1 Bits 19:16 DLC[3:0]: Data Length Code

0-8: CAN + CAN FD: received frame has 0-8 data bytes.

9-15: CAN: received frame has 8 data bytes.

9-15: CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.

• R1 Bits 15:0 RXTS[15:0]: Rx Timestamp

Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC.TCP.

• R2 Bits 31:24 DB3[7:0]: Data Byte 3

• R2 Bits 23:16 DB2[7:0]: Data Byte 2

• R2 Bits 15:8 DB1[7:0]: Data Byte 1

• R2 Bits 7:0 DB0[7:0]: Data Byte 0

• R3 Bits 31:24 DB7[7:0]: Data Byte 7

• R3 Bits 23:16 DB6[7:0]: Data Byte 6

• R3 Bits 15:8 DB5[7:0]: Data Byte 5

• R3 Bits 7:0 DB4[7:0]: Data Byte 4

... ...

• Rn Bits 31:24 DBm[7:0]: Data Byte m

• Rn Bits 23:16 DBm-1[7:0]: Data Byte m-1

• Rn Bits 15:8 DBm-2[7:0]: Data Byte m-2

• Rn Bits 7:0 DBm-3[7:0]: Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_RXESC), between two and sixteen 32-bit words (Rn = 3 ..17) are used for storage of a CAN message's data field.

Figure 51-25. Event Line Block Diagram

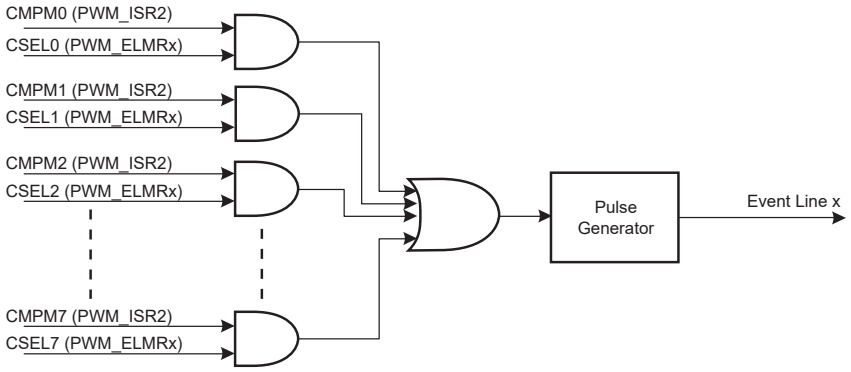
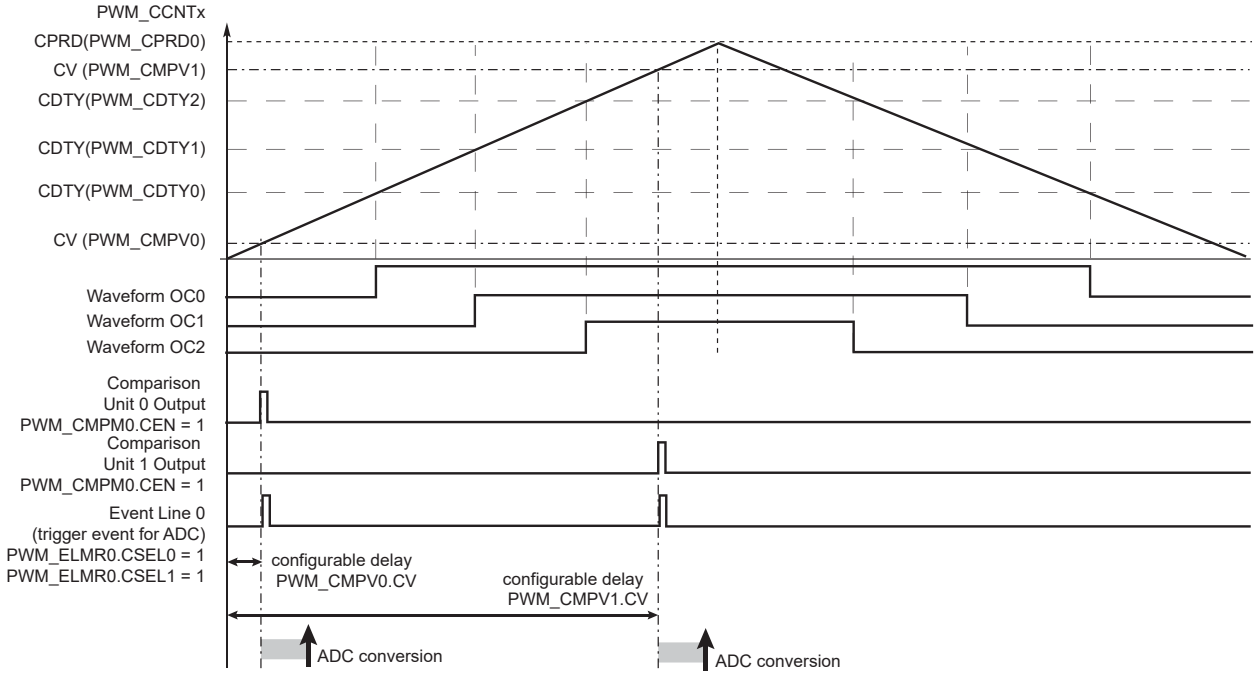


Figure 51-26. Event Line Generation Waveform (Example)



51.6.5 PWM External Trigger Mode

The PWM channels 1 and 2 can be configured to use an external trigger for generating specific PWM signals. The external trigger source can be selected through the bit TRGSRC of the PWM External Trigger Register (see the table below).

Table 51-5. External Event Source Selection

Channel	Trigger Source Selection	Trigger Source
1	PWM_ETRG1.TRGSRC = 0	From PWMEXTRG1 input
	PWM_ETRG1.TRGSRC = 1	From Analog Comparator Controller
2	PWM_ETRG2.TRGSRC = 0	From PWMEXTRG2 input
	PWM_ETRG2.TRGSRC = 1	From Analog Comparator Controller

Each external trigger source can be filtered by writing a one to the TRGFILT bit in the corresponding PWM External Trigger Register (PWM_ETRGx).

51.7.45 PWM Channel Counter Register

Name: PWM_CCNTx
Offset: 0x0214 + x*0x20 [x=0..3]
Reset: 0x00000000
Property: Read-only

Only the first 16 bits (channel counter size) are significant.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CNT[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

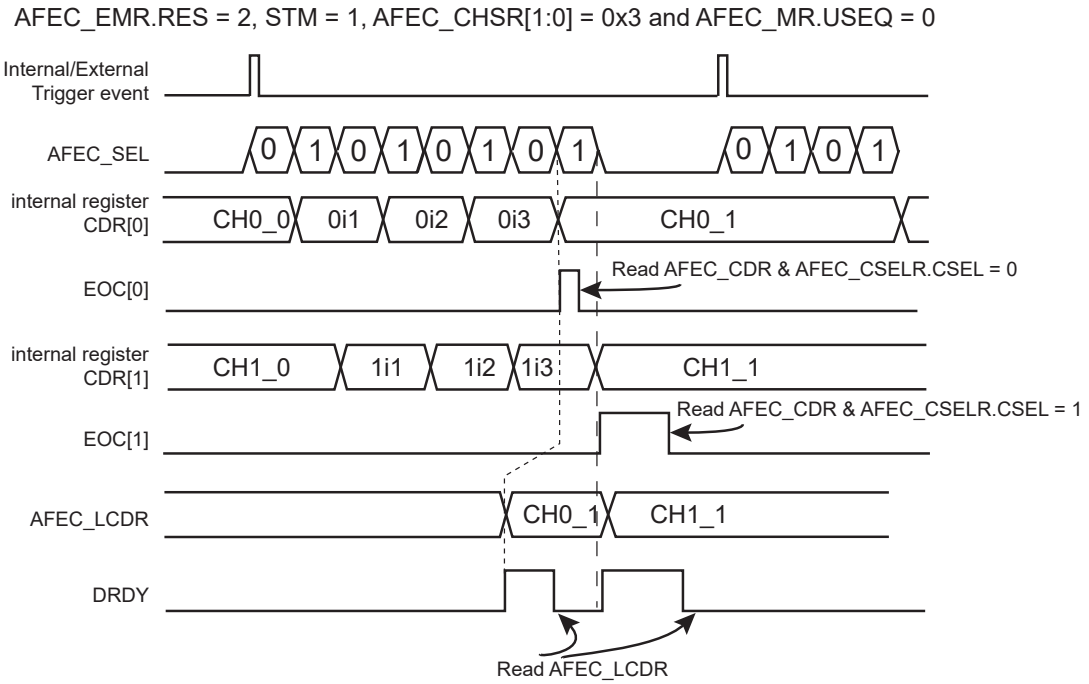
Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – CNT[23:0] Channel Counter Register
Channel counter value. This register is reset when:

• the channel is enabled (writing CHIDx in the PWM_ENA register).

• the channel counter reaches CPRD value defined in the PWM_CPRDx register if the waveform is left-aligned.

Figure 52-12. Digital Averaging Function Waveforms on a Single Trigger Event



Note: 0i1, 0i2, 0i3, 1i1, 1i2, 1i3 are intermediate results and CH0/1_0/1 are final result of average function.

When USEQ is set, the user can define the channel sequence to be converted by configuring AFEC_SEQxR and AFEC_CHER so that channels are not interleaved during the averaging period. Under these conditions, a sample is defined for each end of conversion as described in the figure below.

Therefore, if the same channel is configured to be converted four times consecutively and AFEC_EMR.RES = 2, the averaging result is placed in the corresponding channel internal data register (read by means of the AFEC_CDR) and the AFEC_LCDR for each trigger event.

In this case, the AFE real sample rate remains the maximum AFE sample rate divided by 4.

When USEQ is set and the RES field enables the Enhanced Resolution mode, it is important to note that the user sequence must be a sequence being an integer multiple of 4 (i.e., the number of the enabled channel in the Channel Status register (AFEC_CHSR) must be an integer multiple of 4 and the AFEC_SEQxR must be a series of 4 times the same channel index).

52.7.27 AFEC Channel Error Correction Register

Name: AFEC_CECR
Offset: 0xD8
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the AFEC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					ECORR11	ECORR10	ECORR9	ECORR8
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ECORR7	ECORR6	ECORR5	ECORR4	ECORR3	ECORR2	ECORR1	ECORR0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – ECORRx Error Correction Enable for Channel x

Value	Description
0	Automatic error correction is disabled for channel x.
1	Automatic error correction is enabled for channel x.

59.4 Oscillator Characteristics

59.4.1 32 kHz RC Oscillator Characteristics

Table 59-18. 32 kHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	–	20	32	57	kHz
t_{START}	Startup Time	–	–	–	120	µs
I_{DDON}	Current Consumption	After startup time	–	540	–	nA

59.4.2 4/8/12 MHz RC Oscillator

The 4/8/12 MHz RC oscillator is calibrated in production. This calibration can be read through the Get CALIB Bit command (refer to 22. Enhanced Embedded Flash Controller (EEFC)) and the frequency can be trimmed by software through the PMC.

Table 59-19. 4/8/12 RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ACC_4	4 MHz Total Accuracy(2)	4 MHz output selected (see **Note 1**)	-35	–	46	%
		4 MHz output selected at 25°C (see **Notes 1, 3**)	-1.2	–	0.8	%
ACC_8	8 MHz Total Accuracy	8 MHz output selected at 25°C (see **Notes 1, 3**)	-1.2	–	0.8	%
ACC_{12}	12 MHz Total Accuracy	12 MHz output selected at 25°C (see **Notes 1, 3**)	-1.6	–	0.8	%
	Temp dependency	(see **Note 3**)	–	0.07	0.12	%/°C
t_{START}	Startup Time	–	–	–	20	µs

Note:

1. Frequency range can be configured in the Supply Controller registers.
2. Not trimmed from factory.
3. After trimming at 25°C and VDDCORE = 1.2V.

59.4.3 32.768 kHz Crystal Oscillator Characteristics

Table 59-20. 32.768 kHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN32 Clock Frequency	(see **Note**)	–	–	32	kHz
t_{CHXIN}	XIN32 Clock High Half-period	(see **Note**)	15	–	–	ns
t_{CLXIN}	XIN32 Clock Low Half-period	(see **Note**)	15	–	–	ns

Table 59-47. Static Performance Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
INL	Integral Non-linearity (see **Note 1**)	No R_{LOAD}	-10	±2	10	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
DNL	Differential Non-linearity (see **Note 1**)	No R_{LOAD}	-4	±2	4	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
E_O	Offset Error (see **Note 2**)	–	-8	1	8	mV
E_G	Gain Error	No R_{LOAD}	-1	–	1	%.FSR
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				

Note:

1. Best-fit Curve from 0x080 to 0xF7F.
2. Difference between DACx at 0x800 and V_{VREFP}/2.

Table 59-48. Dynamic Performance Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{START}	Startup Time	From DAC on (CHER.CHx) to DAC ready to convert (CHSR.DACRDYx)	–	10	–	µs
t_S	Settling Time Code to Code; i.e., code(n-1) to code(n) ± 0.5 LSB	R_{LOAD} = 5 Kohm C_{LOAD} = 50 pF	–	0.5	–	µs
	Settling Time Full-scale; i.e., 0x000 to 0xFFF ±0.5 LSB	DACC_ACR.IBCTLCHx = 3 FS = 1 MSps	–	1	–	µs
Slew Rate		–	3	–	V/µs	

Table 59-49. Analog Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{LOAD}	Output Resistor Load	Output load resistor	5	–	–	kOhm
C_{LOAD}	Output Capacitor Load	Output load capacitor	–	–	50	pF
V_{DACx_MIN}	Minimum Output Voltage on DACx	Code = 0x000 No R_{LOAD}, C_{LOAD} = 50 pF, DACC_ACR.IBCTLCHx =3	–	0.1	0.5	%. V_{VREFP}