Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	44
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70j21a-an

11.1.3 Internal ROM

The SAM E70/S70/V70/V71 embeds an Internal ROM for the SAM Boot Assistant (SAM-BA®), In Application Programming functions (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

The ROM may also be mapped at 0x00000000 depending on GPNVM bit setting and ITCM use.

11.1.4 Backup SRAM

The SAM E70/S70/V70/V71 embeds 1 Kbytes of backup SRAM located at 0x4007 4000.

The backup SRAM is accessible in 32-bit words only. Byte or half-word accesses are not supported.

The backup SRAM is supplied by VDDCORE in Normal mode.

In Backup mode, the backup SRAM supply is automatically switched to VDDIO through the backup SRAM power switch when VDDCORE falls. For more details, see the “Backup SRAM Power Switch” section.

11.1.5 Flash Memories

SAM E70/S70/V70/V71 devices embed 512 Kbytes, 1024 Kbytes or 2084 Kbytes of internal Flash mapped at address 0x40 0000.

The devices feature a Quad SPI (QSPI) interface, mapped at address 0x80000000, that extends the Flash size by adding an external SPI or QSPI Flash.

When accessed by the Cortex-M7 processor for programming operations, the QSPI and internal Flash address spaces must be defined in the Cortex-M7 memory protection unit (MPU) with the attribute 'Device' or 'Strongly Ordered'. For fetch or read operations, the attribute ‘Normal memory’ must be set to benefit from the internal cache. Refer to the ARM Cortex-M7 Technical Reference Manual (ARM DDI 0489) available on www.arm.com.

Some precautions must be taken when the accesses are performed by the central DMA. Refer to 22. Enhanced Embedded Flash Controller (EEFC) and 42. Quad Serial Peripheral Interface (QSPI).

11.1.5.1 Embedded Flash Overview

The memory is organized in sectors. Each sector has a size of 128 Kbytes. The first sector is divided into 3 smaller sectors.

The three smaller sectors are organized in 2 sectors of 8 Kbytes and 1 sector of 112 Kbytes. Refer to the figure below.

e. Program PMC_MCKR.CSS.

f. Wait for PMC_SR.MCKRDY to be set.

If a new value for PMC_MCKR.CSS corresponds to MAINCK or SLCK:

a. Program PMC_MCKR.CSS.

b. Wait for PMC_SR.MCKRDY to be set.

c. Program PMC_MCKR.PRES.

d. Wait for PMC_SR.MCKRDY to be set.

If CSS, MDIV or PRES are modified at any stage, the MCKRDY bit goes low to indicate that MCK and HCLK are not yet ready. The user must wait for MCKRDY bit to be set again before using MCK and HCLK.

Note: If PLLA clock was selected as MCK and the user decides to modify it by writing a new value into CKGR_PLLAR, the MCKRDY flag will go low while PLLA is unlocked. Once PLLA is locked again, LOCKA goes high and MCKRDY is set.
While PLLA is unlocked, MCK selection is automatically changed to SLCK for PLLA. For further information, see "Clock Switching Waveforms".

MCK is MAINCK divided by 2.

8. Select the Programmable clocks (PCKx):
PCKx are controlled via registers PMC_SCER, PMC_SCDR and PMC_SCSR.

   PCKx can be enabled and/or disabled via PMC_SCER and PMC_SCDR. Three PCKx can be used. PMC_SCSR indicates which PCKx is enabled. By default all PCKx are disabled.

   PMC_PCKx registers are used to configure PCKx.

   PMC_PCKx.CSS is used to select the PCKx divider source. Several clock options are available:

   – MAINCK
   – SLCK
   – MCK
   – PLLACK
   – UPLLCKDIV
   SLCK is the default clock source.

   PMC_PCKx.PRES is used to control the PCKx prescaler. It is possible to choose between different values (1 to 256). PCKx output is prescaler input divided by PRES. By default, the PRES value is cleared which means that PCKx is equal to Slow clock.

   Once PMC_PCKx has been configured, the corresponding PCKx must be enabled and the user must wait for PMC_SR.PCKRDYx to be set. This can be done either by polling PMC_SR.PCKRDYx or by waiting for the interrupt line to be raised if the associated interrupt source (PCKRDYx) has been enabled in PMC_IER. All parameters in PMC_PCKx can be programmed in a single write operation.

   If the PMC_PCKx.CSS and PMC_PCKx.PRES parameters are to be modified, the corresponding PCKx must be disabled first. The parameters can then be modified. Once this has been done, the user must re-enable PCKx and wait for the PCKRDYx bit to be set.

9. Enable the peripheral clocks

31.20.28 PMC SleepWalking Enable Register 0

Name: PMC_SLPWK_ER0
Offset: 0x0114
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	PID31	PID30	PID29	PID28	PID27	PID26	PID25	PID24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PID7							
Access								
Reset								

Bits 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – PIDx
Peripheral x SleepWalking Enable
Not all PIDs can be configured with asynchronous partial wake-up.

Only the following PID can be configured with asynchronous partial wake-up: UARTx and TWIHSx.

The clock of the peripheral must be enabled before using its asynchronous partial wake-up (SleepWalking) function (its associated PIDx field in PMC Peripheral Clock Status Register 0 or PMC Peripheral Clock Status Register 1 is set to ‘1’).

Value	Description
0	No effect.
1	The asynchronous partial wakeup (SleepWalking) function of the corresponding peripheral is enabled. **Note:** “PIDx” refers to identifiers as defined in the section “Peripheral Identifiers”

36.6 Linked List Descriptor Operation

36.6.1 Linked List Descriptor View

36.6.1.1 Channel Next Descriptor View 0–3 Structures

Table 36-2. Channel Next Descriptor View 0–3 Structures

Channel Next Descriptor	Offset	Structure member	Name
View 0 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Transfer Address Member	MBR_TA
View 1 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
View 2 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
	DSCR_ADDR+0x10	Configuration Register	MBR_CFG
View 3 Structure	DSCR_ADDR+0x00	Next Descriptor Address Member	MBR_NDA
	DSCR_ADDR+0x04	Microblock Control Member	MBR_UBC
	DSCR_ADDR+0x08	Source Address Member	MBR_SA
	DSCR_ADDR+0x0C	Destination Address Member	MBR_DA
	DSCR_ADDR+0x10	Configuration Member	MBR_CFG
	DSCR_ADDR+0x14	Block Control Member	MBR_BC
	DSCR_ADDR+0x18	Data Stride Member	MBR_DS
	DSCR_ADDR+0x1C	Source Microblock Stride Member	MBR_SUS
	DSCR_ADDR+0x20	Destination Microblock Stride Member	MBR_DUS

36.6.2 Descriptor Structure Members Description

Signal Name	Function	MII	RMII
GMDC	Management Data Clock	MDC	MDC
GMDIO	Management Data Input/Output	MDIO	MDIO

Note:

1. Input only. GTXCK must be provided with a 25 MHz / 50 MHz external crystal oscillator for MII / RMII interfaces, respectively.

38.5 Product Dependencies

38.5.1 I/O Lines

The pins used for interfacing the GMAC may be multiplexed with PIO lines. The programmer must first program the PIO Controller to assign the pins to their peripheral function. If I/O lines of the GMAC are not used by the application, they can be used for other purposes by the PIO Controller.

38.5.2 Power Management

The GMAC is not continuously clocked. The user must first enable the GMAC clock in the Power Management Controller before using it.

38.5.3 Interrupt Sources

The GMAC interrupt line is connected to one of the internal sources of the interrupt controller. Using the GMAC interrupt requires prior programming of the interrupt controller.

The GMAC features 6 interrupt sources. Refer to the table "Peripheral Identifiers" in the section "Peripherals" for the interrupt numbers for GMAC priority queues.

Related Links

14.1 Peripheral Identifiers

38.6 Functional Description

38.6.1 Media Access Controller

The Transmit Block of the Media Access Controller (MAC) takes data from FIFO, adds preamble, checks and adds padding and frame check sequence (FCS). Both half duplex and full duplex Ethernet modes of operation are supported.

When operating in half duplex mode, the MAC Transmit Block generates data according to the Carrier Sense Multiple Access with Collision Detect (CSMA/CD) protocol. The start of transmission is deferred if Carrier Sense (CRS) is active. If Collision (COL) is detected during transmission, a jam sequence is asserted and the transmission is retried after a random back off. The CRS and COL signals have no effect in full duplex mode.

The Receive Block of the MAC checks for valid preamble, FCS, alignment and length, and presents received frames to the MAC address checking block and FIFO. Software can configure the GMAC to receive jumbo frames of up to 10240 Bytes. It can optionally strip CRC (Cyclic Redundancy Check) from the received frame before transferring it to FIFO.

The Address Checker recognizes four specific 48-bit addresses, can recognize four different types of ID values, and contains a 64-bit Hash register for matching multicast and unicast addresses as required. It

38.8.97 GMAC Received LPI Transitions

Name: GMAC_RXLPI
Offset: 0x270
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNT[15:0] Count of Received LPI Transitions
A count of the number of times there is a transition from receiving normal idle to receiving low power idle.

Cleared on read.

38.8.109 GMAC Screening Type 2 Register x Priority Queue

Name: GMAC_ST2RPQx
Offset: 0x0540 + x*0x04 [x=0..7]
Reset: 0x00000000
Property: Read/Write

Screening type 2 registers are used to allocate up to 6 priority queues to received frames based on the VLAN priority field of received Ethernet frames.

Bit	31	30	29	28	27	26	25	24
		COMPCE	COMPC[4:0]					COMPBE
Access								
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COMPB[4:0]					COMPAE	COMPA[4:3]	
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		VLANP[2:0]				QNB[2:0]		
Access								
Reset		0	0	0		0	0	0

Bit 30 – COMPCE Compare C Enable

Value	Description
0	Compare C is disabled.
1	Comparison via the register designated by index COMPC is enabled.

Bits 29:25 – COMPC[4:0] Index of Screening Type 2 Compare Word 0/Word 1 register x
COMPC is a pointer to the compare registers GMAC_ST2CW0x and GMAC_ST2CW1x. When COMPCE=1, the compare is true if the data at the frame offset ANDed with the value MASKVAL is equal to the value of COMPVAL ANDed with the value of MASKVAL.

Bit 24 – COMPBE Compare B Enable

Value	Description
0	Compare B is disabled.
1	Comparison via the register designated by index COMPB is enabled.

38.8.112 GMAC Interrupt Mask Register Priority Queue x

Name: GMAC_IMRPQx
Offset: 0x0640 + x*0x04 [x=0..4]
Reset: 0x00000000
Property: Read/Write

A read of this register returns the value of the receive complete interrupt mask.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a '1' is written.

The following values are valid for all listed bit names of this register:

0: Corresponding interrupt is enabled.

1: Corresponding interrupt is disabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access					HRESP	ROVR		
Reset					0	0		

Bit	7	6	5	4	3	2	1	0
Access	TCOMP	AHB	RLEX			RXUBR	RCOMP	
Reset	0	0	0			0	0	

Bit 11 – HRESP HRESP Not OK

Bit 10 – ROVR Receive Overrun

Bit 7 – TCOMP Transmit Complete

Bit 6 – AHB AHB Error

Bit 5 – RLEX Retry Limit Exceeded or Late Collision

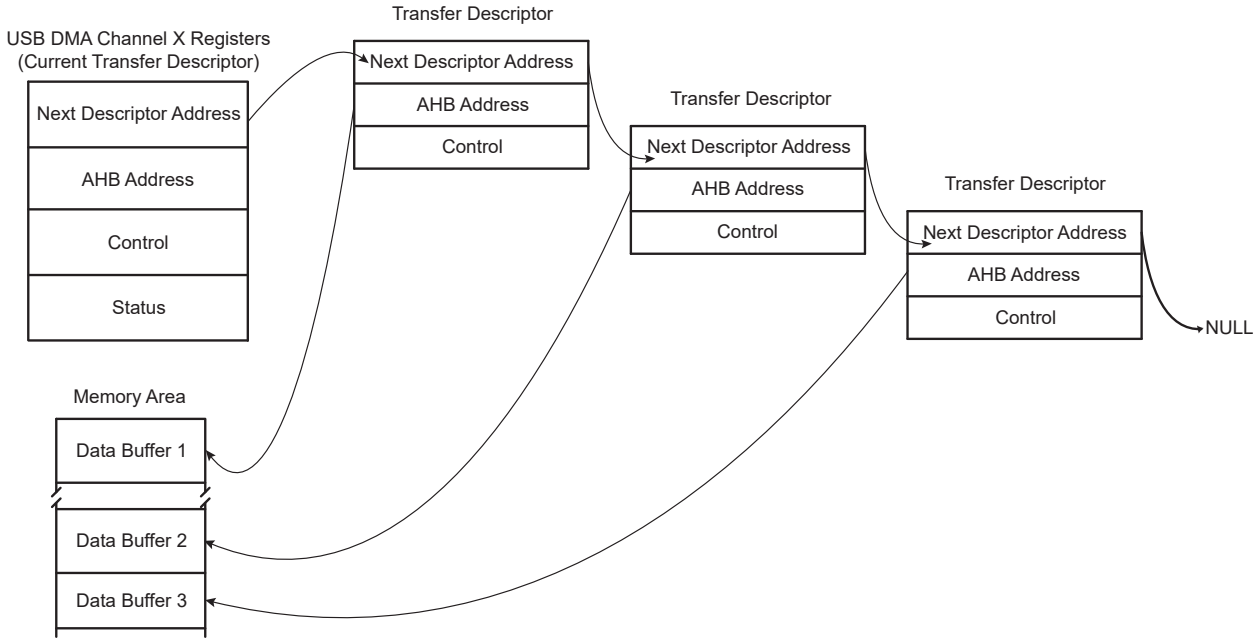
Bit 2 – RXUBR RX Used Bit Read

Bit 1 – RCOMP Receive Complete

means up to 128 words single cycle unbroken AHB bursts for bulk pipes/endpoints and 256 words single cycle unbroken bursts for isochronous pipes/endpoints. This maximal burst length is then controlled by the lowest programmed USB Pipe/Endpoint Size (USBHS_HSTPIPCFGx.PSIZE / USBHS_DEVEPTCFGx.EPSIZE) and the Buffer Byte Length (USBHS_HSTDMACONTROLx.BUFF_LENGTH / USBHS_DEVDMACONTROLx.BUFF_LENGTH) fields.

The USBHS average throughput can reach nearly 480 Mbps. Its average access latency decreases as burst length increases due to the zero wait-state side effect of unchanged pipe/endpoint. Word access allows reducing the AHB bandwidth required for the USB by four, as compared to native byte access. If at least 0 wait-state word burst capability is also provided by the other DMA AHB bus slaves, each DMA AHB bus needs less than 60% bandwidth allocation for full USB bandwidth usage at 33 MHz, and less than 30% at 66 MHz.

Figure 39-24. Example of a DMA Chained List



39.5.5 USB DMA Channel Transfer Descriptor

The DMA channel transfer descriptor is loaded from the memory. The following structures apply:

Offset 0:

- The address must be aligned: 0xXXXX0
- Next Descriptor Address Register: USBHS_xxxDMANXTDSCx

Offset 4:

- The address must be aligned: 0xXXXX4
- DMA Channelx Address Register: USBHS_xxxDMAADDRESSx

Offset 8:

- The address must be aligned: 0xXXXX8
- DMA Channelx Control Register: USBHS_xxxDMACONTROLx

Value	Description
0	As soon as data is written in SPI_TDR.
1	SPI_TDR and internal shift register are empty. If a transfer delay has been defined, TXEMPTY is set after the end of this delay.

Bit 8 – NSSR NSS Rising (cleared on read)

Value	Description
0	No rising edge detected on NSS pin since the last read of SPI_SR.
1	A rising edge occurred on NSS pin since the last read of SPI_SR.

Bit 3 – OVRES Overrun Error Status (cleared on read)
An overrun occurs when SPI_RDR is loaded at least twice from the internal shift register since the last read of SPI_RDR.

Value	Description
0	No overrun has been detected since the last read of SPI_SR.
1	An overrun has occurred since the last read of SPI_SR.

Bit 2 – MODF Mode Fault Error (cleared on read)

Value	Description
0	No mode fault has been detected since the last read of SPI_SR.
1	A mode fault occurred since the last read of SPI_SR.

Bit 1 – TDRE Transmit Data Register Empty (cleared by writing SPI_TDR)
0: Data has been written to SPI_TDR and not yet transferred to the internal shift register.

1: The last data written in SPI_TDR has been transferred to the internal shift register.

TDRE is cleared when the SPI is disabled or at reset. Enabling the SPI sets the TDRE flag.

Bit 0 – RDRF Receive Data Register Full (cleared by reading SPI_RDR)
0: No data has been received since the last read of SPI_RDR.

1: Data has been received and the received data has been transferred from the internal shift register to SPI_RDR since the last read of SPI_RDR.

44.9.3 SSC Receive Clock Mode Register

Name: SSC_RCMR
Offset: 0x10
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the SSC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	PERIOD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	STTDLY[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				STOP	START[3:0]			
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CKG[1:0]		CKI	CKO[2:0]			CKS[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:24 – PERIOD[7:0] Receive Period Divider Selection
This field selects the divider to apply to the selected Receive Clock in order to generate a new Frame Sync signal. If 0, no PERIOD signal is generated. If not 0, a PERIOD signal is generated each 2 x (PERIOD + 1) Receive Clock.

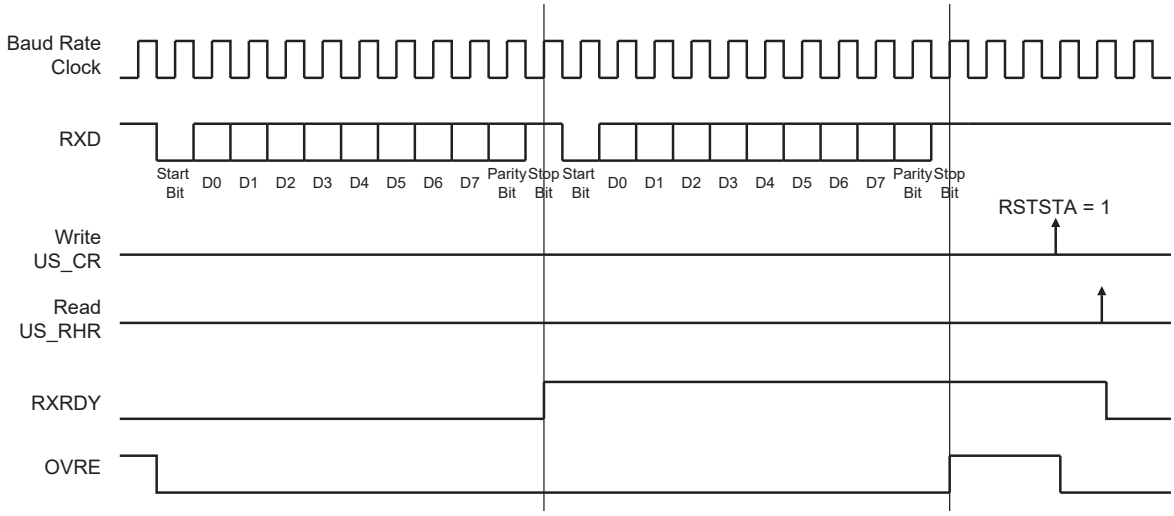
Bits 23:16 – STTDLY[7:0] Receive Start Delay
If STTDLY is not 0, a delay of STTDLY clock cycles is inserted between the start event and the current start of reception. When the receiver is programmed to start synchronously with the transmitter, the delay is also applied.

Note:
STTDLY must be configured in relation to the receive synchronization data to be stored in SSC_RSHR.

Bit 12 – STOP Receive Stop Selection

Value	Description
0	After completion of a data transfer when starting with a Compare 0, the receiver stops the data transfer and waits for a new compare 0.
1	After starting a receive with a Compare 0, the receiver operates in a continuous mode until a Compare 1 is detected.

Figure 46-20. Receiver Status



46.6.3.8 Parity

The USART supports five Parity modes. The PAR field also enables Multidrop mode, see “Multidrop Mode”. Even and odd parity bit generation and error detection are supported. The configuration is done in US_MR.PAR.

If even parity is selected, the parity generator of the transmitter drives the parity bit to 0 if a number of 1s in the character data bit is even, and to 1 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If odd parity is selected, the parity generator of the transmitter drives the parity bit to 1 if a number of 1s in the character data bit is even, and to 0 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If the mark parity is used, the parity generator of the transmitter drives the parity bit to 1 for all characters. The receiver parity checker reports an error if the parity bit is sampled to 0. If the space parity is used, the parity generator of the transmitter drives the parity bit to 0 for all characters. The receiver parity checker reports an error if the parity bit is sampled to 1. If parity is disabled, the transmitter does not generate any parity bit and the receiver does not report any parity error.

The following table shows an example of the parity bit for the character 0x41 (character ASCII “A”) depending on the configuration of the USART. Because there are two bits set to 1 in the character value, the parity bit is set to ‘1’ when the parity is odd, or configured to ‘0’ when the parity is even.

Table 46-6. Parity Bit Examples

Character	Hexadecimal	Binary	Parity Bit	Parity Mode
A	0x41	0100 0001	1	Odd
A	0x41	0100 0001	0	Even
A	0x41	0100 0001	1	Mark
A	0x41	0100 0001	0	Space
A	0x41	0100 0001	None	None

49.6.27 MCAN Receive FIFO 0 Configuration

Name: MCAN_RXF0C
Offset: 0xA0
Reset: 0x00000000
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Bit	31	30	29	28	27	26	25	24
	F0OM	F0WM[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		F0S[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	F0SA[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	F0SA[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit 31 – F0OM FIFO 0 Operation Mode
FIFO 0 can be operated in Blocking or in Overwrite mode (see Rx FIFOs).

Value	Description
0	FIFO 0 Blocking mode.
1	FIFO 0 Overwrite mode.

Bits 30:24 – F0WM[6:0] Receive FIFO 0 Watermark

Value	Description
0	Watermark interrupt disabled.
1-64	Level for Receive FIFO 0 watermark interrupt (MCAN_IR.RF0W).
>64	Watermark interrupt disabled.

Bits 22:16 – F0S[6:0] Receive FIFO 0 Size
The Receive FIFO 0 elements are indexed from 0 to F0S-1.

Value	Description
0	No Receive FIFO 0
1-64	Number of Receive FIFO 0 elements.
>64	Values greater than 64 are interpreted as 64.

50.7.19 TC QDEC Interrupt Mask Register

Name: TC_QIMR
Offset: 0xD0
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					MPE	QERR	DIRCHG	IDX
Access					R	R	R	R
Reset					0	0	0	0

Bit 3 – MPE Consecutive Missing Pulse Error

Value	Description
0	The interrupt on the maximum number of consecutive missing pulses specified in MAXCMP is disabled.
1	The interrupt on the maximum number of consecutive missing pulses specified in MAXCMP is enabled.

Bit 2 – QERR Quadrature Error

Value	Description
0	The interrupt on quadrature error is disabled.
1	The interrupt on quadrature error is enabled.

Bit 1 – DIRCHG Direction Change

Value	Description
0	The interrupt on rotation direction change is disabled.
1	The interrupt on rotation direction change is enabled.

Bit 0 – IDX Index

  - Independent Clock Selection for Each Channel
  - Independent Period, Duty-Cycle and Dead-Time for Each Channel
  - Independent Double Buffering of Period, Duty-Cycle and Dead-Times for Each Channel
  - Independent Programmable Selection of The Output Waveform Polarity for Each Channel, with Double Buffering
  - Independent Programmable Center- or Left-aligned Output Waveform for Each Channel
  - Independent Output Override for Each Channel
  - Independent Interrupt for Each Channel, at Each Period for Left-Aligned or Center-Aligned Configuration
  - Independent Update Time Selection of Double Buffering Registers (Polarity, Duty Cycle) for Each Channel, at Each Period for Left-Aligned or Center-Aligned Configuration
- External Trigger Input Management (e.g., for DC/DC or Lighting Control)
  - External PWM Reset Mode
  - External PWM Start Mode
  - Cycle-By-Cycle Duty Cycle Mode
  - Leading-Edge Blanking
- 2 2-bit Gray Up/Down Channels for Stepper Motor Control
- Spread Spectrum Counter to Allow a Constantly Varying Duty Cycle (only for Channel 0)
- Synchronous Channel Mode
  - Synchronous Channels Share the Same Counter
  - Mode to Update the Synchronous Channels Registers after a Programmable Number of Periods
  - Synchronous Channels Supports Connection of one DMA Controller Channel Which Offers Buffer Transfer Without Processor Intervention To Update Duty-Cycle Registers
- 2 Independent Events Lines Intended to Synchronize ADC Conversions
  - Programmable delay for Events Lines to delay ADC measurements
- 8 Comparison Units Intended to Generate Interrupts, Pulses on Event LinesDMA Controller Transfer Requests
- 8 Programmable Fault Inputs Providing an Asynchronous Protection of PWM Outputs
  - 3 User Driven through PIO Inputs
  - PMC Driven when Crystal Oscillator Clock Fails
  - ADC Controller Driven through Configurable Comparison Function
  - Analog Comparator Controller Driven
  - Timer/Counter Driven through Configurable Comparison Function
- Register Write Protection

51.7.15 PWM Interrupt Disable Register 2

Name: PWM_IDR2
Offset: 0x38
Reset: –
Property: Write-only

This register can only be written if bits WPSWS1 and WPHWS1 are cleared in the PWM Write Protection Status Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CMPU7	CMPU6	CMPU5	CMPU4	CMPU3	CMPU2	CMPU1	CMPU0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	15	14	13	12	11	10	9	8
	CMPM7	CMPM6	CMPM5	CMPM4	CMPM3	CMPM2	CMPM1	CMPM0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	7	6	5	4	3	2	1	0
					UNRE			WRDY
Access					W			W
Reset					–			–

Bits 16, 17, 18, 19, 20, 21, 22, 23 – CMPUx Comparison x Update Interrupt Disable

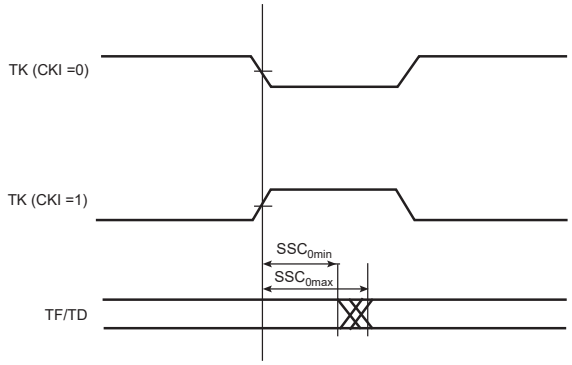
Bits 8, 9, 10, 11, 12, 13, 14, 15 – CMPMx Comparison x Match Interrupt Disable

Bit 3 – UNRE Synchronous Channels Update Underrun Error Interrupt Disable

Bit 0 – WRDY Write Ready for Synchronous Channels Update Interrupt Disable

Value	Name	Description
0	DISABLE_SW_PROT	Disables the software write protection of the register groups of which the bit WPRGx is at ‘1’.
1	ENABLE_SW_PROT	Enables the software write protection of the register groups of which the bit WPRGx is at ‘1’.
2	ENABLE_HW_PROT	Enables the hardware write protection of the register groups of which the bit WPRGx is at ‘1’. Only a hardware reset of the PWM controller can disable the hardware write protection. Moreover, to meet security requirements, the PIO lines associated with the PWM can not be configured through the PIO interface.

Figure 58-41. Min and Max Access Time of Output Signals



58.13.1.15 ISI Timings

58.13.1.15.1 Timing Conditions

Timings are given assuming the load capacitance in the following table.

Table 58-76. Load Capacitance

Supply	C_L Max
3.3V	30 pF
1.7V	PBD

58.13.1.15.2 Timing Extraction

Table 58-77. ISI Timings with Peripheral Supply 3.3V

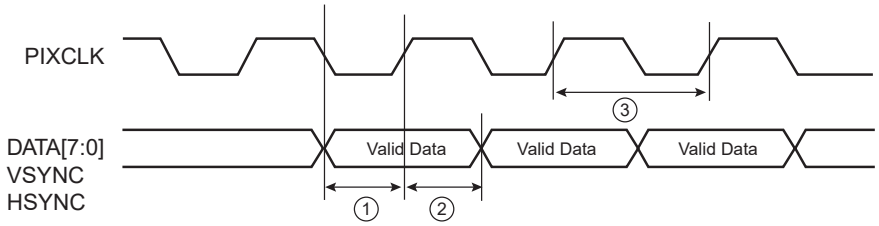
Symbol	Parameter	Min	Max	Unit
ISI_1	DATA/VSYNC/HSYNC setup time	1.5	–	ns
ISI_2	DATA/VSYNC/HSYNC hold time	-1.2	–	ns
ISI_3	PIXCLK frequency	–	75	MHz

Figure 58-42.

Table 58-78. ISI Timings with Peripheral Supply 1.8V

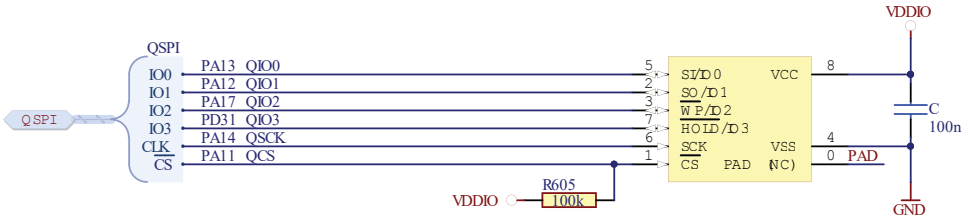
Symbol	Parameter	Min	Max	Unit
ISI_1	DATA/VSYNC/HSYNC setup time	1.8	–	ns
ISI_2	DATA/VSYNC/HSYNC hold time	-1.4	–	ns
ISI_3	PIXCLK frequency	–	75	MHz

Figure 58-43. ISI Timing Diagram



Signal Name	Recommended Pin Connection	Description
	(Pullup at VDDIO)	Pulled-up input (100 kOhm) to VDDIO at reset.
QIO0–QIO3	Application dependent.	QSPI I/O Pulled-up inputs (100 kOhm) to VDDIO at reset.

Figure 60-7. Schematic Example with QSPI Data Flash



60.2.12 Other Interfaces

Signal Name	Recommended Pin Connection	Description
Universal Synchronous Asynchronous Receiver Transmitter		
SCKx	Application dependent.	USARTx Serial Clock Pulled-up inputs (100 kOhm) to VDDIO at reset.
TXDx	Application dependent.	USARTx Transmit Data Pulled-up inputs (100 kOhm) to VDDIO at reset.
RXDx	Application dependent.	USARTx Receive Data Pulled-up inputs (100 kOhm) to VDDIO at reset.
RTSx	Application dependent.	USARTx Request To Send Pulled-up inputs (100 kOhm) to VDDIO at reset.
CTSx	Application dependent.	USARTx Clear To Send Pulled-up inputs (100 kOhm) to VDDIO at reset.
DTRx	Application dependent.	USARTx Data Terminal Ready Pulled-up inputs (100 kOhm) to VDDIO at reset.
DSRx	Application dependent.	USARTx Data Set Ready Pulled-up inputs (100 kOhm) to VDDIO at reset.
DCDx	Application dependent.	USARTx Data Carrier Detect Pulled-up inputs (100 kOhm) to VDDIO at reset.
RIx	Application dependent.	USARTx Ring Indicator Pulled-up inputs (100 kOhm) to VDDIO at reset.
LONCOL1	Application dependent.	LON Collision Detection Pulled-up input (100 kOhm) to VDDIO at reset.
Synchronous Serial Controller		

Date	Changes
	- Table 56-38 “VREFP Electrical Characteristics”: changed min and max values for I_{VREFP}. - Table 56-46 “Single-ended Output Offset Error”: added note on voltage application. - Table 56-47 “Single-ended Static Electrical Characteristics”: added conditions and values. - Table 56-49 “Differential Static Electrical Characteristics”: changed min and max values. Added Section 56.10 “Analog Comparator Characteristics”. Section 56.12 “12-bit DAC Characteristics” - Added note to Table 56-59 “Analog Power Supply Characteristics”. Added new conditions to Table 56-62 “Static Performance Characteristics”. and updated min and max values for INL, DNL and Gain Error. Section 56.13 “Timings for Worst-Case Conditions” - Table 56-68 “I/O Characteristics”: new conditions and the corresponding max values added. - Section 56.13.2 “Embedded Flash Characteristics”: in Table 56-87 “AC Flash Characteristics” changed Full Chip Erase values. Replaced two “Embedded Flash Wait State” tables with single Table 56-88 “Embedded Flash Wait State at 105°C“
	Section 56.14 “Timings for STH Conditions” - Table 56-92 “I/O Characteristics”: new conditions and the corresponding max values added. - Section 56.14.2 “Embedded Flash Characteristics”: replaced two “Embedded Flash Wait State” tables with single Table 56-112 “Embedded Flash Wait State at 105°C“
	Section 57. “Mechanical Characteristics” Deleted Section 57.6 “64-lead QFN Wettable Flanks Package”.
	Section 59. “Ordering Information”: updated ordering codes by appending trailing ‘T’. Removed Note 1 and cross-references. Changed conditioning to Tape & Reel.

Table 62-6. SAM E70/S70/V70/V71 Datasheet Rev. 44003A – Revision History

Date	Changes
15-Oct-13	First issue