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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	44
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70j21b-an

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
PWMCx_PWMH0 – PWMCx_PWMH3	Waveform Output High for Channel 0–3	Output	–	–	–
PWMCx_PWML0– PWMCx_PWML3	Waveform Output Low for Channel 0–3	Output	–	–	Only output in complementary mode when dead time insertion is enabled.
PWMCx_PWMFI0 – PWMCx_PWMFI2	Fault Input	Input	–	–	–
PWMCx_PWMEX TRG0– PWMCx_PWMEX TRG1	External Trigger Input	Input	–	–	–
Serial Peripheral Interface - SPI(x=[0..1])					
SPIx_MISO	Master In Slave Out	I/O	–	–	–
SPIx_MOSI	Master Out Slave In	I/O	–	–	–
SPIx_SPCK	SPI Serial Clock	I/O	–	–	–
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	–	–
SPIx_NPCS1– SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	–	–
Quad IO SPI - QSPI					
QSCK	QSPI Serial Clock	Output	–	–	–
QCS	QSPI Chip Select	Output	–	–	–
QIO0–QIO3	QSPI I/O QIO0 is QMOSI Master Out Slave In QIO1 is QMISO Master In Slave Out	I/O	–	–	–
Two-Wire Interface - TWIHS(x=0..2)					
TWDx	TWIx Two-wire Serial Data	I/O	–	–	–
TWCKx	TWIx Two-wire Serial Clock	I/O	–	–	–
Analog					

Value	Name	Description
		This results in not having one clock cycle latency when the fixed master tries to access the slave again.

Bits 9:1 – SLOT_CYCLE[8:0] Maximum Bus Grant Duration for Masters
When SLOT_CYCLE AHB clock cycles have elapsed since the last arbitration, a new arbitration takes place to let another master access this slave. If another master is requesting the slave bus, then the current master burst is broken.

If SLOT_CYCLE = 0, the slot cycle limit feature is disabled and bursts always complete unless broken according to the ULBT.

This limit has been placed in order to enforce arbitration so as to meet potential latency constraints of masters waiting for slave access.

This limit must not be too small. Unreasonably small values break every burst and the MATRIX arbitrates without performing any data transfer. The default maximum value is usually an optimal conservative choice.

In most cases, this feature is not needed and should be disabled for power saving.

See “Slot Cycle Limit Arbitration” for details.

31.20.31 PMC SleepWalking Disable Register 1

Name: PMC_SLPWK_DR1
Offset: 0x0138
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
		PID62		PID60	PID59	PID58	PID57	PID56
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
			PID53	PID52	PID51	PID50	PID49	PID48
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	PID47	PID46	PID45	PID44	PID43	PID42	PID41	PID40
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	PID39		PID37		PID35	PID34	PID33	PID32
Access								
Reset								

Bits 0:3,5,7:28,30 – PID Peripheral Clock x Disable

Value	Description
0	No effect.
1	Disables the corresponding peripheral clock.

After reset, depending on the I/O, pullup or pulldown can be set.

32.5.2 I/O Line or Peripheral Function Selection

When a pin is multiplexed with one or two peripheral functions, the selection is controlled with the Enable Register (PIO_PER) and the Disable Register (PIO_PDR). The Status Register (PIO_PSR) is the result of the set and clear registers and indicates whether the pin is controlled by the corresponding peripheral or by the PIO Controller. A value of zero indicates that the pin is controlled by the corresponding on-chip peripheral selected in the Peripheral ABCD Select registers (PIO_ABCDSR1 and PIO_ABCDSR2). A value of one indicates the pin is controlled by the PIO Controller.

If a pin is used as a general-purpose I/O line (not multiplexed with an on-chip peripheral), PIO_PER and PIO_PDR have no effect and PIO_PSR returns a one for the corresponding bit.

After reset, the I/O lines are controlled by the PIO Controller, i.e., PIO_PSR resets at one. However, in some events, it is important that PIO lines are controlled by the peripheral (as in the case of memory chip select lines that must be driven inactive after reset, or for address lines that must be driven low for booting out of an external memory). Thus, the reset value of PIO_PSR is defined at the product level and depends on the multiplexing of the device.

32.5.3 Peripheral A or B or C or D Selection

The PIO Controller provides multiplexing of up to four peripheral functions on a single pin. The selection is performed by writing PIO_ABCDSR1 and PIO_ABCDSR2.

For each pin:

- The corresponding bit at level zero in PIO_ABCDSR1 and the corresponding bit at level zero in PIO_ABCDSR2 means peripheral A is selected.
- The corresponding bit at level one in PIO_ABCDSR1 and the corresponding bit at level zero in PIO_ABCDSR2 means peripheral B is selected.
- The corresponding bit at level zero in PIO_ABCDSR1 and the corresponding bit at level one in PIO_ABCDSR2 means peripheral C is selected.
- The corresponding bit at level one in PIO_ABCDSR1 and the corresponding bit at level one in PIO_ABCDSR2 means peripheral D is selected.

Note that multiplexing of peripheral lines A, B, C and D only affects the output line. The peripheral input lines are always connected to the pin input (refer to Figure 32-2).

Writing in PIO_ABCDSR1 and PIO_ABCDSR2 manages the multiplexing regardless of the configuration of the pin. However, assignment of a pin to a peripheral function requires a write in PIO_ABCDSR1 and PIO_ABCDSR2 in addition to a write in PIO_PDR.

After reset, PIO_ABCDSR1 and PIO_ABCDSR2 are zero, thus indicating that all the PIO lines are configured on peripheral A. However, peripheral A generally does not drive the pin as the PIO Controller resets in I/O Line mode.

If the software selects a peripheral A, B, C or D which does not exist for a pin, no alternate functions are enabled for this pin and the selection is taken into account. The PIO Controller does not carry out checks to prevent selection of a peripheral which does not exist.

32.5.4 Output Control

When the I/O line is assigned to a peripheral function, i.e., the corresponding bit in PIO_PSR is at zero, the drive of the I/O line is controlled by the peripheral. Peripheral A or B or C or D depending on the value in PIO_ABCDSR1 and PIO_ABCDSR2 determines whether the pin is driven or not.

Value	Description
0	D7 → R7.
1	D0 → R7.

Bit 13 – GRAYSCALE Grayscale Mode Format Enable

Value	Description
0	Grayscale mode is disabled.
1	Input image is assumed to be grayscale-coded.

Bit 12 – RGB_MODE RGB Input Mode

Value	Description
0	RGB 8:8:8 24 bits.
1	RGB 5:6:5 16 bits.

Bit 11 – GS_MODE Grayscale Pixel Format Mode

Value	Description
0	2 pixels per word.
1	1 pixel per word.

Bits 10:0 – IM_VSIZE[10:0] Vertical Size of the Image Sensor [0..2047]
IM_VSIZE = Vertical size - 1

37.6.22 DMA Codec Control Register

Name: ISI_DMA_C_CTRL
Offset: 0x54
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					C_DONE	C_IEN	C_WB	C_FETCH
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – C_DONE Codec Transfer Done
This bit is only updated in the memory.

Value	Description
0	The transfer related to this descriptor has not been performed.
1	The transfer related to this descriptor has completed. This bit is updated in memory at the end of the transfer when writeback operation is enabled.

Bit 2 – C_IEN Transfer Done Flag Control

Value	Description
0	Codec transfer done flag generation is enabled.
1	Codec transfer done flag generation is disabled.

Bit 1 – C_WB Descriptor Writeback Control Bit

Value	Description
0	Codec channel writeback operation is disabled.
1	Codec channel writeback operation is enabled.

Bit 0 – C_FETCH Descriptor Fetch Control Bit

38.8.52 GMAC Single Collision Frames Register

Name: GMAC_SCF
Offset: 0x138
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							SCOL[17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	SCOL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – SCOL[17:0] Single Collision
This register counts the number of frames experiencing a single collision before being successfully transmitted i.e., no underrun.

38.8.76 GMAC Receive Symbol Errors Register

Name: GMAC_RSE
Offset: 0x198
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							RXSE[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RXSE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – RXSE[9:0] Receive Symbol Errors
This bit field counts the number of frames that had GRXER asserted during reception. For 10/100 mode symbol errors are counted regardless of frame length checks. Receive symbol errors will also be counted as an FCS or alignment error if the frame is between 64 and 1518 Bytes (1536 Bytes if GMAC_NCFGR.MAXFS=1). If the frame is larger it will be recorded as a jabber error.

39.6.10 Device Global Interrupt Disable Register

Name: USBHS_DEVIDR
Offset: 0x0014
Property: Write-only

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_DEVIMR.

Bit	31	30	29	28	27	26	25	24
	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			PEP_9	PEP_8	PEP_7	PEP_6	PEP_5	PEP_4
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PEP_3	PEP_2	PEP_1	PEP_0				
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		UPRSMEC	EORSMEC	WAKEUPEC	EORSTEC	SOFEC	MSOFEC	SUSPEC
Access								
Reset								

Bits 25, 26, 27, 28, 29, 30, 31 – DMA_ DMA Channel x Interrupt Disable

Bits 12, 13, 14, 15, 16, 17, 18, 19, 20, 21 – PEP_ Endpoint x Interrupt Disable

Bit 6 – UPRSMEC Upstream Resume Interrupt Disable

Bit 5 – EORSMEC End of Resume Interrupt Disable

Bit 4 – WAKEUPEC Wakeup Interrupt Disable

Bit 3 – EORSTEC End of Reset Interrupt Disable

Bit 2 – SOFEC Start of Frame Interrupt Disable

Bit 1 – MSOFEC Micro Start of Frame Interrupt Disable

Bit 0 – SUSPEC Suspend Interrupt Disable

Value	Description
0	Frees the endpoint memory.
1	Allocates the endpoint memory. The user should check the USBHS_DEVEPTISRx.CFGOK bit to know whether the allocation of this endpoint is correct.

39.6.48 Host Pipe x Clear Register (Control, Bulk Pipes)

Name: USBHS_HSTPIPICRx
Offset: 0x0560 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if PTYPE = 0x0 or 0x2 in "Host Pipe x Configuration Register".

For additional information, see "Host Pipe x Status Register (Control, Bulk Pipes)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_HSTPIPISRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETIC	RXSTALLDIC	OVERFIC	NAKEDIC		TXSTPIC	TXOUTIC	RXINIC
Access								
Reset	0	0	0	0		0	0	0

Bit 7 – SHORTPACKETIC Short Packet Interrupt Clear

Bit 6 – RXSTALLDIC Received STALLed Interrupt Clear

Bit 5 – OVERFIC Overflow Interrupt Clear

Bit 4 – NAKEDIC NAKed Interrupt Clear

Bit 2 – TXSTPIC Transmitted SETUP Interrupt Clear

Bit 1 – TXOUTIC Transmitted OUT Data Interrupt Clear

Bits 21:19 – TRTYP[2:0] Transfer Type

Value	Name	Description
0	SINGLE	MMC/SD Card Single Block
1	MULTIPLE	MMC/SD Card Multiple Block
2	STREAM	MMC Stream
4	BYTE	SDIO Byte
5	BLOCK	SDIO Block

Bit 18 – TRDIR Transfer Direction
0 (WRITE): Write.

1 (READ): Read.

Bits 17:16 – TRCMD[1:0] Transfer Command

Value	Name	Description
0	NO_DATA	No data transfer
1	START_DATA	Start data transfer
2	STOP_DATA	Stop data transfer
3	Reserved	Reserved

Bit 12 – MAXLAT Max Latency for Command to Response
0 (5): 5-cycle max latency.

1 (64): 64-cycle max latency.

Bit 11 – OPDCMD Open Drain Command
0 (PUSHPULL): Push pull command.

1 (OPENDRAIN): Open drain command.

Bits 10:8 – SPCMD[2:0] Special Command

Value	Name	Description
0	STD	Not a special CMD.
1	INIT	Initialization CMD: 74 clock cycles for initialization sequence.
2	SYNC	Synchronized CMD: Wait for the end of the current data block transfer before sending the pending command.
3	CE_ATA	CE-ATA Completion Signal disable Command. The host cancels the ability for the device to return a command completion signal on the command line.
4	IT_CMD	Interrupt command: Corresponds to the Interrupt Mode (CMD40).
5	IT_RESP	Interrupt response: Corresponds to the Interrupt Mode (CMD40).

One physical channel after the ChannelAddress is sent on MLBS, the transmitting MediaLB Device associated with that ChannelAddress outputs a command byte (Command) on MLBS and respective data (Data) on MLBD, concurrently. The Command byte contains information about the data simultaneously being transmitted. The MediaLB Device receiving the data outputs a status byte (RxStatus) on MLBS after the transmitting Device sends the Command byte. This status response can indicate that the Device is ready to receive the data, or that the receiving Device is busy (e.g. cannot receive the data at present). Since synchronous stream data is sent in a broadcast fashion, Devices receiving synchronous data can never return a busy status response. In this situation, the RxStatus byte must not be actively driven onto the MLBS line by Devices receiving synchronous data.

The ChannelAddresses output by the Controller for each logical channel are used in normal data transport and can be statically or dynamically assigned. To support dynamic configuration of MediaLB Devices, a unique DeviceAddress must be assigned to all MediaLB Devices before startup. DeviceAddresses allow the External Host Controller (EHC) and MediaLB Controller to dynamically determine which Devices exist on the bus. At the request of a MediaLB Device (e.g. EHC), the Controller scans for DeviceAddresses in the System Channel. Once a Device is detected, a ChannelAddress for each logical channel can be assigned.

The DeviceAddress, ChannelAddress, Command, and RxStatus structures are described in the Link Layer section.

48.2 Embedded Characteristics

- Support of all MOST data transport methods: synchronous stream data, asynchronous packet data, control message data, and isochronous data
- Multiple clock rates supported
- Scalable data rate for all MOST Network data transport methods
- A frame synchronization pattern (FRAMESYNC) enables easy Device synchronization to MOST Networks
- Dedicated system-broadcast channel for administration
- Support of MediaLB Controller to MediaLB Device transfers and inter-MediaLB Devices transfers
- Broadcast support from one transmitter to multiple receivers for synchronous stream data

48.3 Block Diagram

The following figure is the top-level block diagram of the MLB behavioral models.

HBI Channel	CAT Address	CAT Offset
0x3E	0x8F	110
0x3F	0x8F	111

48.6.3.3 Routing Fabric Block

The Routing Fabric (RF) block manages the flow of data between the MediaLB Port and the HBI Port. Bus multiplexers and a bus arbiter are implemented in the RF block for accessing the channel table RAM (CTR) and data buffer RAM (DBR).

Each DMA controller in the routing fabric uses Channel Descriptors (stored in the CTR) to manage access to dynamic buffers in the DBR.

Data Buffer RAM

The MLB has an external data buffer RAM (DBR) that is 8-bit x 16k entries deep. The DBR provides dynamic circular buffering between the transmit and receive devices.

The size and location of each data buffer is defined by software in the channel descriptor table (CDT), which is located in the CTR.

Receive devices retain the write address pointer to the associated circular data buffer in the DBR, while transmit devices retain the read address pointer. The DMA controllers in the routing fabric are responsible for ensuring that the circular buffers do not overflow or underflow. Each channel type (e.g., synchronous, isochronous, asynchronous and control) has Full and Empty detection.

- Synchronous Channels
  For synchronous channels, two mechanisms prevent overflow and underflow of the data buffer:
  - Hardware aligns the read pointer (RPTR) to the write pointer (WPTR) to ensure an offset of two sub-buffers.
  - RPTR and WPTR are periodically synchronized to the start of the next sub-buffer (e.g. following a FRAMESYNC).
- Isochronous Channels
  For isochronous channels, hardware does not read from an empty data buffer or write to a full data buffer. The conditions used by hardware for detection include:

  Data buffer Empty condition: (RPTR = WPTR) AND (BF = 0), and

  Data buffer Full condition: (WPTR = RPTR) AND (BF = 1).
- Asynchronous and Control Channels
  For asynchronous and control channels, hardware does not read from an empty data buffer or write to a full data buffer. Hardware evaluates the DMA pointers (RPTR, WPTR) and packet count (RPC, WPC) to detect the data buffer condition, where:
  - Data buffer Empty condition: (RPTR = WPTR) AND (RPC = WPC), and
  - Data buffer Full condition: ((WPTR = RPTR) AND (WPC != RPC)) OR (WPC = (RPC - 1)).

Channel Table RAM

The MLB has an external Channel Table RAM (CTR) that is 128-bit x 144-entry. The CTR allows system software to dynamically configure channel routing and allocate data buffers in the DBR.

The CTR is logically divided into three sub-tables:

- Channel Descriptor Table (CDT)

Offset	Name	Bit Pos.								
		15:8	TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
		23:16	TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
		31:24	TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
0xE4	MCAN_TXBCIE	7:0	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
		15:8	CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
		23:16	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
		31:24	CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
0xE8 ... 0xEF	Reserved									
0xF0	MCAN_TXEFC	7:0	EFSA[5:0]							
		15:8	EFSA[13:6]							
		23:16			EFS[5:0]					
		31:24			EFWM[5:0]					
0xF4	MCAN_TXEFS	7:0			EFFL[5:0]					
		15:8				EFGI[4:0]				
		23:16				EFPI[4:0]				
		31:24							TEFL	EFF
0xF8	MCAN_TXEFA	7:0				EFAI[4:0]				
		15:8								
		23:16								
		31:24								

Value	Description
0	The interrupt on IDX input is disabled.
1	The interrupt on IDX input is enabled.

52.7.26 AFEC Correction Values Register

Name: AFEC_CVR
Offset: 0xD4
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the AFEC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	GAINCORR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GAINCORR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	OFFSETCORR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OFFSETCORR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GAINCORR[15:0] Gain Correction
Gain correction to apply on converted data. Only bits 0 to 15 are relevant (other bits are ignored and read as 0).

Bits 15:0 – OFFSETCORR[15:0] Offset Correction
Offset correction to apply on converted data. The offset is signed (2's complement), only bits 0 to 11 are relevant (other bits are ignored and read as 0).

57.5.15 AES GCM Encryption Counter Value Register

Name: AES_CTRR
Offset: 0x98
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	CTR[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CTR[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CTR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CTR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CTR[31:0] GCM Encryption Counter
Reports the current value of the 32-bit GCM counter.

DACC_ACR.IBCTLCHx	Maximum Conversion Rate
2	N/A
3	1 Ms/s

Table 58-45. Voltage Reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VREFP}	Positive Voltage Reference	Externally decoupled 1 µF	1.7	–	V_{DDIN}	V
I_{VREFP}	DC Current on VREFP	–	–	2.5	–	µA

Note: V_{REFP} is the positive reference shared with AFE and may have a different value for AFE. Refer to the AFE electrical characteristics if AFE is used. The V_{REFN} pin must be connected to ground.

Table 58-46. DAC Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DAC}	DAC Clock Frequency	–	–	–	12	MHz
f_S	Sampling Frequency	–	–	f_{DAC} / 12	–	MHz

Table 58-47. Static Performance Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
INL	Integral Non-linearity (see **Note 1**)	No R_{LOAD}	-10	±2	10	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
DNL	Differential Non-linearity (see **Note 1**)	No R_{LOAD}	-4	±2	4	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
E_O	Offset Error (see **Note 2**)	–	-8	1	8	mV
E_G	Gain Error	No R_{LOAD}	-1	–	1	%.FSR
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				

Note:

1. Best-fit Curve from 0x080 to 0xF7F.
2. Difference between DACx at 0x800 and V_{VREFP}/2.

60. Schematic Checklist

The schematic checklist provides the user with the requirements regarding the different pin connections that must be considered before starting any new board design. It also provides information on the minimum hardware resources required to quickly develop an application with the SAM E70/S70/V70/V71 device. It does not consider PCB layout constraints.

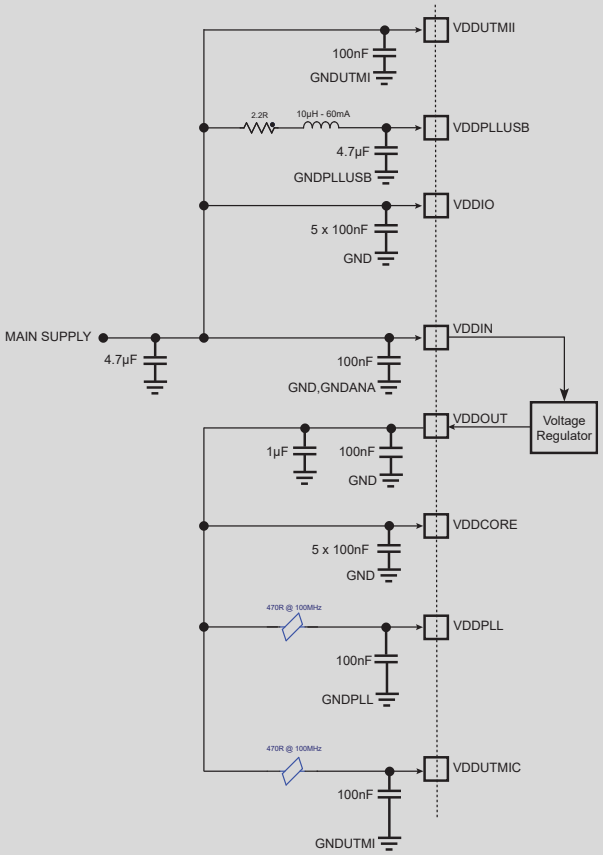
This information is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible. The checklist contains a column for use by designers, making it easy to track and verify each line item.

60.1 Power Supplies

60.1.1 Supplying the Device With Only One Supply

⚠ CAUTION To guarantee reliable operation of the device, the board design must comply with powerup and powerdown sequence guidelines provided in the "Power Considerations" chapter.

Power Supplies Schematic Example with Internal Regulator Use



Note: Component values are given only as a typical example.

Note: