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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	44
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70j21b-ant

Offset	Name	Bit Pos.								
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x64 ... 0x7F	Reserved									
0x80	MATRIX_PRAS0	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x84	MATRIX_PRBS0	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0x88	MATRIX_PRAS1	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x8C	MATRIX_PRBS1	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0x90	MATRIX_PRAS2	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x94	MATRIX_PRBS2	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0x98	MATRIX_PRAS3	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x9C	MATRIX_PRBS3	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0xA0	MATRIX_PRAS4	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0xA4	MATRIX_PRBS4	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0xA8	MATRIX_PRAS5	7:0			M1PR[1:0]				M0PR[1:0]	

32.6.1.40 PIO Level Select Register

Name: PIO_LSR
Offset: 0x00C4
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Level Interrupt Selection

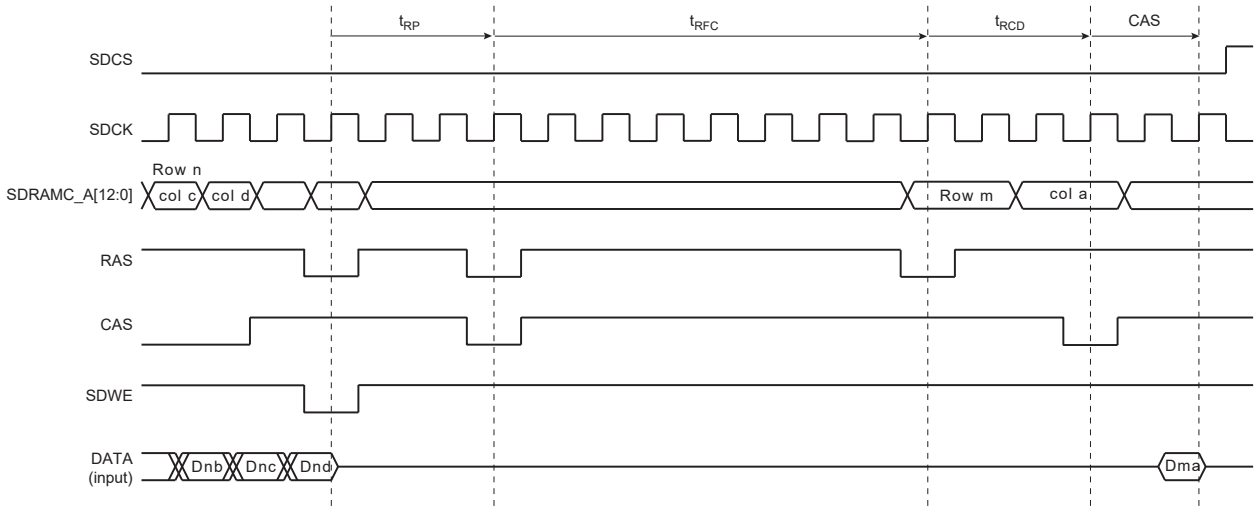
Value	Description
0	No effect.
1	The interrupt source is a level-detection event.

generates these autorefresh commands periodically. An internal timer is loaded with the value in SDRAMC_TR that indicates the number of clock cycles between refresh cycles.

A refresh error interrupt is generated when the previous autorefresh command did not perform. It is acknowledged by reading the Interrupt Status register (SDRAMC_ISR).

When the SDRAMC initiates a refresh of the SDRAM device, internal memory accesses are not delayed. However, if the processor tries to access the SDRAM, the slave indicates that the device is busy and the master is held by a wait signal. Refer to the following figure.

Figure 34-5. Refresh Cycle Followed by a Read Access



34.6.5 Power Management

Three low-power modes are available:

- Self-refresh mode: The SDRAM executes its own Autorefresh cycle without control of the SDRAMC. Current drained by the SDRAM is very low.
- Powerdown mode: Autorefresh cycles are controlled by the SDRAMC. Between autorefresh cycles, the SDRAM is in powerdown. Current drained in Powerdown mode is higher than in Self-refresh Mode.
- Deep Powerdown mode (only available with Mobile SDRAM): The SDRAM contents are lost, but the SDRAM does not drain any current.

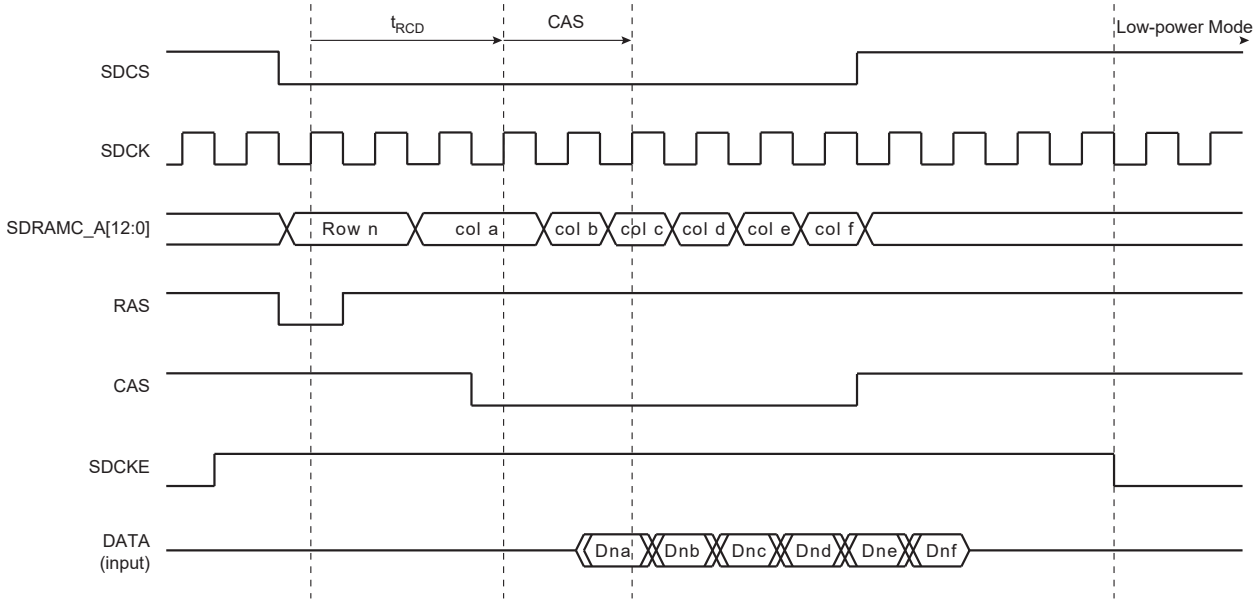
The SDRAMC activates one low-power mode as soon as the SDRAM device is not selected. It is possible to delay the entry in Self-refresh and Powerdown modes after the last access by programming a timeout value in the SDRAMC_LPR.

34.6.5.1 Self-refresh Mode

This mode is selected by configuring SDRAMC_LPR.LPCB to 1. In Self-refresh mode, the SDRAM device retains data without external clocking and provides its own internal clocking, thus performing its own autorefresh cycles. All the inputs to the SDRAM device become “don’t care” except SDCKE, which remains low. As soon as the SDRAM device is selected, the SDRAMC provides a sequence of commands and exits Self-refresh mode.

Some low-power SDRAMs (e.g., mobile SDRAM) can refresh only one-quarter or a half quarter or all banks of the SDRAM array. This feature reduces the self-refresh current. To configure this feature, Temperature Compensated Self-Refresh (TCSR), Partial Array Self-Refresh (PASR) and Drive Strength (DS) must be set in the SDRAMC_LPR and transmitted to the low-power SDRAM during initialization.

Figure 34-7. Low-power Mode Behavior



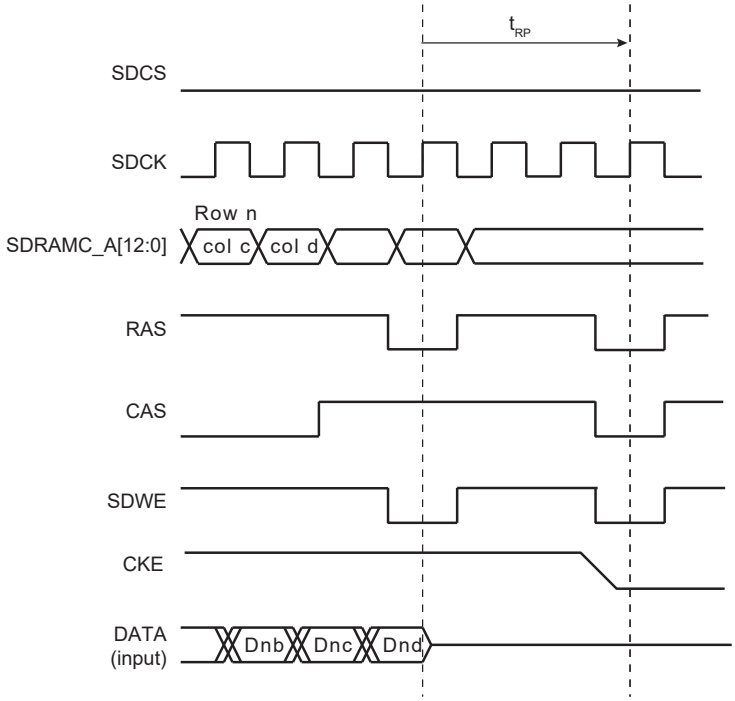
34.6.5.3 Deep Powerdown Mode

This mode is selected by configuring SDRAMC_LPR.LPCB to 3. When this mode is activated, all internal voltage generators inside the SDRAM are stopped and all data is lost.

When this mode is enabled, the application must not access the SDRAM until a new initialization sequence is done (see “SDRAM Device Initialization”).

Refer to the following figure.

Figure 34-8. Deep Powerdown Mode Behavior



Value	Description
0	Codec datapath DMA interface requires a request to restart.
1	Codec datapath DMA automatically restarts.

Bits 10:8 – FRATE[2:0] Frame Rate [0..7]

Value	Description
0	All the frames are captured, else one frame every FRATE + 1 is captured.

Bit 7 – CRC_SYNC Embedded Synchronization Correction

Value	Description
0	No CRC correction is performed on embedded synchronization.
1	CRC correction is performed. If the correction is not possible, the current frame is discarded and the CRC_ERR bit is set in the ISI_SR.

Bit 6 – EMB_SYNC Embedded Synchronization

Value	Description
0	Synchronization by HSYNC, VSYNC.
1	Synchronization by embedded synchronization sequence SAV/EAV.

Bit 5 – GRAYLE Grayscale Little Endian
Refer to Table 37-8 and Table 37-9 for details.

Value	Description
0	The two pixels are represented in big-endian format within a 32-bit register.
1	The two pixels are represented in little-endian format within a 32-bit register.

Bit 4 – PIXCLK_POL Pixel Clock Polarity

Value	Description
0	Data is sampled on rising edge of pixel clock.
1	Data is sampled on falling edge of pixel clock.

Bit 3 – VSYNC_POL Vertical Synchronization Polarity

Value	Description
0	VSYNC active high.
1	VSYNC active low.

Bit 2 – HSYNC_POL Horizontal Synchronization Polarity

Value	Description
0	HSYNC active high.
1	HSYNC active low.

Bit 11 – TXCOEN Transmitter Checksum Generation Offload Enable
Transmitter IP, TCP and UDP checksum generation offload enable.

Value	Description
0	Frame data is unaffected.
1	The transmitter checksum generation engine calculates and substitutes checksums for transmit frames.

Bit 10 – TXPBMS Transmitter Packet Buffer Memory Size Select
When written to zero, the amount of memory used for the transmit packet buffer is reduced by 50%. This reduces the amount of memory used by the GMAC.

It is important to write this bit to '1' if the full configured physical memory is available. The value in parentheses represents the size that would result for the default maximum configured memory size of 4KBytes.

Value	Description
0	Top address bits not used. (2KByte used.)
1	Full configured addressable space (4KBytes) used.

Bits 9:8 – RXBMS[1:0] Receiver Packet Buffer Memory Size Select
The default receive packet buffer size is FULL=4 Kbytes. The table below shows how to configure this memory to FULL, HALF, QUARTER or EIGHTH of the default size.

Value	Name	Description
0	EIGHTH	4/8 Kbyte Memory Size
1	QUARTER	4/4 Kbytes Memory Size
2	HALF	4/2 Kbytes Memory Size
3	FULL	4 Kbytes Memory Size

Bit 7 – ESPA Endian Swap Mode Enable for Packet Data Accesses

Value	Description
0	Little endian mode for AHB transfers selected.
1	Big endian mode for AHB transfers selected.

Bit 6 – ESMA Endian Swap Mode Enable for Management Descriptor Accesses

Value	Description
0	Little endian mode for AHB transfers selected.
1	Big endian mode for AHB transfers selected.

Bits 4:0 – FBLDO[4:0] Fixed Burst Length for DMA Data Operations
Selects the burst length to attempt to use on the AHB when transferring frame data. Not used for DMA management operations and only used where space and data size allow. Otherwise SINGLE type AHB transfers are used.

One-hot priority encoding enforced automatically on register writes as follows. ‘x’ represents don’t care.

Value	Name	Description
0	-	Reserved
1	SINGLE	00001: Always use SINGLE AHB bursts

38.8.18 GMAC RX Partial Store and Forward Register

Name: GMAC_RPSF
Offset: 0x044
Reset: 0x00000FFF
Property: -

Bit	31	30	29	28	27	26	25	24
	ENRXP							
Access	R							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RPB1ADR[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					1	1	1	1

Bit	7	6	5	4	3	2	1	0
	RPB1ADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 31 – ENRXP Enable RX Partial Store and Forward Operation

Bits 11:0 – RPB1ADR[11:0] Receive Partial Store and Forward Address
Watermark value. Reset = 1.

38.8.46 GMAC 128 to 255 Byte Frames Transmitted Register

Name: GMAC_TBFT255
Offset: 0x120
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

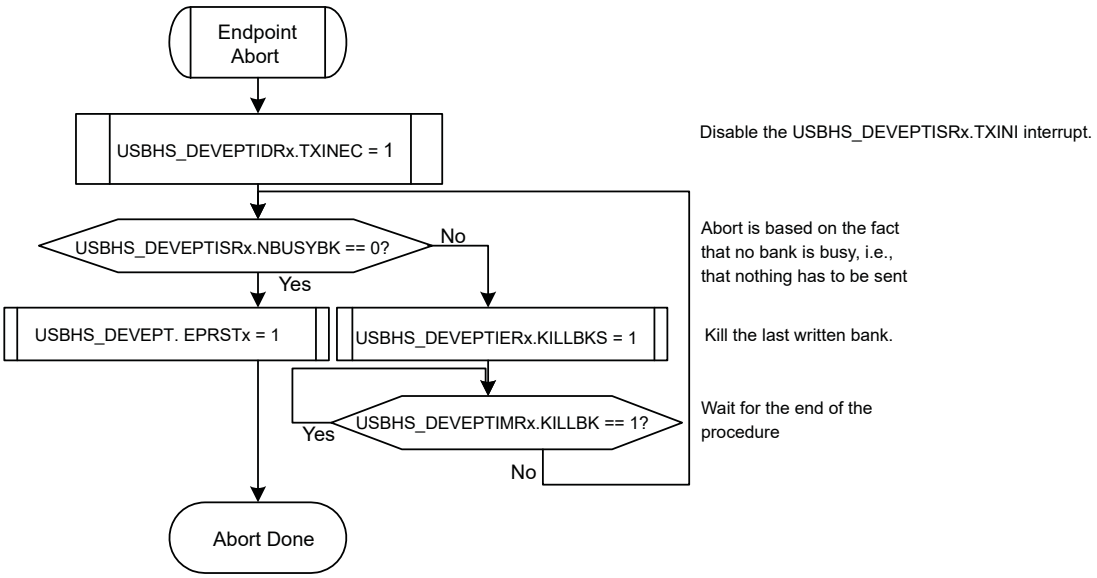
Bits 31:0 – NFTX[31:0] 128 to 255 Byte Frames Transmitted without Error
This register counts the number of 128 to 255 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

- The user writes the data into the current bank by using the USB Pipe/Endpoint nFIFO Data (USBFIFOnDATA) register, until all the data frame is written or the bank is full (in which case USBHS_DEVEPTISRx.RWALL is cleared and the Byte Count (USBHS_DEVEPTISRx.BYCT) field reaches the endpoint size).
- The user allows the controller to send the bank and switches to the next bank (if any) by clearing USBHS_DEVEPTIMRx.FIFOCON.

If the endpoint uses several banks, the current one can be written while the previous one is being read by the host. Then, when the user clears USBHS_DEVEPTIMRx.FIFOCON, the following bank may already be free and USBHS_DEVEPTISRx.TXINI is set immediately.

An “Abort” stage can be produced when a zero-length OUT packet is received during an IN stage of a control or isochronous IN transaction. The Kill IN Bank (USBHS_DEVEPTIMRx.KILLBK) bit is used to kill the last written bank. The best way to manage this abort is to apply the algorithm represented in the following figure.

Figure 39-13. Abort Algorithm



39.5.2.13 Management of OUT Endpoints

Overview

OUT packets are sent by the host. All data which acknowledges or not the bank can be read when it is empty.

The endpoint must be configured first.

The USBHS_DEVEPTISRx.RXOUTI bit is set at the same time as USBHS_DEVEPTIMRx.FIFOCON when the current bank is full. This triggers a PEP_x interrupt if the Received OUT Data Interrupt Enable (USBHS_DEVEPTIMRx.RXOUTE) bit is one.

USBHS_DEVEPTISRx.RXOUTI is cleared by software (by writing a one to the Received OUT Data Interrupt Clear (USBHS_DEVEPTICRx.RXOUTIC) bit to acknowledge the interrupt, which has no effect on the endpoint FIFO.

The user then reads from the FIFO and clears the USBHS_DEVEPTIMRx.FIFOCON bit to free the bank. If the OUT endpoint is composed of multiple banks, this also switches to the next bank. The

39.6.38 Host Frame Number Register

Name: USBHS_HSTFNUM
Offset: 0x0420
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	FLENHIGH[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			FNUM[10:5]					
Access								
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FNUM[4:0]					MFNUM[2:0]		
Access								
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – FLENHIGH[7:0] Frame Length
In High-speed mode, this field contains the 8 high-order bits of the 16-bit internal frame counter (at 30 MHz, the counter length is 3750 to ensure a SOF generation every 125 µs).

Bits 13:3 – FNUM[10:0] Frame Number
This field contains the current SOF number.

This field can be written. In this case, the MFNUM field is reset to zero.

Bits 2:0 – MFNUM[2:0] Micro Frame Number
This field contains the current microframe number (can vary from 0 to 7), updated every 125 µs.

When operating in Full-speed mode, this field is tied to zero.

Card addressing is implemented using a session address assigned during the initialization phase by the bus controller to all currently connected cards. Their unique CID number identifies individual cards.

The structure of commands, responses and data blocks is described in the High-Speed Multimedia Card System Specification. See Table 40-4 for additional information.

High-Speed Multimedia Card bus data transfers are composed of these tokens.

There are different types of operations. Addressed operations always contain a command and a response token. In addition, some operations have a data token; the others transfer their information directly within the command or response structure. In this case, no data token is present in an operation. The bits on the DAT and the CMD lines are transferred synchronous to the clock HSMCI clock.

Two types of data transfer commands are defined:

- Sequential commands—These commands initiate a continuous data stream. They are terminated only when a stop command follows on the CMD line. This mode reduces the command overhead to an absolute minimum.
- Block-oriented commands—These commands send a data block succeeded by CRC bits.

Both read and write operations allow either single or multiple block transmission. A multiple block transmission is terminated when a stop command follows on the CMD line similarly to the sequential read or when a multiple block transmission has a predefined block count (see "Data Transfer Operation").

The HSMCI provides a set of registers to perform the entire range of High-Speed Multimedia Card operations.

40.8.1 Command - Response Operation

After reset, the HSMCI is disabled and becomes valid after setting the MCIEN bit in the HSMCI_CR.

The PWSEN bit saves power by dividing the HSMCI clock by 2^{PWSDIV} + 1 when the bus is inactive.

The two bits, RDPROOF and WRPROOF in the HSMCI Mode Register (HSMCI_MR) allow stopping the HSMCI clock during read or write access if the internal FIFO is full. This will guarantee data integrity, not bandwidth.

All the timings for High Speed MultiMedia Card are defined in the High Speed MultiMedia Card System Specification.

The two bus modes (open drain and push/pull) needed to process all the operations are defined in the HSMCI Command Register (HSMCI_CMDR). The HSMCI_CMDR allows a command to be carried out.

For example, to perform an ALL_SEND_CID command:

	Host Command					N_{ID} Cycles			Response			High Impedance State		
CMD	S	T	Content	CRC	E	Z	******	Z	S	T	CID Content	Z	Z	Z

The command ALL_SEND_CID and the fields and values for the HSMCI_CMDR are described in the following two tables.

Table 40-4. ALL_SEND_CID Command Description

CMD Index	Type	Argument	Response	Abbreviation	Command Description
CMD2	bcr(1)	[31:0] stuff bits	R2	ALL_SEND_CID	Asks all cards to send their CID numbers on the CMD line

40.14.7 HSMCI Block Register

Name: HSMCI_BLKR
Offset: 0x18
Reset: 0x0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	BLKLEN[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BLKLEN[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BCNT[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BCNT[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – BLKLEN[15:0] Data Block Length
This field determines the size of the data block.

Bits 16 and 17 must be configured to 0 if FBYTE is disabled.

Note: In SDIO Byte mode, BLKLEN field is not used.

Bits 15:0 – BCNT[15:0] MMC/SDIO Block Count - SDIO Byte Count
This field determines the number of data byte(s) or block(s) to transfer.

The transfer data type and the authorized values for BCNT field are determined by the TRTYP field in the HSMCI Command Register (HSMCI_CMDR).

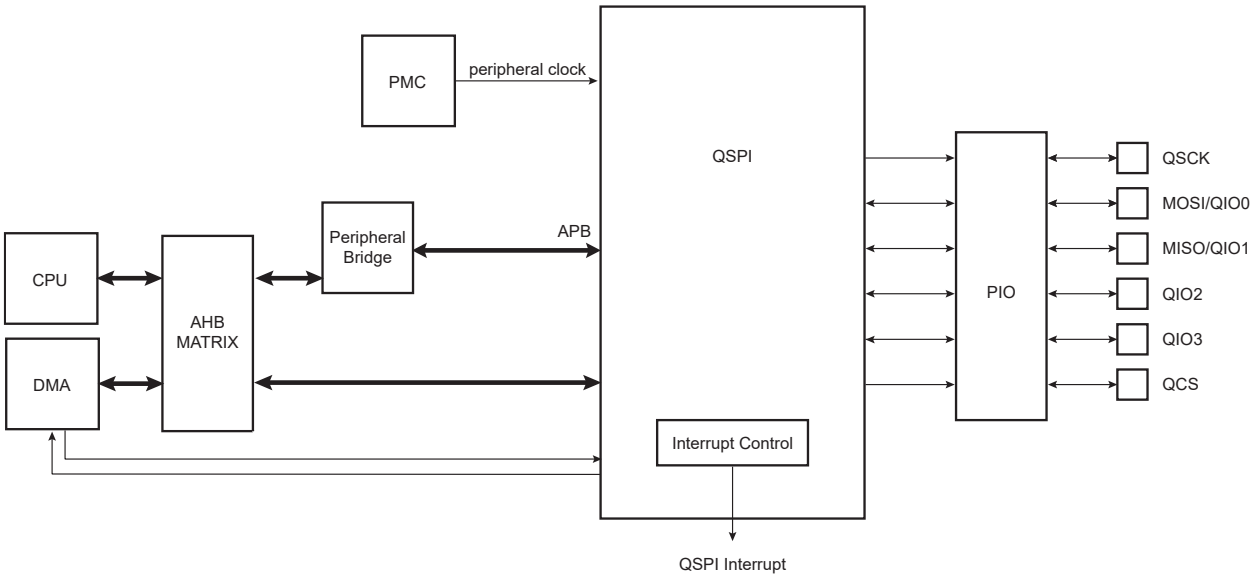
When TRTYP = 1 (MMC/SDCARD Multiple Block), BCNT can be programmed from 1 to 65535, 0 corresponds to an infinite block transfer.

When TRTYP = 4 (SDIO Byte), BCNT can be programmed from 1 to 511, 0 corresponds to 512-byte transfer. Values in range 512 to 65536 are forbidden.

When TRTYP = 5 (SDIO Block), BCNT can be programmed from 1 to 511, 0 corresponds to an infinite block transfer. Values in range 512 to 65536 are forbidden.

42.3 Block Diagram

Figure 42-1. Block Diagram



42.4 Signal Description

Table 42-1. Signal Description

Pin Name	Pin Description	Type
QSCK	Serial Clock	Output
MOSI (QIO0) (1)(2)	Data Output (Data Input Output 0)	Output (Input/Output)
MISO (QIO1) (1)(2)	Data Input (Data Input Output 1)	Input (Input/Output)
QIO2 (3)	Data Input Output 2	Input/Output
QIO3 (3)	Data Input Output 3	Input/Output
QCS	Peripheral Chip Select	Output

Note:

1. MOSI and MISO are used for single-bit SPI operation.
2. QIO0–QIO1 are used for Dual SPI operation.
3. QIO0–QIO3 are used for Quad SPI operation.

42.5 Product Dependencies

42.5.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the QSPI pins to their peripheral functions.

See Master Write with One-, Two- or Three-Byte Internal Address and One Data Byte and Internal Address Usage for the master write operation with internal address.

The three internal address bytes are configurable through TWIHS_MMR.

If the slave device supports only a 7-bit address, i.e., no internal address, IADRSZ must be set to 0.

The table below shows the abbreviations used in the figures below.

Table 43-4. Abbreviations

Abbreviation	Definition
S	Start
Sr	Repeated Start
P	Stop
W	Write
R	Read
A	Acknowledge
NA	Not Acknowledge
DADR	Device Address
IADR	Internal Address

Figure 43-10. Master Write with One-, Two- or Three-Byte Internal Address and One Data Byte

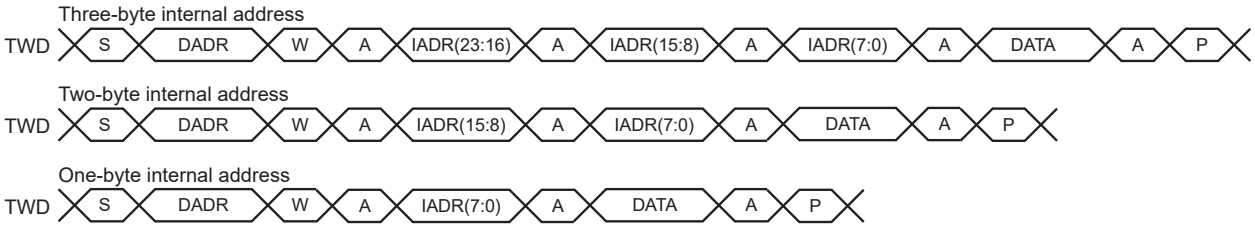
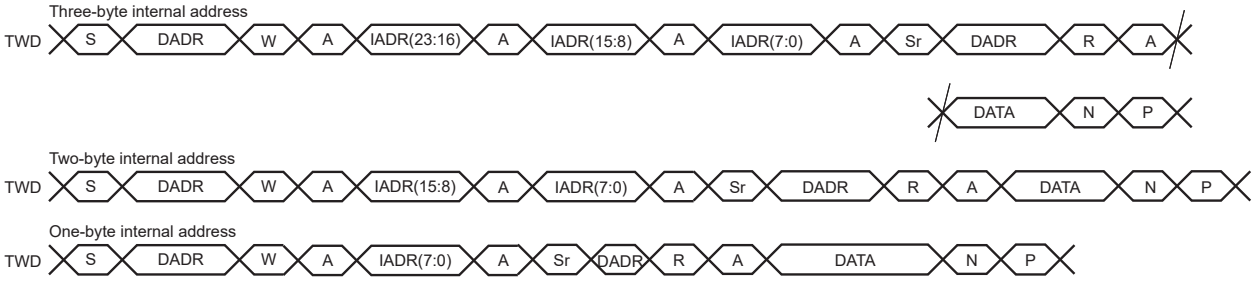


Figure 43-11. Master Read with One-, Two- or Three-Byte Internal Address and One Data Byte



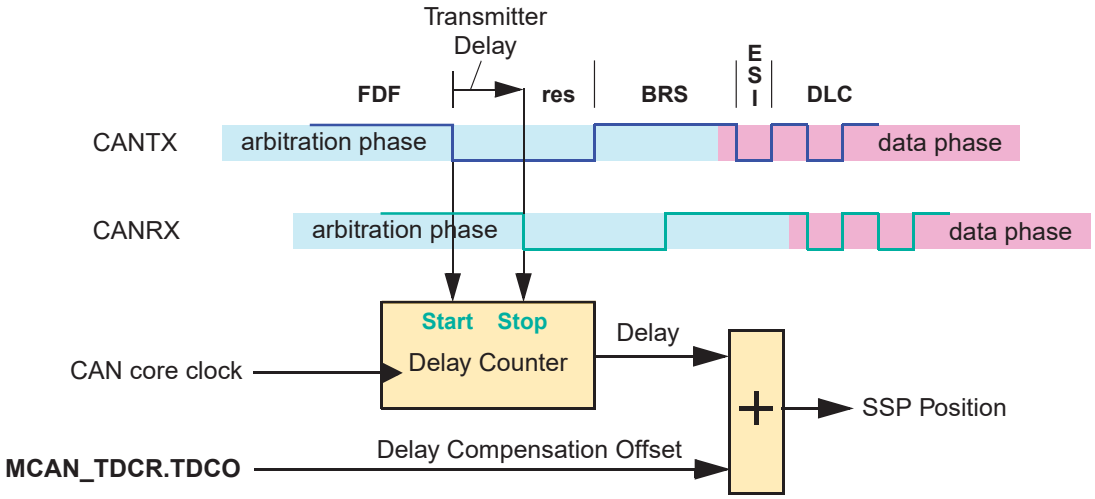
43.6.3.5.2 10-bit Slave Addressing

For a slave address higher than seven bits, configure the address size (IADRSZ) and set the other slave address bits in the Internal Address register (TWIHS_IADR). The two remaining internal address bytes, IADR[15:8] and IADR[23:16], can be used the same way as in 7-bit slave addressing.

Example: Address a 10-bit device (10-bit device address is b1 b2 b3 b4 b5 b6 b7 b8 b9 b10)

1. Program IADRSZ = 1,
2. Program DADR with 1 1 1 1 0 b1 b2 (b1 is the MSB of the 10-bit address, b2, etc.)

Figure 49-2. Transmitter Delay Measurement



To avoid that a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in a to early SSP position, the use of a transmitter delay compensation filter window can be enabled by programming MCAN_TDCR.TDCF.

This defines a minimum value for the SSP position. Dominant edges on CANRX, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least MCAN_TDCR.TDCF AND CANRX is low.

49.5.1.5 Restricted Operation Mode

In Restricted Operation mode, the node is able to receive data and remote frames and to give acknowledge to valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The error counters are not incremented. The processor can set the MCAN into Restricted Operation mode by setting bit MCAN_CCCR.ASM. The bit can only be set by the processor when both MCAN_CCCR.CCE and MCAN_CCCR.INIT are set to '1'. The bit can be reset by the processor at any time.

Restricted Operation mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation mode, the processor has to reset MCAN_CCCR.ASM.

The Restricted Operation mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation mode after it has received a valid frame.

Note: The Restricted Operation Mode must not be combined with the Loop Back mode (internal or external).

49.5.1.6 Bus Monitoring Mode

The MCAN is set in Bus Monitoring mode by setting MCAN_CCCR.MON. In Bus Monitoring mode (see ISO11898-1, 10.12 Bus monitoring), the MCAN is able to receive valid data frames and valid remote frames, but cannot start a transmission. In this mode, it sends only recessive bits on the CAN bus. If the MCAN is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the MCAN monitors this dominant bit, although the CAN bus may remain in recessive state. In Bus Monitoring mode, the Tx Buffer Request Pending register (MCAN_TXBRP) is held in reset state.

51.7.7 PWM Interrupt Mask Register 1

Name: PWM_IMR1
Offset: 0x18
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					FCHID3	FCHID2	FCHID1	FCHID0
Access					R	R	R	R
Reset					0	0	0	0

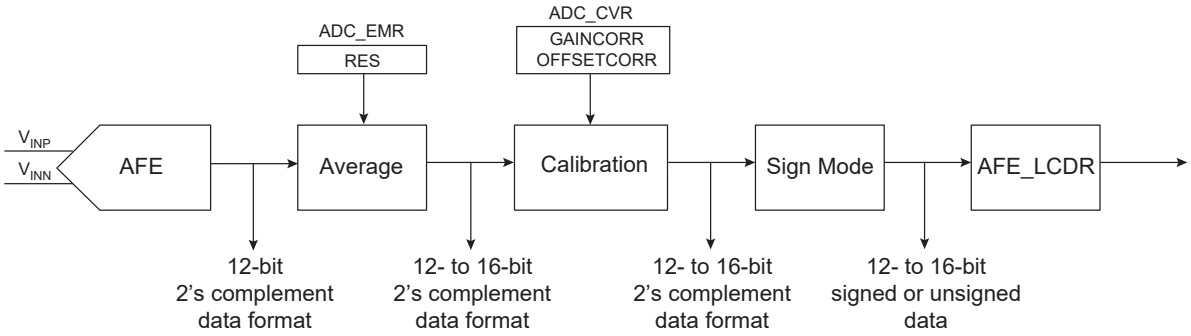
Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					CHID3	CHID2	CHID1	CHID0
Access					R	R	R	R
Reset					0	0	0	0

Bits 16, 17, 18, 19 – FCHIDx Fault Protection Trigger on Channel x Interrupt Mask

Bits 0, 1, 2, 3 – CHIDx Counter Event on Channel x Interrupt Mask

Figure 52-14. AFE Digital Signal Processing



52.6.16 Buffer Structure

The DMA read channel is triggered each time a new data is stored in AFEC_LCDR. The same structure of data is repeatedly stored in AFEC_LCDR each time a trigger event occurs. Depending on the user mode of operation (AFEC_MR, AFEC_CHSR, AFEC_SEQ1R, AFEC_SEQ2R) the structure differs. When TAG is cleared, each data transferred to DMA buffer is carried on a half-word (16-bit) and consists of the last converted data right-aligned. When TAG is set, this data is carried on a word buffer (32-bit) and CHNB carries the channel number, thus simplifying post-processing in the DMA buffer and ensuring the integrity of the DMA buffer.

52.6.17 Fault Output

The AFEC internal fault output is directly connected to the PWM fault input. Fault output may be asserted depending on the configuration of AFEC_EMR, AFEC_CWR, AFEC_TEMPMR and AFEC_TEMPCWR and converted values.

Two types of comparison can trigger a compare event (fault output pulse). The first comparison type is based on AFEC_CWR settings, thus on all converted channels except the last one; the second type is linked to the last channel where temperature is measured. As an example, overcurrent and temperature exceeding limits can trigger a fault to PWM.

When the compare occurs, the AFEC fault output generates a pulse of one peripheral clock cycle to the PWM fault input. This fault line can be enabled or disabled within the PWM. If it is activated and asserted by the AFEC, the PWM outputs are immediately placed in a safe state (pure combinational path).

Note that the AFEC fault output connected to the PWM is not the COMPE bit. Thus the Fault Mode (FMOD) within the PWM configuration must be FMOD = 1.

52.6.18 Register Write Protection

To prevent any single software error from corrupting AFEC behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the AFEC Write Protection Mode Register (AFEC_WPMR).

If a write access to a write-protected register is detected, the WPVS flag in the AFEC Write Protection Status Register (AFEC_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS flag is automatically cleared by reading the AFEC_WPSR.

The protected registers are:

- AFEC Mode Register
- AFEC Extended Mode Register

57.5.4 AES Interrupt Disable Register

Name: AES_IDR
Offset: 0x14
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								TAGRDY
Access								W
Reset								–

Bit	15	14	13	12	11	10	9	8
								URAD
Access								W
Reset								–

Bit	7	6	5	4	3	2	1	0
								DATRDY
Access								W
Reset								–

Bit 16 – TAGRDY GCM Tag Ready Interrupt Disable

Bit 8 – URAD Unspecified Register Access Detection Interrupt Disable

Bit 0 – DATRDY Data Ready Interrupt Disable

Symbol	Parameter	Condition	Min	Max	Unit
V_{hys}	Hysteresis of Schmitt Trigger Inputs	–	0.150	–	V
V_{OL}	Low-level Output Voltage	3 mA sink current	–	0.4	V
t_R	Rise Time for both TWD and TWCK		$20 + 0.1C_b$(1)(2)	300	ns
t_{OF}	Output Fall Time from V_{IHmin} to V_{ILmax}	10 pF < C_b < 400 pF see the figure below	$20 + 0.1C_b$(1)(2)	250	ns
C_i(1)	Capacitance for each I/O Pin	–	–	10	pF
f_{TWCK}	TWCK Clock Frequency	–	0	400	kHz
R_P	Value of Pull-up resistor	$f_{TWCK} \le 100$ kHz	(V_{DDIO} - 0.4V) ÷ 3mA	1000ns ÷ C_b	Ω
		$f_{TWCK} > 100$ kHz		300ns ÷ C_b	Ω
t_{LOW}	Low Period of the TWCK clock	$f_{TWCK} \le 100$ kHz	(3)	–	µs
		$f_{TWCK} > 100$ kHz	(3)	–	µs
t_{HIGH}	High period of the TWCK clock	$f_{TWCK} \le 100$ kHz	(4)	–	µs
		$f_{TWCK} > 100$ kHz	(4)	–	µs
$t_{HD;STA}$	Hold Time (repeated) START Condition	$f_{TWCK} \le 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{TWCK} \le 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs
$t_{HD;DAT}$	Data hold time	$f_{TWCK} \le 100$ kHz	0	3 × t_{CPMCK}(5)	µs
		$f_{TWCK} > 100$ kHz	0	3 ×t_{CPMCK}(5)	µs
$t_{SU;DAT}$	Data setup time	$f_{TWCK} \le 100$ kHz	t_{LOW} - 3 × t_{CPMCK}(5)	–	ns
		$f_{TWCK} > 100$ kHz	t_{LOW} - 3 × t_{CPMCK}(5)	–	ns
$t_{SU;STO}$	Setup time for STOP condition	$f_{TWCK} \le 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs
$t_{HD;STA}$	Hold Time (repeated) START Condition	$f_{TWCK} \le 100$ kHz	t_{HIGH}	–	µs
		$f_{TWCK} > 100$ kHz	t_{HIGH}	–	µs

Note:

1. Required only for $f_{TWCK} > 100$ kHz.
2. C_b = capacitance of one bus line in pF. Per I^2C standard, C_b max = 400pF.
3. The TWCK low period is defined as follows: $t_{LOW} = ((CLDIV \times 2^{CKDIV}) + 4) \times t_{MCK}$.
4. The TWCK high period is defined as follows: $t_{HIGH} = ((CHDIV \times 2^{CKDIV}) + 4) \times t_{MCK}$.

Date	Comments
01-June-16	Section 42. “Quad SPI Interface (QSPI)” Section 42.2 “Embedded Characteristics”: added bullet on Single Data Rate and Double Data Rate modes. Figure 42-2 “QSPI Transfer Format (QSPI_SCR.CPHA = 0, 8 bits per transfer)” and Figure 42-3 “QSPI Transfer Format (QSPI_SCR.CPHA = 1, 8 bits per transfer)””: modified NSS to QCS. Section 42.7.2 “QSPI Mode Register”: updated CSMODE description. Section 42.7.5 “QSPI Status Register”: updated descriptions of bits CSR and INSTRE.
	Section 43. “Two-wire Interface (TWIHS)” Updated Figure 43-1 “Block Diagram”. Section 43.6.3.9 “SMBus Mode”: deleted bullet on SMBALERT. Section 43.6.5.6 “SMBus Mode”: deleted bullet on SMBALERT. Section 43.7.5 “TWIHS Clock Waveform Generator Register”: Bit 20 now ‘reserved’ (was CKSRC: Transfer Rate Clock Source). HOLD field extended to 6 bits.
	Section 44. “Synchronous Serial Controller (SSC)” in Figure 44-19 “Interrupt Block Diagram”: renamed RXSYNC to RXSYN; renamed TXSYNC to TXSYN.
	Section 45. “Inter-IC Sound Controller (I2SC)” Throughout: In text, tables and figures, pin names changed to: - I2SC_MCK - I2SC_CK - I2SC_WS - I2SC_DI - I2SC_DO Updated Figure 45-1 “I2SC Block Diagram”. Section 45.6.1 “Initialization”: modified register name from CCFG_I2SCLKSEL to CCFG_PCCR. Section 45.6.5 “Serial Clock and Word Select Generation”: updated paragraph on I2SC input clock selection in Master mode. Updated Figure 45-3 “I2SC Clock Generation”. Section 45.8.2 “I2SC Mode Register”: updated MODE bit description for value ‘1’. Updated IMCKDIV and IMCKMODE field descriptions.
	Section 46. “Universal Synchronous Asynchronous Receiver Transceiver (USART)” Section 46.2 “Embedded Characteristics”: added bullet “Optimal for Node-to-Node Communication (no embedded digital line filter)” to LON Mode features.