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Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70n19a-cn

SAM E70/S70/V70/V71 Family

Power Management Controller (PMC)

31.20.3 PMC System Clock Status Register

Name: PMC_SCSR
Offset: 0x0008
Reset: 0x00000001
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PCK7	PCK6	PCK5	PCK4	PCK3	PCK2	PCK1	PCK0
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			USBCLK					HCLKS
Access								
Reset			0					1

Bits 8, 9, 10, 11, 12, 13, 14, 15 – PCK Programmable Clock x Output Status

Value	Description
0	The corresponding Programmable Clock output is disabled.
1	The corresponding Programmable Clock output is enabled.

Bit 5 – USBCLK USB FS Clock Status

Value	Description
0	The USB FS clock is disabled.
1	The USB FS clock is enabled.

Bit 0 – HCLKS HCLK Status

Value	Description
0	HCLK is disabled.
1	HCLK is enabled.

SAM E70/S70/V70/V71 Family

Parallel Input/Output Controller (PIO)

The filters also introduce some latencies, illustrated in the following two figures.

The glitch filters are controlled by the Input Filter Enable Register (PIO_IFER), the Input Filter Disable Register (PIO_IFDR) and the Input Filter Status Register (PIO_IFSR). Writing PIO_IFER and PIO_IFDR respectively sets and clears bits in PIO_IFSR. This last register enables the glitch filter on the I/O lines.

When the glitch and/or debouncing filter is enabled, it does not modify the behavior of the inputs on the peripherals. It acts only on the value read in PIO_PDSR and on the input change interrupt detection. The glitch and debouncing filters require that the peripheral clock is enabled.

Figure 32-4. Input Glitch Filter Timing

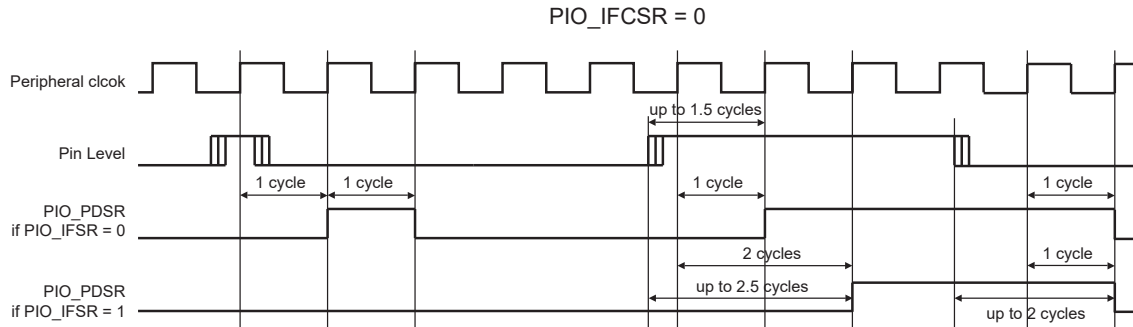
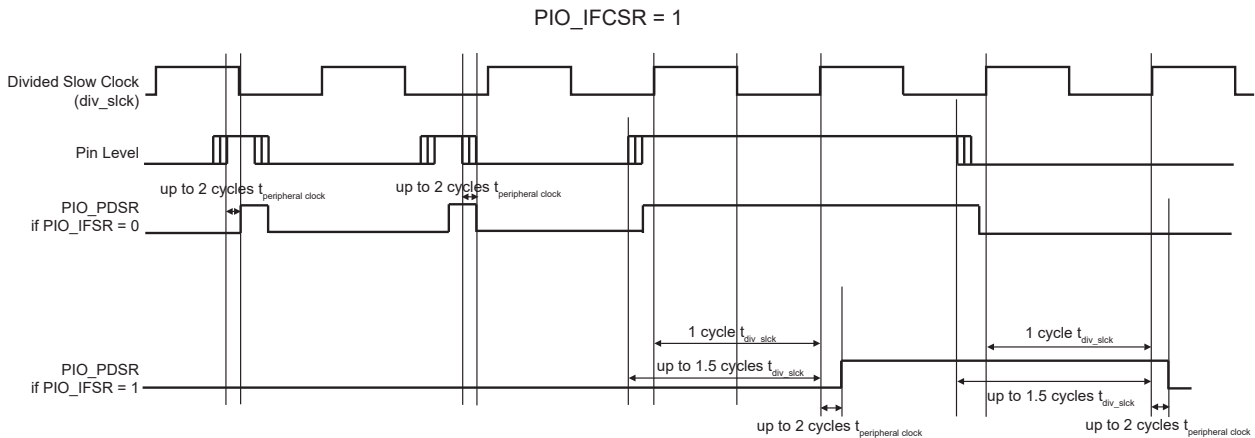


Figure 32-5. Input Debouncing Filter Timing



32.5.10 Input Edge/Level Interrupt

The PIO Controller can be programmed to generate an interrupt when it detects an edge or a level on an I/O line. The Input Edge/Level interrupt is controlled by writing the Interrupt Enable Register (PIO_IER) and the Interrupt Disable Register (PIO_IDR), which enable and disable the input change interrupt respectively by setting and clearing the corresponding bit in the Interrupt Mask Register (PIO_IMR). As input change detection is possible only by comparing two successive samplings of the input of the I/O line, the peripheral clock must be enabled. The Input Change interrupt is available regardless of the configuration of the I/O line, i.e., configured as an input only, controlled by the PIO Controller or assigned to a peripheral function.

By default, the interrupt can be generated at any time an edge is detected on the input.

Some additional interrupt modes can be enabled/disabled by writing in the Additional Interrupt Modes Enable Register (PIO_AIMER) and Additional Interrupt Modes Disable Register (PIO_AIMDR). The current state of this selection can be read through the Additional Interrupt Modes Mask Register (PIO_AIMMR).

SAM E70/S70/V70/V71 Family

Parallel Input/Output Controller (PIO)

32.6.1.41 PIO Edge/Level Status Register

Name: PIO_ELSR
Offset: 0x00C8
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Edge/Level Interrupt Source Selection

Value	Description
0	The interrupt source is an edge-detection event.
1	The interrupt source is a level-detection event.

SAM E70/S70/V70/V71 Family

Parallel Input/Output Controller (PIO)

32.6.1.50 PIO Parallel Capture Mode Register

Name: PIO_PCMR
Offset: 0x0150
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the [PIO Write Protection Mode Register](#).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
					FRSTS	HALFS	ALWYS	
Access								
Reset					0	0	0	
Bit	7	6	5	4	3	2	1	0
			DSIZE[1:0]					PCEN
Access								
Reset			0	0				0

Bit 11 – FRSTS Parallel Capture Mode First Sample

This bit is useful only if the HALFS bit is set to 1. If data are numbered in the order that they are received with an index from 0 to n:

Value	Description
0	Only data with an even index are sampled.
1	Only data with an odd index are sampled.

Bit 10 – HALFS Parallel Capture Mode Half Sampling

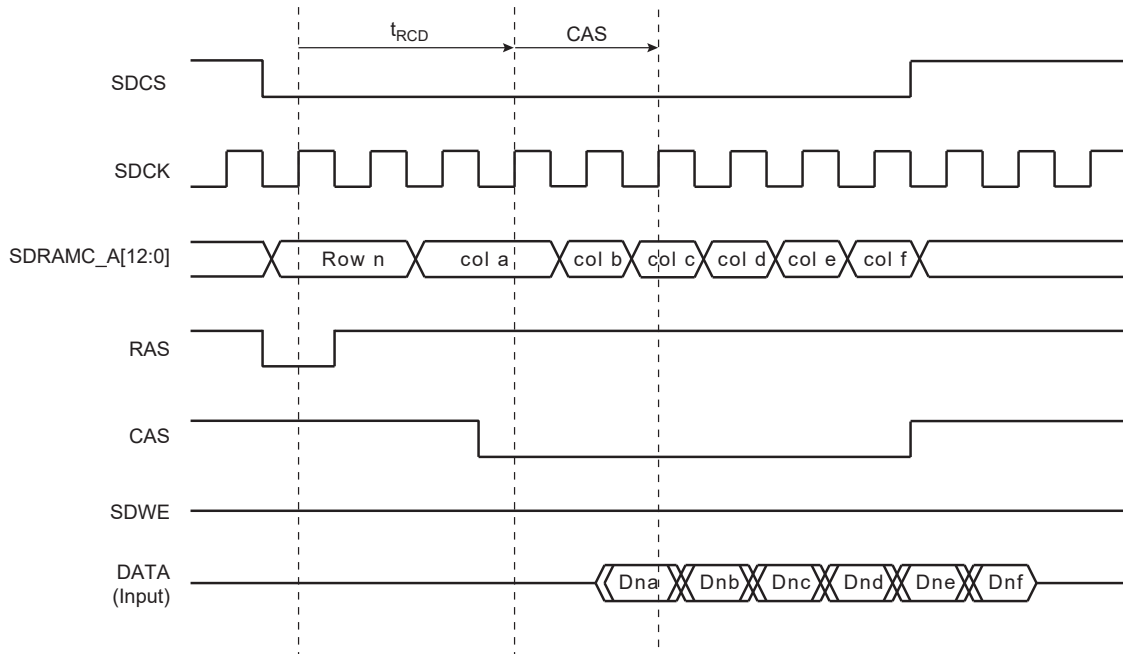
Independently from the ALWYS bit:

Value	Description
0	The Parallel Capture mode samples all the data.
1	The Parallel Capture mode samples the data only every other time.

Bit 9 – ALWYS Parallel Capture Mode Always Sampling

Value	Description
0	The Parallel Capture mode samples the data when both data enables are active.
1	The Parallel Capture mode samples the data whatever the data enables are.

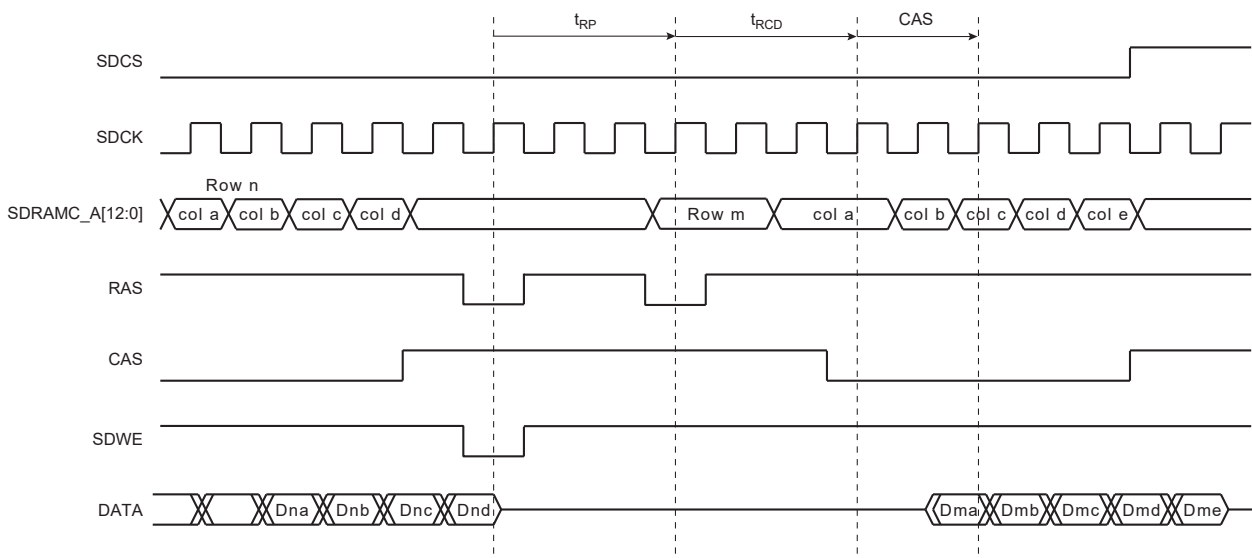
Figure 34-3. Read Burst SDRAM Access



34.6.3 Border Management

When the memory row boundary has been reached, an automatic page break is inserted. In this case, the SDRAMC generates a precharge command, activates the new row and initiates a read or write command. To comply with SDRAM timing parameters, an additional clock cycle is inserted between the precharge and the active command (t_{RP}) and between the active and the read command (t_{RCD}). Refer to the following figure.

Figure 34-4. Read Burst with Boundary Row Access



34.6.4 SDRAM Controller Refresh Cycles

An autorefresh command is used to refresh the SDRAM device. Refresh addresses are generated internally by the SDRAM device and incremented after each autorefresh automatically. The SDRAMC

SAM E70/S70/V70/V71 Family

Image Sensor Interface (ISI)

Offset	Name	Bit Pos.								
0x28	ISI_SR	7:0						SRST	DIS_DONE	ENABLE
		15:8						VSYNC		CDC_PND
		23:16					SIP		CXFR_DONE	PXFR_DONE
		31:24					FR_OVR	CRC_ERR	C_OVR	P_OVR
0x2C	ISI_IER	7:0						SRST	DIS_DONE	
		15:8						VSYNC		
		23:16							CXFR_DONE	PXFR_DONE
		31:24					FR_OVR	CRC_ERR	C_OVR	P_OVR
0x30	ISI_IDR	7:0						SRST	DIS_DONE	
		15:8						VSYNC		
		23:16							CXFR_DONE	PXFR_DONE
		31:24					FR_OVR	CRC_ERR	C_OVR	P_OVR
0x34	ISI_IMR	7:0						SRST	DIS_DONE	
		15:8						VSYNC		
		23:16							CXFR_DONE	PXFR_DONE
		31:24					FR_OVR	CRC_ERR	C_OVR	P_OVR
0x38	ISI_DMA_CHER	7:0							C_CH_EN	P_CH_EN
		15:8								
		23:16								
		31:24								
0x3C	ISI_DMA_CHDR	7:0							C_CH_DIS	P_CH_DIS
		15:8								
		23:16								
		31:24								
0x40	ISI_DMA_CHSR	7:0							C_CH_S	P_CH_S
		15:8								
		23:16								
		31:24								
0x44	ISI_DMA_P_ADDR	7:0	P_ADDR[5:0]							
		15:8	P_ADDR[13:6]							
		23:16	P_ADDR[21:14]							
		31:24	P_ADDR[29:22]							
0x48	ISI_DMA_P_CTRL	7:0					P_DONE	P_IEN	P_WB	P_FETCH
		15:8								
		23:16								
		31:24								
0x4C	ISI_DMA_P_DSCR	7:0	P_DSCR[5:0]							
		15:8	P_DSCR[13:6]							
		23:16	P_DSCR[21:14]							
		31:24	P_DSCR[29:22]							
0x50	ISI_DMA_C_ADDR	7:0	C_ADDR[5:0]							
		15:8	C_ADDR[13:6]							
		23:16	C_ADDR[21:14]							
		31:24	C_ADDR[29:22]							
0x54	ISI_DMA_C_CTRL	7:0					C_DONE	C_IEN	C_WB	C_FETCH
		15:8								

SAM E70/S70/V70/V71 Family

GMAC - Ethernet MAC

Value	Name	Description
2	-	Reserved
4	INCR4	001xx: Attempt to use INCR4 AHB bursts (Default)
8	INCR8	01xxx: Attempt to use INCR8 AHB bursts
16	INCR16	1xxxx: Attempt to use INCR16 AHB bursts

38.8.89 GMAC PTP Event Frame Transmitted Seconds Low Register

Name: GMAC_EFTSL

Offset: 0x1E0

Reset: 0x00000000

Property: Read-only

Bit	31	30	29	28	27	26	25	24
	RUD[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RUD[31:0] Register Update

The register is updated with the value that the IEEE 1588 Timer Seconds Register holds when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the register is updated.

SAM E70/S70/V70/V71 Family

USB High-Speed Interface (USBHS)

Offset	Name	Bit Pos.								
0x0754	USBHS_HSTDMAA DDRESSx	7:0	BUFF_ADD[7:0]							
		15:8	BUFF_ADD[15:8]							
		23:16	BUFF_ADD[23:16]							
		31:24	BUFF_ADD[31:24]							
0x0758	USBHS_HSTDMAC ONTROLx	7:0	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
		15:8								
		23:16	BUFF_LENGTH[7:0]							
		31:24	BUFF_LENGTH[15:8]							
0x075C	USBHS_HSTDMAS TATUSx	7:0		DESC_LDST	END_BF_ST	END_TR_ST			CHANN_ACT	CHANN_ENB
		15:8								
		23:16	BUFF_COUNT[7:0]							
		31:24	BUFF_COUNT[15:8]							
0x0760	USBHS_HSTDMAN XTDSC7	7:0	NXT_DSC_ADD[7:0]							
		15:8	NXT_DSC_ADD[15:8]							
		23:16	NXT_DSC_ADD[23:16]							
		31:24	NXT_DSC_ADD[31:24]							
0x0764	USBHS_HSTDMAA DDRESSx	7:0	BUFF_ADD[7:0]							
		15:8	BUFF_ADD[15:8]							
		23:16	BUFF_ADD[23:16]							
		31:24	BUFF_ADD[31:24]							
0x0768	USBHS_HSTDMAC ONTROLx	7:0	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
		15:8								
		23:16	BUFF_LENGTH[7:0]							
		31:24	BUFF_LENGTH[15:8]							
0x076C	USBHS_HSTDMAS TATUSx	7:0		DESC_LDST	END_BF_ST	END_TR_ST			CHANN_ACT	CHANN_ENB
		15:8								
		23:16	BUFF_COUNT[7:0]							
		31:24	BUFF_COUNT[15:8]							
0x0770 ... 0x07FF	Reserved									
0x0800	USBHS_CTRL	7:0				RDERRE				
		15:8	USBE	FRZCLK						VBUSHWC
		23:16								
		31:24						UIMOD	UID	
0x0804	USBHS_SR	7:0				RDERRI				
		15:8		CLKUSABLE	SPEED[1:0]					
		23:16								
		31:24								
0x0808	USBHS_SCR	7:0				RDERRIC				
		15:8								
		23:16								
		31:24								
0x080C	USBHS_SFR	7:0				RDERRIS				
		15:8						VBUSRQS		

SAM E70/S70/V70/V71 Family

USB High-Speed Interface (USBHS)

39.6.45 Host Pipe x Status Register (Control, Bulk Pipes)

Name: USBHS_HSTPIISR_x
Offset: 0x0530 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if PTYPE = 0x0 or 0x2 in "Host Pipe x Configuration Register".

Bit	31	30	29	28	27	26	25	24
		PBYCT[10:4]						
Access								
Reset		0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	PBYCT[3:0]					CFGOK		RWALL
Access								
Reset	0	0	0	0		0		0
Bit	15	14	13	12	11	10	9	8
	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
Access								
Reset	0	0	0	0			0	0
Bit	7	6	5	4	3	2	1	0
	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
Access								
Reset	0	0	0	0	0	0	0	0

Bits 30:20 – PBYCT[10:0] Pipe Byte Count

This field contains the byte count of the FIFO.

For an OUT pipe, the field is incremented after each byte written by the user into the pipe and decremented after each byte sent to the peripheral.

For an IN pipe, the field is incremented after each byte received from the peripheral and decremented after each byte read by the user from the pipe.

This field may be updated 1 clock cycle after the RWALL bit changes, so the user should not poll this field as an interrupt bit.

Bit 18 – CFGOK Configuration OK Status

This bit is set/cleared when the USBHS_HSTPIPCFGx.ALLOC bit is set.

This bit is set if the pipe x number of banks (USBHS_HSTPIPCFGx.PBK) and size (USBHS_HSTPIPCFGx.PSIZE) are correct compared to the maximal allowed number of banks and size for this pipe and to the maximal FIFO size (i.e., the DPRAM size).

If this bit is cleared, the user should rewrite correct values for the PBK and PSIZE fields in the USBHS_HSTPIPCFGx register.

SAM E70/S70/V70/V71 Family

High-Speed Multimedia Card Interface (HSMCI)

40.14 Register Summary

Offset	Name	Bit Pos.									
0x00	HSMCI_CR	7:0	SWRST				PWSDIS	PWSEN	MCIDIS	MCIEN	
		15:8									
		23:16									
		31:24									
0x00	HSMCI_FIFOn [x=0..255]	7:0	DATA[7:0]								
		15:8	DATA[15:8]								
		23:16	DATA[23:16]								
		31:24	DATA[31:24]								
0x04	HSMCI_MR	7:0	CLKDIV[7:0]								
		15:8		PADV	FBYTE	WRPROOF	RDPROOF	PWSDIV[2:0]			
		23:16								CLKODD	
		31:24									
0x08	HSMCI_DTOR	7:0		DTOMUL[2:0]			DTCYC[3:0]				
		15:8									
		23:16									
		31:24									
0x0C	HSMCI_SDCR	7:0	SDCBUS[1:0]				SDCSEL[1:0]				
		15:8									
		23:16									
		31:24									
0x10	HSMCI_ARGR	7:0	ARG[7:0]								
		15:8	ARG[15:8]								
		23:16	ARG[23:16]								
		31:24	ARG[31:24]								
0x14	HSMCI_CMDR	7:0	RSPTYP[1:0]		CMDNB[5:0]						
		15:8				MAXLAT	OPDCMD	SPCMD[2:0]			
		23:16			TRTYP[2:0]			TRDIR	TRCMD[1:0]		
		31:24					BOOT_ACK	ATACS	IOSPCMD[1:0]		
0x18	HSMCI_BLKRR	7:0	BCNT[7:0]								
		15:8	BCNT[15:8]								
		23:16	BLKLEN[7:0]								
		31:24	BLKLEN[15:8]								
0x1C	HSMCI_CSTOR	7:0		CSTOMUL[2:0]			CSTOCYC[3:0]				
		15:8									
		23:16									
		31:24									
0x20	HSMCI_RSRR	7:0	RSP[7:0]								
		15:8	RSP[15:8]								
		23:16	RSP[23:16]								
		31:24	RSP[31:24]								
0x24 ... 0x2F	Reserved										

41.7.3.2 Master Mode Flow Diagram

Figure 41-7. Master Mode Flow Diagram

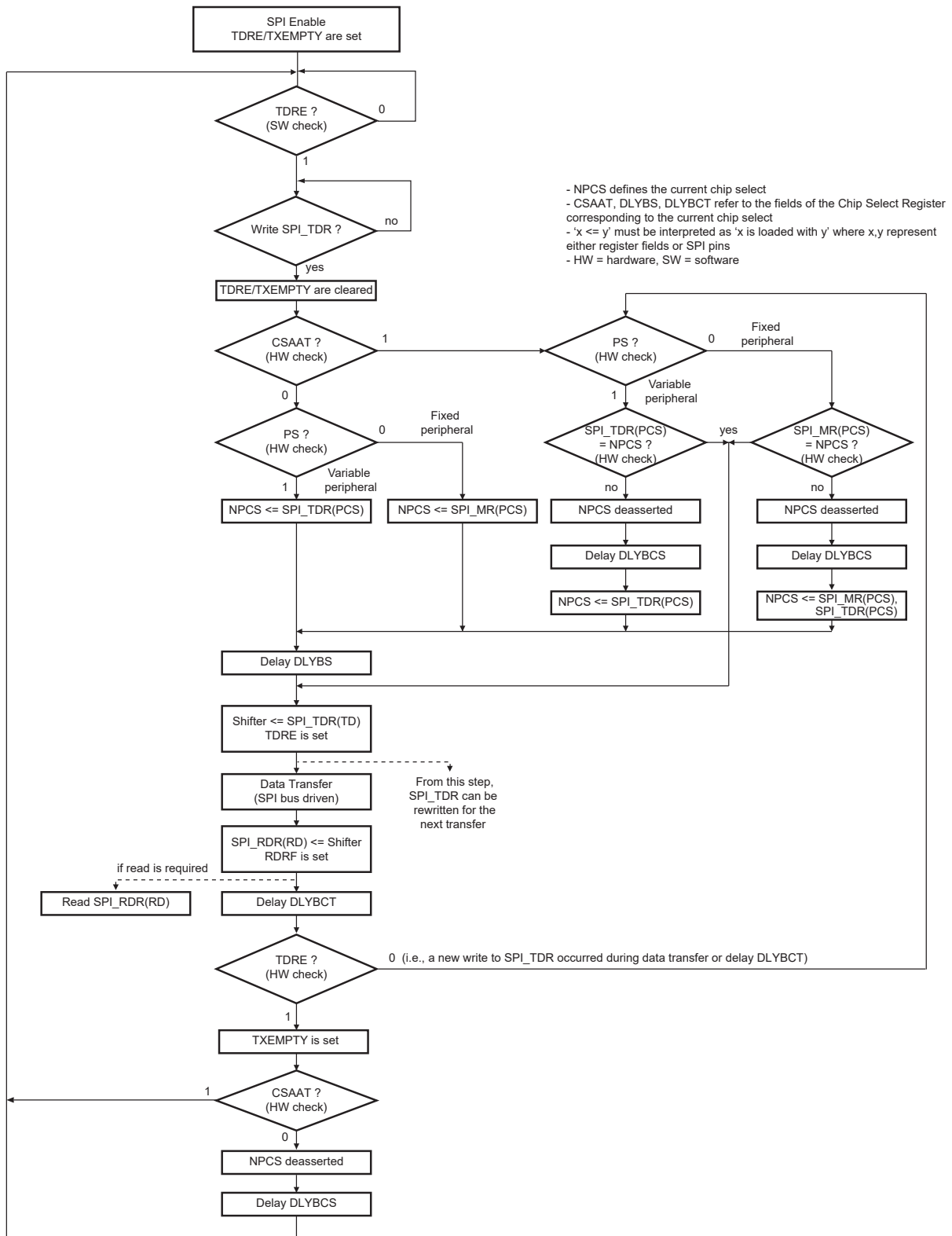
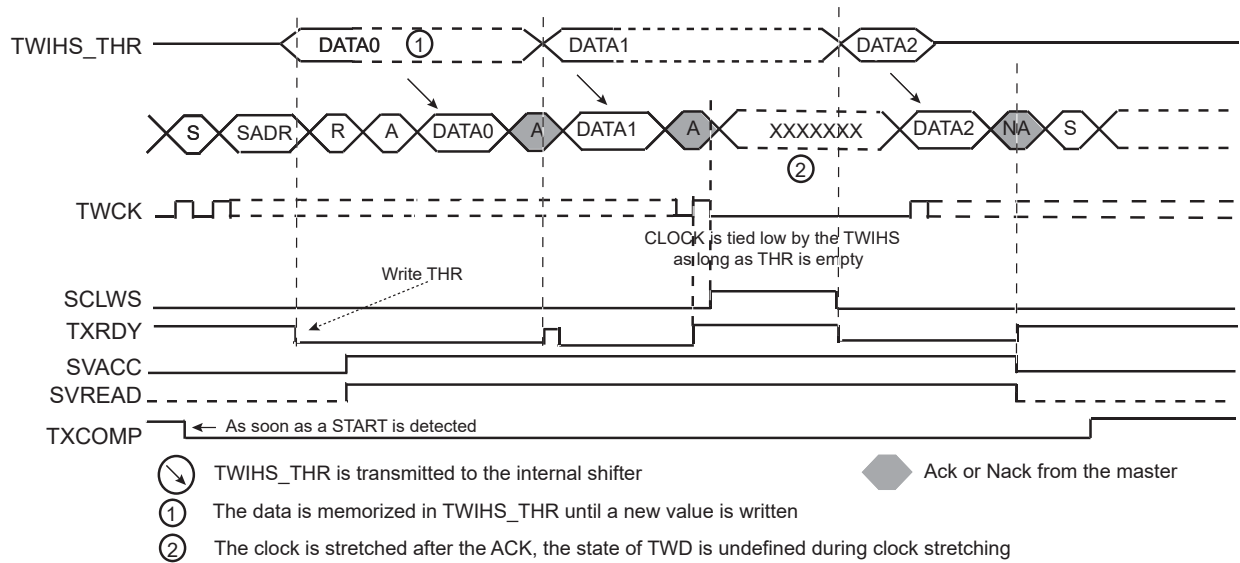


Figure 43-34. Clock Stretching in Read Mode



Note:

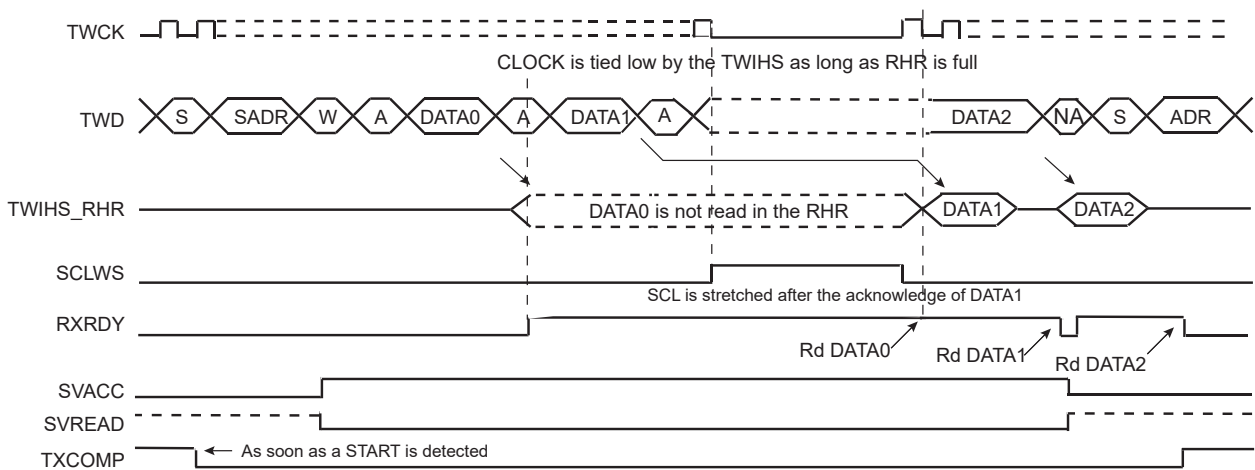
1. TXRDY is reset when data has been written in TWIHS_THR to the internal shifter and set when this data has been acknowledged or non acknowledged.
2. At the end of the read sequence, TXCOMP is set after a STOP or after a REPEATED_START + an address different from SADR.
3. SCLWS is automatically set when the clock stretching mechanism is started.

Clock Stretching in Write Mode

The clock is tied low if the internal shifter and TWIHS_RHR is full. If a STOP or REPEATED_START condition was not detected, it is tied low until TWIHS_RHR is read.

The figure below describes the clock stretching in Write mode.

Figure 43-35. Clock Stretching in Write Mode



Note:

1. At the end of the read sequence, TXCOMP is set after a STOP or after a REPEATED_START + an address different from SADR.
2. SCLWS is automatically set when the clock stretching mechanism is started and automatically reset when the mechanism is finished.

1: A data or address byte has not been acknowledged by the slave component. Set at the same time as TXCOMP.

- NACK used in Slave Read mode:

0: Each data byte has been correctly received by the master.

1: In Read mode, a data byte has not been acknowledged by the master. When NACK is set, the user must not fill TWIHS_THR even if TXRDY is set, because it means that the master stops the data transfer or re-initiate it.

Note: In Slave Write mode, all data are acknowledged by the TWIHS.

Bit 7 – UNRE Underrun Error (cleared on read)

This bit is used only if clock stretching is disabled.

Value	Description
0	TWIHS_THR has been filled on time.
1	TWIHS_THR has not been filled on time.

Bit 6 – OVRE Overrun Error (cleared on read)

This bit is used only if clock stretching is disabled.

Value	Description
0	TWIHS_RHR has not been loaded while RXRDY was set.
1	TWIHS_RHR has been loaded while RXRDY was set. Reset by read in TWIHS_SR when TXCOMP is set.

Bit 5 – GACC General Call Access (cleared on read)

This bit is used in Slave mode only.

GACC behavior can be seen in [Master Performs a General Call](#).

Value	Description
0	No general call has been detected.
1	A general call has been detected. After the detection of general call, if need be, the user may acknowledge this access and decode the following bytes and respond according to the value of the bytes.

Bit 4 – SVACC Slave Access

This bit is used in Slave mode only.

SVACC behavior can be seen in [Read Access Ordered by a Master](#), [Clock Stretching in Read Mode](#), [Repeated Start and Reversal from Read Mode to Write Mode](#) and [Repeated Start and Reversal from Write Mode to Read Mode](#).

Value	Description
0	TWIHS is not addressed. SVACC is automatically cleared after a NACK or a STOP condition is detected.
1	Indicates that the address decoding sequence has matched (A master has sent SADR). SVACC remains high until a NACK or a STOP condition is detected.

SAM E70/S70/V70/V71 Family

Synchronous Serial Controller (SSC)

Bit 5 – OVRUN Receive Overrun Interrupt Mask

Value	Description
0	The Receive Overrun Interrupt is disabled.
1	The Receive Overrun Interrupt is enabled.

Bit 4 – RXRDY Receive Ready Interrupt Mask

Value	Description
0	The Receive Ready Interrupt is disabled.
1	The Receive Ready Interrupt is enabled.

Bit 1 – TXEMPTY Transmit Empty Interrupt Mask

Value	Description
0	The Transmit Empty Interrupt is disabled.
1	The Transmit Empty Interrupt is enabled.

Bit 0 – TXRDY Transmit Ready Interrupt Mask

Value	Description
0	The Transmit Ready Interrupt is disabled.
1	The Transmit Ready Interrupt is enabled.

SAM E70/S70/V70/V71 Family

Universal Synchronous Asynchronous Receiver Transc...

46.7.7 USART Interrupt Enable Register (LIN_MODE)

Name: US_IER (LIN_MODE)
Offset: 0x0008
Property: Write-only

This configuration is relevant only if USART_MODE = 0xA or 0xB in the [USART Mode Register](#).

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
	LINHTE	LINSTE	LINSNRE	LINCE	LINIZE	LINISFE	LINBE	
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LINTC	LINID	LINBK				TXEMPTY	TIMEOUT
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PARE	FRAME	OVRE				TXRDY	RXRDY
Access								
Reset								

Bit 31 – LINHTE LIN Header Timeout Error Interrupt Enable

Bit 30 – LINSTE LIN Synch Tolerance Error Interrupt Enable

Bit 29 – LINSNRE LIN Slave Not Responding Error Interrupt Enable

Bit 28 – LINCE LIN Checksum Error Interrupt Enable

Bit 27 – LINIZE LIN Identifier Parity Interrupt Enable

Bit 26 – LINISFE LIN Inconsistent Synch Field Error Interrupt Enable

Bit 25 – LINBE LIN Bus Error Interrupt Enable

Bit 15 – LINTC LIN Transfer Completed Interrupt Enable

Bit 14 – LINID LIN Identifier Sent or LIN Identifier Received Interrupt Enable

Bit 26 – WDI Watchdog Interrupt

Value	Description
0	No Message RAM Watchdog event occurred.
1	Message RAM Watchdog event due to missing READY.

Bit 25 – BO Bus_Off Status

Value	Description
0	Bus_Off status unchanged.
1	Bus_Off status changed.

Bit 24 – EW Warning Status

Value	Description
0	Error_Warning status unchanged.
1	Error_Warning status changed.

Bit 23 – EP Error Passive

Value	Description
0	Error_Passive status unchanged.
1	Error_Passive status changed.

Bit 22 – ELO Error Logging Overflow

Value	Description
0	CAN Error Logging Counter did not overflow.
1	Overflow of CAN Error Logging Counter occurred.

Bit 19 – DRX Message stored to Dedicated Receive Buffer

The flag is set whenever a received message has been stored into a dedicated Receive Buffer.

Value	Description
0	No Receive Buffer updated.
1	At least one received message stored into a Receive Buffer.

Bit 18 – TOO Timeout Occurred

Value	Description
0	No timeout.
1	Timeout reached.

Bit 17 – MRAF Message RAM Access Failure

The flag is set, when the Rx Handler

- has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message.
- was not able to write a message to the Message RAM. In this case message storage is aborted.

In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Receive Buffer is not set, a partly stored message is overwritten when the next message is stored to this location.

54. Analog Comparator Controller (ACC)

54.1 Description

The Analog Comparator Controller (ACC) configures the analog comparator and generates an interrupt depending on user settings. The analog comparator embeds two 8-to-1 multiplexers that generate two internal inputs. These inputs are compared, resulting in a compare output. The hysteresis level, edge detection and polarity are configurable.

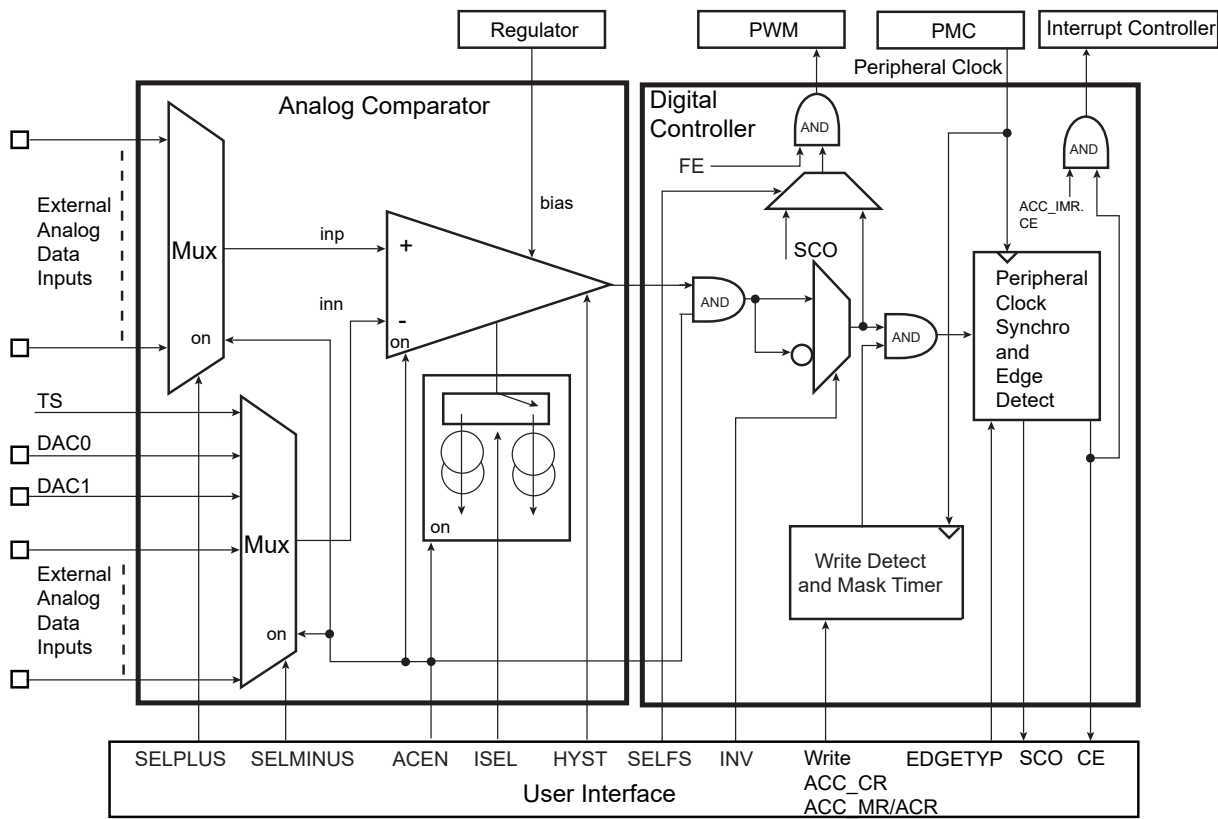
The ACC also generates a compare event which can be used by the Pulse Width Modulator (PWM).

54.2 Embedded Characteristics

- ANA_INPUTS User Analog Inputs Selectable for Comparison
- VOLT_REF Voltage References Selectable for Comparison: External Voltage Reference, DAC0, DAC1, Temperature Sensor (TS)
- Interrupt Generation
- Compare Event Fault Generation for PWM

54.3 Block Diagram

Figure 54-1. Analog Comparator Controller Block Diagram



58. Electrical Characteristics for SAM V70/V71

58.1 Absolute Maximum Ratings

Table 58-1. Absolute Maximum Ratings*

<p>Storage Temperature -60°C to + 150°C</p> <p>Voltage on Input Pins with Respect to Ground -0.3V to + 4.0V</p> <p>Maximum Operating Voltage VDDPLL, VDDUTMIC, VDDCORE 1.4V</p> <p>Maximum Operating Voltage VDDIO, VDDUTMII, VDDPLLUSB, VDDIN 4.0V</p> <p>Total DC Output Current on all I/O lines: 150 mA</p>	<p>*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.</p>
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Table 58-2. Recommended Thermal Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T _A	Operating Temperature	—	-40	—	105	°C
T _J	Junction Temperature	—	-40	—	125	°C
R _{JA}	Junction-to-ambient Thermal Resistance	TFBGA144	—	45	—	°C/W
		LQFP144	—	36	—	
		TFBGA100	—	47	—	
		LQFP100	—	41	—	
		LQFP64	—	46	—	
P _D	Power Dissipation	At T _A = 85°C, TFBGA144	—	—	—	mW
		At T _A = 105°C TFBGA144	—	—	425	
P _D	Power Dissipation	At T _A = 85°C, LQFP144	—	—	1047	mW
		At T _A = 105°C, LQFP144	—	—	523	mW

SAM E70/S70/V70/V71 Family

Electrical Characteristics for SAM E70/S70

Note:

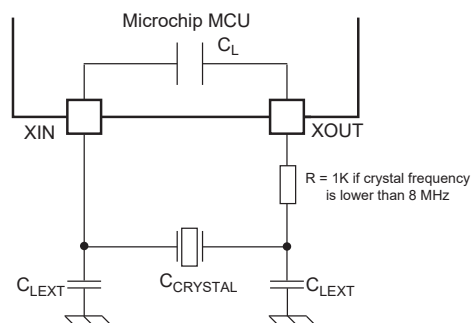
- These characteristics apply only when the 32.768 kHz crystal oscillator is in Bypass mode.

59.4.6 3 to 20 MHz Crystal Oscillator Characteristics

Table 59-23. 3 to 20 MHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	Normal mode with crystal	3	—	20	MHz
t_{START}	Startup Time	3 MHz, $C_{SHUNT} = 3 \text{ pF}$	—	—	40	ms
		12 MHz, $C_{SHUNT} = 7 \text{ pF}$ with $C_M = 1.6 \text{ fF}$	—	—	6	ms
		20 MHz, $C_{SHUNT} = 7 \text{ pF}$ with $C_M = 1.6 \text{ fF}$	—	—	5.7	ms
I_{DDON}	Current Consumption (on VDDIO)	3 MHz	—	230	—	μA
		12 MHz	—	390	—	μA
		20 MHz	—	450	—	μA
C_L	Internal Equivalent Load Capacitance	Integrated Load Capacitance	7.5	9	10.5	pF
		(X_{IN} and X_{OUT} in series)				

Figure 59-10. 3 to 20 MHz Crystal Oscillator Schematics



$$C_{LEXT} = 2 \times (C_{CRYSTAL} - C_L - C_{PCB})$$

where, C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the pin.

59.4.7 3 to 20 MHz Crystal Characteristics

Table 59-24. 3 to 20 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor	Fundamental at 3 MHz	—	—	150	Ohm
		Fundamental at 8 MHz			140	
		Fundamental at 12 MHz			120	
		Fundamental at 16 MHz			80	
		Fundamental at 20 MHz			50	
C_M	Motional capacitance	Fundamental at 3 MHz	3	—	8	fF
		Fundamental at 8–20 MHz	1.6	—	8	