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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70n20b-an

5. Automotive Quality Grade

The SAM V70 and SAM V71 devices have been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. This data sheet contains limit values extracted from the results of extensive characterization (temperature and voltage).

The quality and reliability of the SAM V70 and SAM V71 has been verified during regular product qualification as per AEC-Q100 grade 2 (–40°C to +105°C).

Table 5-1. Temperature Grade Identification for Automotive Products

Temperature (°C)	Temperature Identifier	Comments
–40°C to +105°C	B	AEC-Q100 Grade 2

24.5.3 Watchdog Timer Status Register

Name: WDT_SR
Offset: 0x08
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							WDERR	WDUNF
Access							R	R
Reset							0	0

Bit 1 – WDERR Watchdog Error (cleared on read)

Value	Description
0	No watchdog error occurred since the last read of WDT_SR.
1	At least one watchdog error occurred since the last read of WDT_SR.

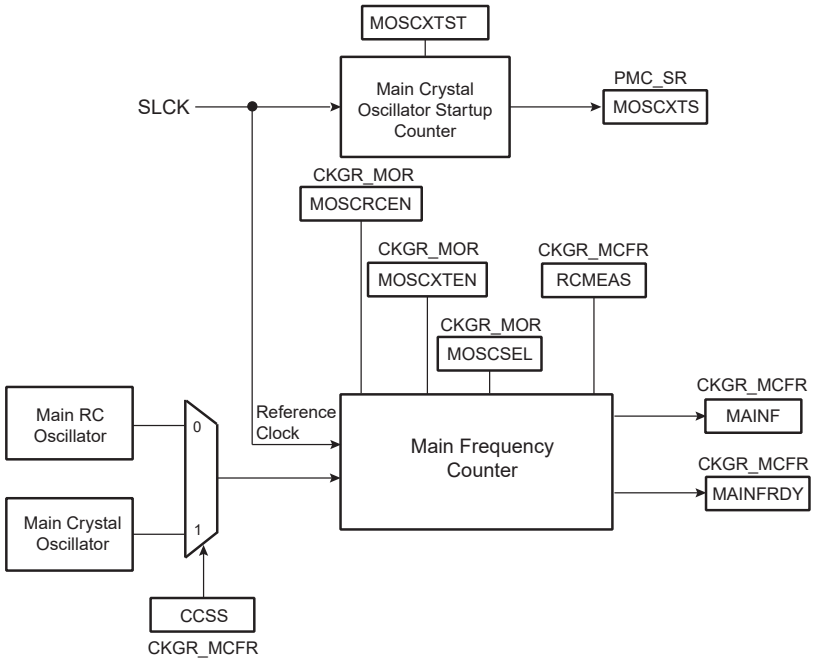
Bit 0 – WDUNF Watchdog Underflow (cleared on read)

Value	Description
0	No watchdog underflow occurred since the last read of WDT_SR.
1	At least one watchdog underflow occurred since the last read of WDT_SR.

1. Enable the Main crystal oscillator by setting CKGR_MOR.MOSCXTEN. Configure the CKGR_MOR. MOSCXTST field with the Main crystal oscillator startup time as defined in the section “Electrical Characteristics”.
2. Wait for PMC_SR.MOSCXTS flag to rise, indicating the end of a startup period of the Main crystal oscillator.
3. Select the Main crystal oscillator as the source clock of the Main frequency counter by setting CKGR_MCFR.CCSS.
4. Initiate a frequency measurement by setting CKGR_MCFR.RCMEAS.
5. Read CKGR_MCFR.MAINFRDY until its value equals 1.
6. Read CKGR_MCFR.MAINF and compute the value of the Main crystal frequency.

If the MAINF value is valid, software can switch MAINCK to the Main crystal oscillator. Refer to "Main Clock Source Selection".

Figure 30-3. Main Frequency Counter Block Diagram



30.6 PLLA Clock

The PLLA clock (PLLACK) is generated from MAINCK by the PLLA and a predivider. This combination allows a wide range of frequencies to be selected on either MCK, HCLK or the PCKx outputs.

The following figure shows the block diagram of the dividers and PLLA blocks.

Offset	Name	Bit Pos.								
0x01BC	XDMAC_CDS_MSP5	7:0	SDS_MSP[7:0]							
		15:8	SDS_MSP[15:8]							
		23:16	DDS_MSP[7:0]							
		31:24	DDS_MSP[15:8]							
0x01C0	XDMAC_CSUS5	7:0	SUBS[7:0]							
		15:8	SUBS[15:8]							
		23:16	SUBS[23:16]							
		31:24								
0x01C4	XDMAC_CDUS5	7:0	DUBS[7:0]							
		15:8	DUBS[15:8]							
		23:16	DUBS[23:16]							
		31:24								
0x01C8 ... 0x01CF	Reserved									
0x01D0	XDMAC_CIE6	7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
		15:8								
		23:16								
		31:24								
0x01D4	XDMAC_CID6	7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8								
		23:16								
		31:24								
0x01D8	XDMAC_CIM6	7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
		23:16								
		31:24								
0x01DC	XDMAC_CIS6	7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
		23:16								
		31:24								
0x01E0	XDMAC_CSA6	7:0	SA[7:0]							
		15:8	SA[15:8]							
		23:16	SA[23:16]							
		31:24	SA[31:24]							
0x01E4	XDMAC_CDA6	7:0	DA[7:0]							
		15:8	DA[15:8]							
		23:16	DA[23:16]							
		31:24	DA[31:24]							
0x01E8	XDMAC_CNDA6	7:0	NDA[5:0]							NDAIF
		15:8	NDA[13:6]							
		23:16	NDA[21:14]							
		31:24	NDA[29:22]							
0x01EC	XDMAC_CNDC6	7:0				NDVIEW[1:0]		NDDUP	NDSUP	NDE
		15:8								
		23:16								

38.8.2 GMAC Network Configuration Register

Name: GMAC_NCFGR
Offset: 0x004
Reset: 0x00080000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
		IRXER	RXBP	IPGSEN		IRXFCS	EFRHD	RXCOEN
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
	DCPF	DBW[1:0]		CLK[2:0]			RFCS	LFERD
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	0	0	0

Bit	15	14	13	12	11	10	9	8
	RXBUFO[1:0]		PEN	RTY				MAXFS
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit	7	6	5	4	3	2	1	0
	UNIHEN	MTIHEN	NBC	CAF	JFRAME	DNVLAN	FD	SPD
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 30 – IRXER Ignore IPG GRXER
When this bit is written to '1', the Receive Error signal (GRXER) has no effect on the GMAC operation when Receive Data Valid signal (GRXDV) is low.

Bit 29 – RXBP Receive Bad Preamble
When written to '1', frames with non-standard preamble are not rejected.

Bit 28 – IPGSEN IP Stretch Enable
Writing a '1' to this bit allows the transmit IPG to increase above 96 bit times, depending on the previous frame length using the IPG Stretch Register.

Bit 26 – IRXFCS Ignore RX FCS
For normal operation this bit must be written to zero.

When this bit is written to '1', frames with FCS/CRC errors will not be rejected. FCS error statistics will still be collected for frames with bad FCS, and FCS status will be recorded in the DMA descriptor of the frame.

Bit 25 – EFRHD Enable Frames Received in half-duplex
Writing a '1' to this bit enables frames to be received in half-duplex mode while transmitting.

38.8.4 GMAC User Register

Name: GMAC_UR
Offset: 0x00C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								R/W
Reset								0

Bit 0 – Reduced MII Mode

Value	Description
0	RMII mode is selected
1	MII mode is selected

38.8.67 GMAC 256 to 511 Byte Frames Received Register

Name: GMAC_TBFR511
Offset: 0x174
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 256 to 511 Byte Frames Received without Error
This bit fields counts the number of 256 to 511 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

39.6.22 Device Endpoint Interrupt Mask Register (Isochronous Endpoints)

Name: USBHS_DEVEPTIMRx (ISOENPT)
Offset: 0x01C0 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if EPTYPE = 0x1 in "Device Endpoint x Configuration Register".

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						RSTDT		EPDISHDMA
Access								
Reset						0		0

Bit	15	14	13	12	11	10	9	8
		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
Access								
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
Access								
Reset	0	0	0	0	0	0	0	0

Bit 18 – RSTDT Reset Data Toggle
This bit is set when USBHS_DEVEPTIERx.RSTDTS = 1. This clears the data toggle sequence, i.e., sets to Data0 the data toggle sequence of the next sent (IN endpoints) or received (OUT endpoints) packet.

This bit is cleared instantaneously.

The user does not have to wait for this bit to be cleared.

Bit 16 – EPDISHDMA Endpoint Interrupts Disable HDMA Request
This bit is set when USBHS_DEVEPTIERx.EPDISHDMAS = 1. This pauses the on-going DMA channel x transfer on any Endpoint x interrupt (PEP_x), whatever the state of the Endpoint x Interrupt Enable bit (PEP_x).

The user then has to acknowledge or to disable the interrupt source (e.g. USBHS_DEVEPTISRx.RXOUTI) or to clear the EPDISHDMA bit (by writing a one to the USBHS_DEVEPTIDRx.EPDISHDMAC bit) in order to complete the DMA transfer.

In Ping-pong mode, if the interrupt is associated to a new system-bank packet (e.g. Bank1) and the current DMA transfer is running on the previous packet (Bank0), then the previous-packet DMA transfer completes normally, but the new-packet DMA transfer does not start (not requested).

39.6.40 Host Address 2 Register

Name: USBHS_HSTADDR2
Offset: 0x0428
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
		HSTADDRP7[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		HSTADDRP6[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		HSTADDRP5[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		HSTADDRP4[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bits 30:24 – HSTADDRP7[6:0] USB Host Address
This field contains the address of the Pipe7 of the USB device.

This field is cleared when a USB reset is requested.

Bits 22:16 – HSTADDRP6[6:0] USB Host Address
This field contains the address of the Pipe6 of the USB device.

This field is cleared when a USB reset is requested.

Bits 14:8 – HSTADDRP5[6:0] USB Host Address
This field contains the address of the Pipe5 of the USB device.

This field is cleared when a USB reset is requested.

Bits 6:0 – HSTADDRP4[6:0] USB Host Address
This field contains the address of the Pipe4 of the USB device.

This field is cleared when a USB reset is requested.

Offset	Name	Bit Pos.								
0x34	SSC_TSHR	7:0	TSDAT[7:0]							
		15:8	TSDAT[15:8]							
		23:16								
		31:24								
0x38	SSC_RC0R	7:0	CP0[7:0]							
		15:8	CP0[15:8]							
		23:16								
		31:24								
0x3C	SSC_RC1R	7:0	CP1[7:0]							
		15:8	CP1[15:8]							
		23:16								
		31:24								
0x40	SSC_SR	7:0			OVRUN	RXRDY			TXEMPTY	TXRDY
		15:8					RXSYN	TXSYN	CP1	CP0
		23:16							RXEN	TXEN
		31:24								
0x44	SSC_IER	7:0			OVRUN	RXRDY			TXEMPTY	TXRDY
		15:8					RXSYN	TXSYN	CP1	CP0
		23:16								
		31:24								
0x48	SSC_IDR	7:0			OVRUN	RXRDY			TXEMPTY	TXRDY
		15:8					RXSYN	TXSYN	CP1	CP0
		23:16								
		31:24								
0x4C	SSC_IMR	7:0			OVRUN	RXRDY			TXEMPTY	TXRDY
		15:8					RXSYN	TXSYN	CP1	CP0
		23:16								
		31:24								
0x50 ... 0xE3	Reserved									
0xE4	SSC_WPMR	7:0								WPEN
		15:8	WPKEY[7:0]							
		23:16	WPKEY[15:8]							
		31:24	WPKEY[23:16]							
0xE8	SSC_WPSR	7:0								WPVS
		15:8	WPVSRC[7:0]							
		23:16	WPVSRC[15:8]							
		31:24								

Bits 29:24 – IMCKFS[5:0] Master Clock to f_s Ratio
Master clock frequency is [2 x 16 × (IMCKFS + 1)] / (IMCKDIV + 1) times the sample rate, i.e., I2SC_WS frequency.

Value	Name	Description
0	M2SF32	Sample frequency ratio set to 32
1	M2SF64	Sample frequency ratio set to 64
2	M2SF96	Sample frequency ratio set to 96
3	M2SF128	Sample frequency ratio set to 128
5	M2SF192	Sample frequency ratio set to 192
7	M2SF256	Sample frequency ratio set to 256
11	M2SF384	Sample frequency ratio set to 384
15	M2SF512	Sample frequency ratio set to 512
23	M2SF768	Sample frequency ratio set to 768
31	M2SF1024	Sample frequency ratio set to 1024
47	M2SF1536	Sample frequency ratio set to 1536
63	M2SF2048	Sample frequency ratio set to 2048

Bits 21:16 – IMCKDIV[5:0] Selected Clock to I2SC Master Clock Ratio
I2SC_MCK Master clock output frequency is Selected Clock divided by (IMCKDIV + 1). Refer to the IMCKFS field description.

Note:

1. This field is write-only. Always read as ‘0’.
2. Do not write a ‘0’ to this field.

Bit 14 – TXSAME Transmit Data when Underrun

Value	Description
0	Zero sample transmitted when underrun.
1	Previous sample transmitted when underrun

Bit 13 – TXDMA Single or Multiple DMA Controller Channels for TransmitterDMA Controller Channels for Transmitter

Value	Description
0	The transmitter uses only one DMA Controller channel for all audio channels.
1	The transmitter uses one DMA Controller channel per audio channel.

Bit 12 – TXMONO Transmit Mono

Value	Description
0	Stereo
1	Mono, with left audio samples duplicated to right audio channel by the I2SC.

Bit 10 – RXLOOP Loopback Test Mode

Value	Description
0	Normal mode
1	I2SC_DO output of I2SC is internally connected to I2SC_DI input.

Note: All reserved Channel Descriptor bits must be written to ‘0’ by software when initialized.

Synchronous Channel Operation

The MLB provides two modes of operation (Standard and Multi-Frame per Sub- buffer) to provide flexibility for implementing synchronous channels.

Channels set up for Standard mode require less buffer space, but have higher interrupt rates and more stringent latency requirements. For channels configured for Standard mode, the Host Controller must transfer one full frame of streaming data in/out of each streaming channel's data buffer for each frame period.

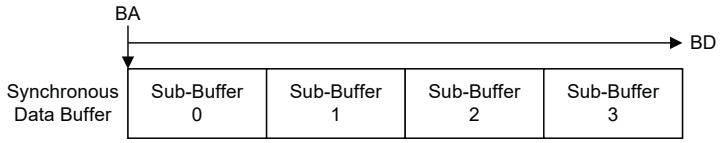
Channels set up for Multi-Frame per Sub-buffer mode require more buffer space, but have lower interrupt rates and less stringent latency requirements. For channels configured for Multi-Frame per Sub-buffer mode, the Host Controller must transfer N full frames of streaming data in/out of each streaming channel's data buffer for each frame period.

To set up a channel in Multi-Frame per Sub-buffer mode:

- Program MLB_MLBC0.FCNT[2:0] to select the number of frames per sub-buffer
- Program the CAT to enable multi-frame sub-buffering (MFE = 1) for each particular channel
- Set the buffer depth in the CDT: BD = 4 × m × bpf - 1,
  where m = frames per sub- buffer, bpf = bytes per frame
- Repeat for additional synchronous channels

A sample synchronous data buffer is shown in the following figure. Each data buffer contains four sub-buffers and each sub-buffer contains space for 1 to 64 frames of data, determined by MLB_MLBC0.FCNT[2:0].

Figure 48-17. Synchronous Data Buffer Structure



Synchronous Channel Descriptors

The format and field definitions for a synchronous CDT entry are shown in Table 48-14 and Table 48-14, respectively.

Table 48-14. Synchronous CDT Entry Format

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WSBC		Reserved													
16	RSBC		Reserved													
32	Reserved															
48	Reserved															
64	WSTS[3:0]				WPTR[11:0]											
80	RSTS[3:0]				RPTR[11:0]											
96	Reserved				BD[11:0]											
112	Reserved		BA[13:0]													

Bits 20:16 – DBRP[4:0] Data Bit Rate Prescaler
The value by which the peripheral clock is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

Bits 12:8 – DTSEG1[4:0] Data Time Segment Before Sample Point
0: Forbidden.

1 to 31: The duration of time segment is t_q x (DTSEG1 + 1).

Bits 7:4 – DTSEG2[3:0] Data Time Segment After Sample Point
The duration of time segment is t_q x (DTSEG2 + 1).

Bits 2:0 – DSJW[2:0] Data (Re) Synchronization Jump Width
The duration of a synchronization jump is t_q x (DSJW + 1).

49.6.38 MCAN Transmit Buffer Request Pending

Name: MCAN_TXBRP
Offset: 0xCC
Reset: 0x00000000
Property: Read-only

MCAN_TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding MCAN_TXBRP bit is reset.

Bit	31	30	29	28	27	26	25	24
	TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – TRPx Transmission Request Pending for Buffer x
Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register MCAN_TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register MCAN_TXBCR.

TXBRP bits are set only for those Tx Buffers configured via MCAN_TXBC. After a MCAN_TXBRP bit has been set, a Tx scan (see Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID).

A cancellation request resets the corresponding transmission request pending bit of register MCAN_TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset.

After a cancellation has been requested, a finished cancellation is signalled via MCAN_TXBCF.

- after successful transmission together with the corresponding MCAN_TXBTO bit.
- when the transmission has not yet been started at the point of cancellation.

Figure 50-10. WAVSEL = 10 without Trigger

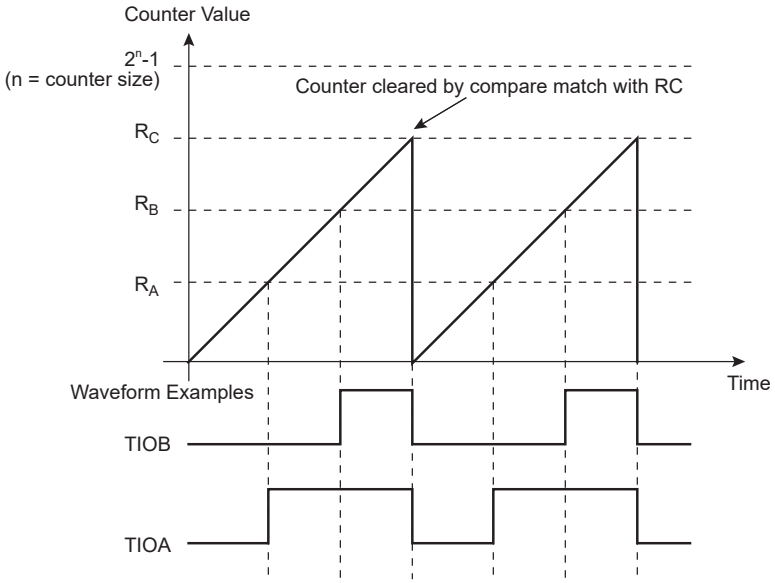
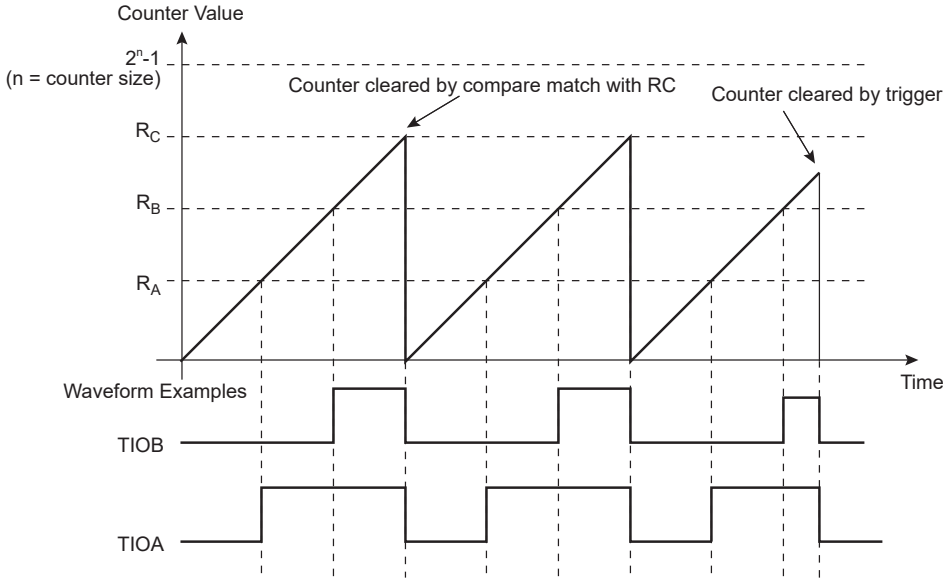


Figure 50-11. WAVSEL = 10 with Trigger



50.6.12.3 WAVSEL = 01

When WAVSEL = 01, the value of TC_CV is incremented from 0 to 2^{16}-1 . Once 2^{16}-1 is reached, the value of TC_CV is decremented to 0, then reincremented to 2^{16}-1 and so on.

A trigger such as an external event or a software trigger can modify TC_CV at any time. If a trigger occurs while TC_CV is incrementing, TC_CV then decrements. If a trigger is received while TC_CV is decrementing, TC_CV then increments.

Refer to the figures below.

RC Compare cannot be programmed to generate a trigger in this configuration.

At the same time, RC Compare can stop the counter clock (CPCSTOP = 1) and/or disable the counter clock (CPCDIS = 1).

Value	Name	Description
0	DISABLED	One data to convert is written to the FIFO per access to DACC.
1	ENABLED	Two data to convert are written to the FIFO per access to DACC (reduces the number of requests to DMA and the number of system bus accesses).

Bits 0, 1 – MAXSx Max Speed Mode for Channel x

Value	Name	Description
0	TRIG_EVENT	Trigger mode or Free-running mode enabled. (See TRGENx.DACC_TRIGR.)
1	MAXIMUM	Max speed mode enabled.

Symbol	Parameter	Digital Code	Min	Typ	Max	Unit
		1110	–	3.28	–	
		1111	–	3.4	–	

Figure 58-3. VDDIO Supply Monitor

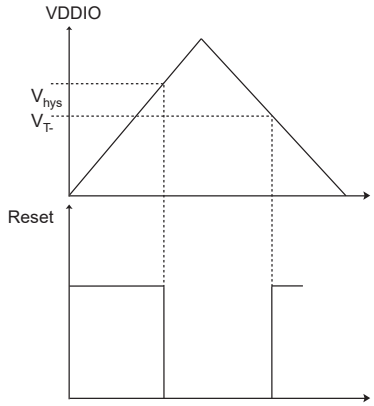
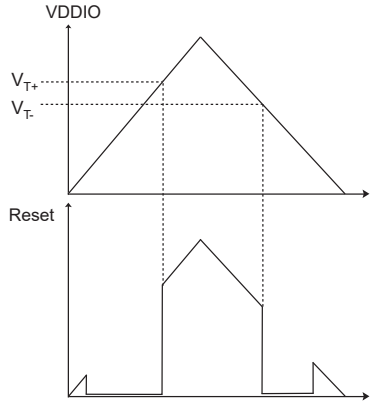


Table 58-10. VDDIO Power-On Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T+}	Threshold Voltage Rising	–	1.45	1.53	1.61	V
V_{T-}	Threshold Voltage Falling	–	1.37	1.46	–	V
V_{hys}	Hysteresis	–	40	80	130	mV
t_{RES}	Reset Time-out Period	–	240	320	800	µs

Figure 58-4. VDDIO Power-On Reset Characteristics



58.3 Power Consumption

- Power consumption of the device depending on the different Low-Power modes (Backup, Wait, Sleep) and Active mode
- Power consumption on power supply in different modes: Backup, Wait, Sleep and Active
- Power consumption by peripheral:

shown further below, the device sampling point extends the propagation delay (t_p) for slave and routing delays to more than half the SPI clock period, whereas the common sampling point allows only less than half the SPI clock period.

As an example, an SPI Slave working in Mode 0 can be safely driven if the SPI Master is configured in Mode 0.

Figure 58-19. MISO Capture in Master Mode

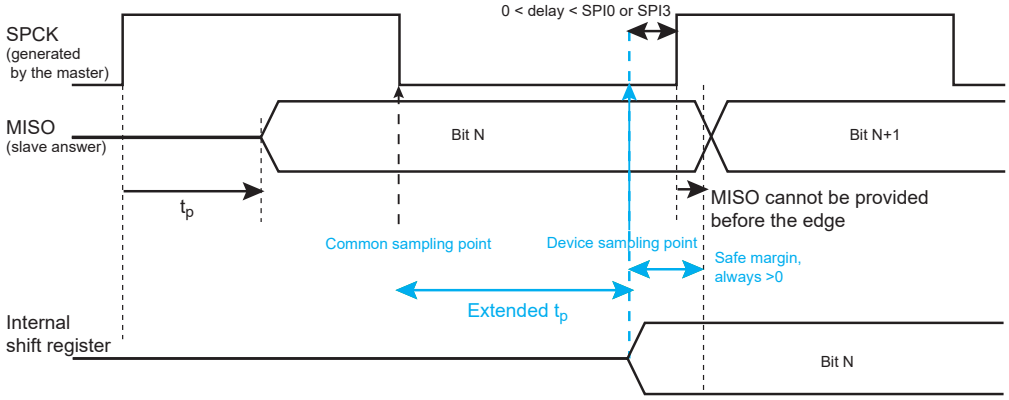


Figure 58-20. SPI Master Mode with (CPOL= NCPHA = 0) or (CPOL= NCPHA= 1)

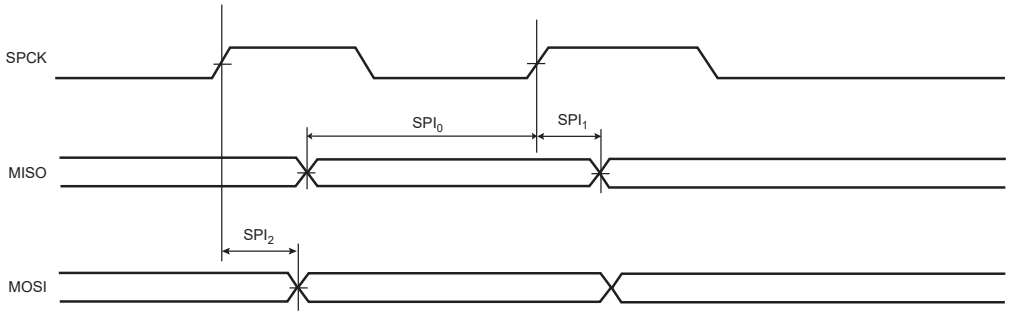
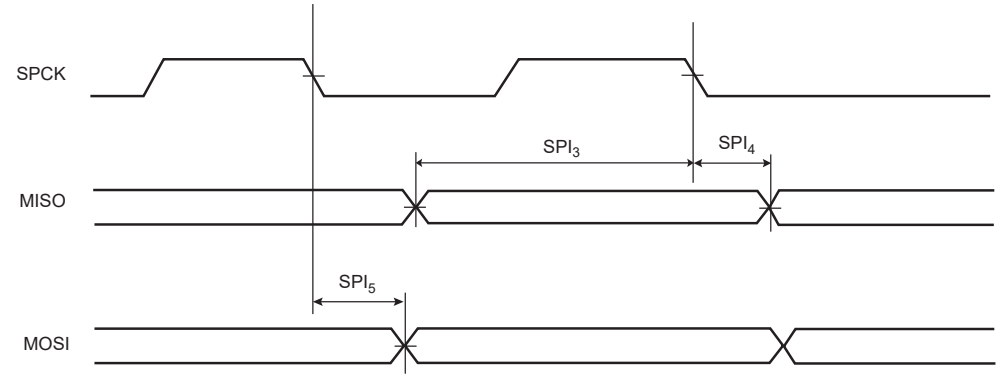
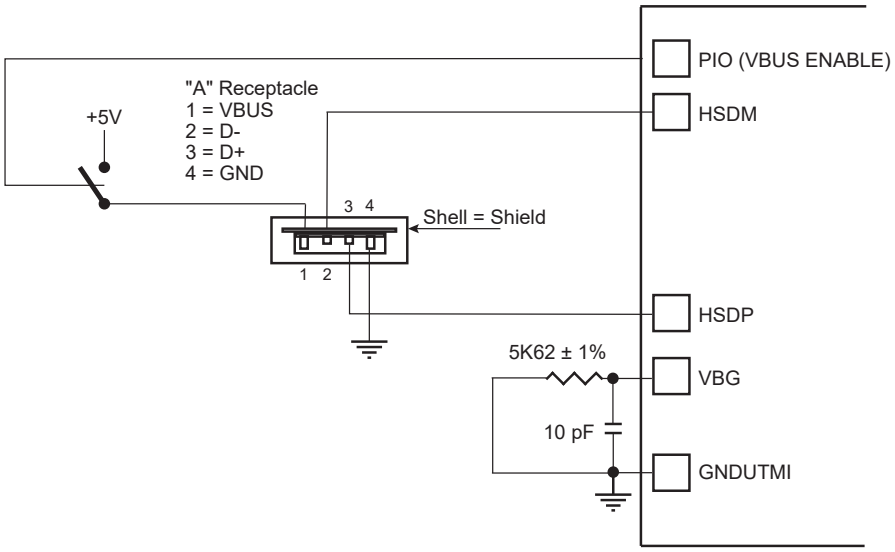


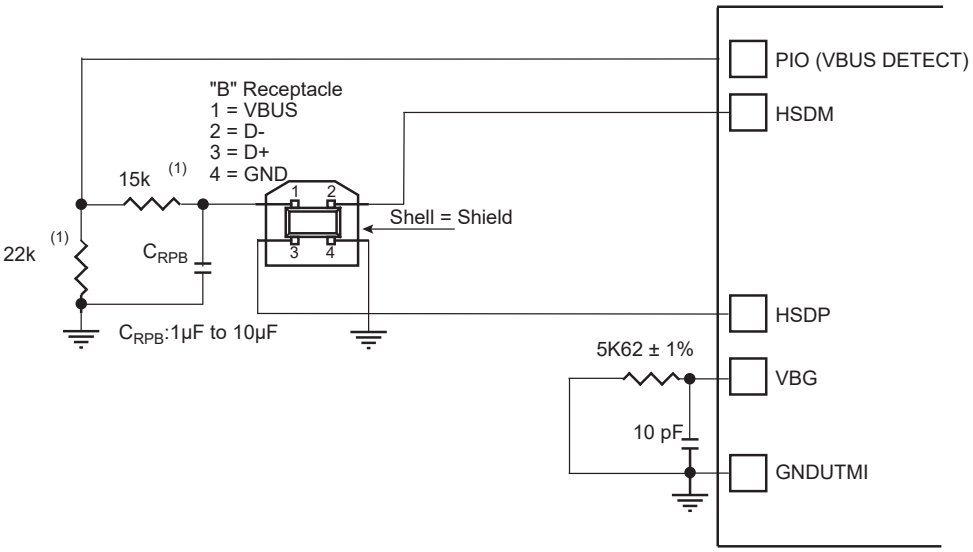
Figure 58-21. SPI Master Mode with (CPOL = 0 and NCPHA=1) or (CPOL=1 and NCPHA= 0)



1. The following schematic shows an example of USB High Speed host connection. For more information, refer to 39. USB High-Speed Interface (USBHS)



2. The following schematic shows a typical USB High Speed device connection: For more information, refer to 39. USB High-Speed Interface (USBHS).



Note: The values shown on the 22 kΩ and 15 kΩ resistors are only valid with 3.3V supplied PIOs.

60.2.9 Memory Controllers

Signal Name	Recommended Pin Connection	Description
External Bus Interface		
D[15:0]	Application dependent.	Data Bus (D0 to D15) All data lines are pullup inputs to VDDIO at reset.
A[23:0]	Application dependent.	Address Bus (A0 to A23) All address lines pullup inputs to VDDIO at reset.

Date	Comments
	Section 46.6.3.11 “Receiver Timeout”: deleted redundant paragraphs on STTTO and RETTO. Section 46.6.4 “ISO7816 Mode”: corrected USART_MODE value for prototcol T = 1. Section 46.6.10 “LON Mode”: added information on node-to-node communication. Section 46.7.3 “USART Mode Register”: updated USART_MODE description to include LIN mode support.
cont’d	
01-June-16	Section 49. “Controller Area Network (MCAN)” Throughout: Renamed Fast Bit TIming and Prescaler Register to Data Bit TIming and Prescaler Register (MCAN_DBTP). Renamed field FBRP to DBRP and updated description. Updated descriptions of DSJW, DTSEG2 and DTSEG1. Added Section 49.4.5 “Timestamping”. Changed ‘Baud’ to ‘Bit’ in: - Section 49.5.3 “Timeout Counter”: in ‘Note’. - Section 49.6.4 “MCAN Data Bit Timing and Prescaler Register”: DBRP field description. - Section 49.6.8 “MCAN Nominal Bit Timing and Prescaler Register” NBRP field description. Updated Section 49.5.1.3 “CAN FD Operation”. Renamed section Transceiver Delay Compensation to Transmitter Delay Compensation (Section 49.5.1.4). Changed NTSEG1 to TSEG1. Updated content. Section 49.5.1.5 “Restricted Operation Mode”: added ‘Note’. Updated Figure 49-5 “Standard Message ID Filter Path” and Figure 49-6 “Extended Message ID Filter Path”. Section 49.6.7 “MCAN CC Control Register”: added bit NISO. Updated descriptions of FDOE, BRSE, PXHD and EFBI. Section 49.6.9 “MCAN Timestamp Counter Configuration Register”: updated TSS description. Section 49.6.10 “MCAN Timestamp Counter Value Register”: updated TSC description. Section 49.6.20 “MCAN Global Filter Configuration”: added some details on register description. Updated ANFE and ANFS field descriptions. Section 49.6.21 “MCAN Standard ID Filter Configuration” and Section 49.6.22 “MCAN Extended ID Filter Configuration”: added some details on register description. Section 49.6.24 “MCAN High Priority Message Status”: updated MSI description for value ‘1’.
	Section 50. “Timer Counter (TC)” Throughout: Replaced TIOA, TIOB, TCLK with TIOAx, TIOBx, TCLKx. Reformatted and renamed Table 50-2 “Channel Signal Description”.