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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70n21b-cn

35.16.1.3 SMC Cycle Register

Name: SMC_CYCLE[0..3]
Offset: 0x00
Reset: 0
Property: R/W

This register can only be written if the WPEN bit is cleared in the “SMC Write Protection Mode Register” .

Bit	31	30	29	28	27	26	25	24
								NRD_CYCLE[8:8]
Access								
Reset								0

Bit	23	22	21	20	19	18	17	16
	NRD_CYCLE[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
								NWE_CYCLE[8:8]
Access								
Reset								0

Bit	7	6	5	4	3	2	1	0
	NWE_CYCLE[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 24:16 – NRD_CYCLE[8:0] Total Read Cycle Length
The total read cycle length is the total duration in clock cycles of the read cycle. It is equal to the sum of the setup, pulse and hold steps of the NRD and NCS signals. It is defined as:

Read cycle length = (NRD_CYCLE[8:7]*256 + NRD_CYCLE[6:0]) clock cycles

Bits 8:0 – NWE_CYCLE[8:0] Total Write Cycle Length
The total write cycle length is the total duration in clock cycles of the write cycle. It is equal to the sum of the setup, pulse and hold steps of the NWE and NCS signals. It is defined as:

Write cycle length = (NWE_CYCLE[8:7]*256 + NWE_CYCLE[6:0]) clock cycles

Frame Segment	Value
Type (Octets 12–13)	86dd
IP stuff (Octets 14–19)	—
UDP (Octet 20)	11
IP stuff (Octets 21–37)	—
IP DA (Octets 38–53)	FF0X00000000018
Source IP port (Octets 54–55)	—
Dest IP port (Octets 56–57)	013F
Other stuff (Octets 58–61)	—
Message type (Octet 62)	00
Other stuff (Octets 63–93)	—
Version PTP (Octet 94)	02

Table 38-11. Example of Pdelay_Resp Frame in 1588 Version 2 (UDP/IPv6) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	86dd
IP stuff (Octets 14–19)	—
UDP (Octet 20)	11
IP stuff (Octets 21–37)	—
IP DA (Octets 38–53)	FF0200000000006B
Source IP port (Octets 54–55)	—
Dest IP port (Octets 56–57)	013F
Other stuff (Octets 58–61)	—
Message type (Octet 62)	03
Other stuff (Octets 63–93)	—
Version PTP (Octet 94)	02

For the multicast address 011B19000000 sync and delay request frames are recognized depending on the message type field, 00 for sync and 01 for delay request.

Broadcast Frames Transmitted Register	64 Byte Frames Received Register
Multicast Frames Transmitted Register	65 to 127 Byte Frames Received Register
Pause Frames Transmitted Register	128 to 255 Byte Frames Received Register
64 Byte Frames Transmitted Register	256 to 511 Byte Frames Received Register
65 to 127 Byte Frames Transmitted Register	512 to 1023 Byte Frames Received Register
128 to 255 Byte Frames Transmitted Register	1024 to 1518 Byte Frames Received Register
256 to 511 Byte Frames Transmitted Register	1519 to Maximum Byte Frames Received Register
512 to 1023 Byte Frames Transmitted Register	Undersize Frames Received Register
1024 to 1518 Byte Frames Transmitted Register	Oversize Frames Received Register
Greater Than 1518 Byte Frames Transmitted Register	Jabbers Received Register
Transmit Underruns Register	Frame Check Sequence Errors Register
Single Collision Frames Register	Length Field Frame Errors Register
Multiple Collision Frames Register	Receive Symbol Errors Register
Excessive Collisions Register	Alignment Errors Register
Late Collisions Register	Receive Resource Errors Register
Deferred Transmission Frames Register	Receive Overrun Register
Carrier Sense Errors Register	IP Header Checksum Errors Register
Octets Received Low Register	TCP Checksum Errors Register
Octets Received High Register	UDP Checksum Errors Register
Frames Received Register	

These registers reset to zero on a read and stick at all ones when they count to their maximum value. They should be read frequently enough to prevent loss of data.

The receive statistics registers are only incremented when the receive enable bit (RXEN) is set in the Network Control register.

Once a statistics register has been read, it is automatically cleared. When reading the Octets Transmitted and Octets Received registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

Offset	Name	Bit Pos.								
0x0150	GMAC_ORLO	7:0	RXO[7:0]							
		15:8	RXO[15:8]							
		23:16	RXO[23:16]							
		31:24	RXO[31:24]							
0x0154	GMAC_ORHI	7:0	RXO[7:0]							
		15:8	RXO[15:8]							
		23:16								
		31:24								
0x0158	GMAC_FR	7:0	FRX[7:0]							
		15:8	FRX[15:8]							
		23:16	FRX[23:16]							
		31:24	FRX[31:24]							
0x015C	GMAC_BCFR	7:0	BFRX[7:0]							
		15:8	BFRX[15:8]							
		23:16	BFRX[23:16]							
		31:24	BFRX[31:24]							
0x0160	GMAC_MFR	7:0	MFRX[7:0]							
		15:8	MFRX[15:8]							
		23:16	MFRX[23:16]							
		31:24	MFRX[31:24]							
0x0164	GMAC_PFR	7:0	PFRX[7:0]							
		15:8	PFRX[15:8]							
		23:16								
		31:24								
0x0168	GMAC_BFR64	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x016C	GMAC_TBFR127	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x0170	GMAC_TBFR255	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x0174	GMAC_TBFR511	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x0178	GMAC_TBFR1023	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x017C	GMAC_TBFR1518	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							

38.8.42 GMAC Multicast Frames Transmitted Register

Name: GMAC_MFT
Offset: 0x110
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	MFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MFTX[31:0] Multicast Frames Transmitted without Error
This register counts the number of multicast frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

Value	Description
0	USBHS_HSTDMASTATUSx.DESC_LDST rising does not trigger any interrupt.
1	An interrupt is generated when a descriptor has been loaded from the bus.

Bit 5 – END_BUFFIT End of Buffer Interrupt Enable

Value	Description
0	USBHS_HSTDMASTATUSx.END_BF_ST rising does not trigger any interrupt.
1	An interrupt is generated when USBHS_HSTDMASTATUSx.BUFF_COUNT reaches zero.

Bit 4 – END_TR_IT End of Transfer Interrupt Enable
Use when the receive size is unknown.

Value	Description
0	Completion of a USBHS device-initiated buffer transfer does not trigger any interrupt at USBHS_HSTDMASTATUSx.END_TR_ST rising.
1	An interrupt is sent after the buffer transfer is complete, if the USBHS device has ended the buffer transfer.

Bit 3 – END_B_EN End of Buffer Enable Control
This is mainly for short packet OUT validations initiated by the DMA reaching the end of buffer, but could be used for IN packet truncation (discarding of unwanted packet data) at the end of DMA buffer.

Value	Description
0	DMA Buffer End has no impact on USB packet transfer.
1	The pipe can validate the packet (according to the values programmed in the USBHS_HSTPIPCFGx.AUTOSW and USBHS_HSTPIPIMRx.SHORTPACKETIE fields) at DMA Buffer End, i.e., when USBHS_HSTDMASTATUS.BUFF_COUNT reaches 0.

Bit 2 – END_TR_EN End of Transfer Enable Control (OUT transfers only)
When set, a BULK or INTERRUPT short packet closes the current buffer and the USBHS_HSTDMASTATUSx.END_TR_ST flag is raised.

This is intended for a USBHS non-prenegotiated USB transfer size.

Value	Description
0	USB end of transfer is ignored.
1	The USBHS device can put an end to the current buffer transfer.

Bit 1 – LDNXT_DSC Load Next Channel Transfer Descriptor Enable Command
If the CHANN_ENB bit is cleared, the next descriptor is loaded immediately upon transfer request.

DMA Channel Control Command Summary:

Value LDNXT_DSC	Value CHANN_ENB	Name	Description
0	0	STOP_NOW	Stop now
0	1	RUN_AND_STOP	Run and stop at end of buffer
1	0	LOAD_NEXT_DESC	Load next descriptor now
1	1	RUN_AND_LINK	Run and link at end of buffer

5. Issue the Boot Operation Request command by writing to the HSMCI_CMDR with SPCND set to BOOTREQ, TRDIR set to READ and TRCMD set to “start data transfer”.
6. DMA controller copies the boot partition to the memory.
7. When DMA transfer is completed, host processor shall terminate the boot stream by writing the HSMCI_CMDR with SPCMD field set to BOOTEND.

40.12 HSMCI Transfer Done Timings

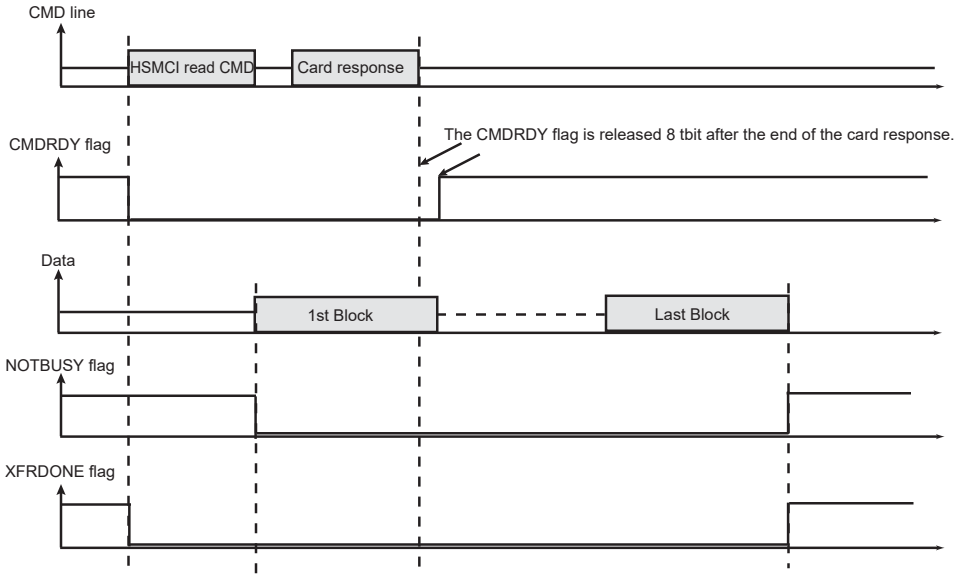
40.12.1 Definition

The XFRDONE flag in the HSMCI_SR indicates exactly when the read or write sequence is finished.

40.12.2 Read Access

During a read access, the XFRDONE flag behaves as shown in the following figure.

Figure 40-11. XFRDONE During a Read Access



40.12.3 Write Access

During a write access, the XFRDONE flag behaves as shown in the following figure.

Bit 1 – SPIDIS SPI Disable
All pins are set in Input mode after completion of the transmission in progress, if any.

If a transfer is in progress when SPIDIS is set, the SPI completes the transmission of the shifter register and does not start any new transfer, even if SPI_THR is loaded.

If both SPIEN and SPIDIS are equal to one when SPI_CR is written, the SPI is disabled.

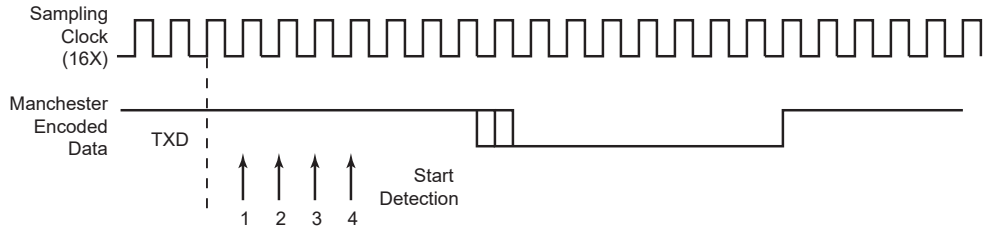
Value	Description
0	No effect.
1	Disables the SPI.

Bit 0 – SPIEN SPI Enable

Value	Description
0	No effect.
1	Enables the SPI to transfer and receive data.

The US_MAN.RXIDLEV informs the USART of the receiver line idle state value (receiver line inactive). The user must define RXIDLEV to ensure reliable synchronization. By default, RXIDLEV is set to ‘1’ (receiver line is at level 1 when there is no activity).

Figure 46-13. Asynchronous Start Bit Detection



The receiver is activated and starts preamble and frame delimiter detection, sampling the data at one quarter and then three quarters. If a valid preamble pattern or start frame delimiter is detected, the receiver continues decoding with the same synchronization. If the stream does not match a valid pattern or a valid start frame delimiter, the receiver resynchronizes on the next valid edge.The minimum time threshold to estimate the bit value is three quarters of a bit time.

If a valid preamble (if used) followed with a valid start frame delimiter is detected, the incoming stream is decoded into NRZ data and passed to the USART for processing. Figure 46-14 illustrates Manchester pattern mismatch. When incoming data stream is passed to the USART, the receiver is also able to detect Manchester code violation. A code violation is a lack of transition in the middle of a bit cell. In this case, the US_CSR.MANERR flag is raised. It is cleared by writing a ‘1’ to US_CR.RSTSTA. See Figure 46-15 for an example of Manchester error detection during data phase.

Figure 46-14. Preamble Pattern Mismatch

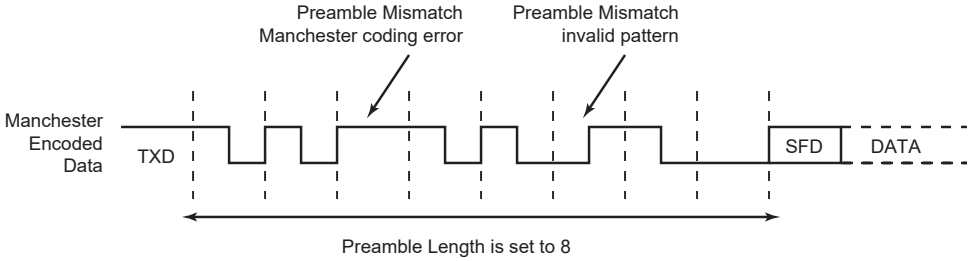
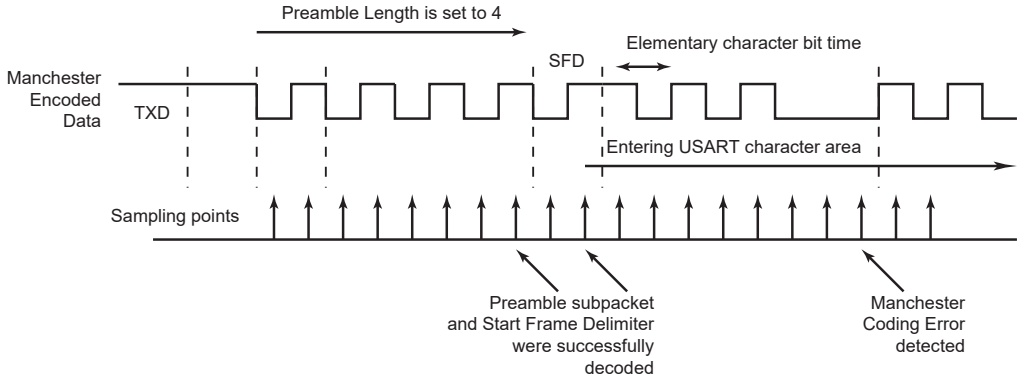


Figure 46-15. Manchester Error Flag



When the start frame delimiter is a sync pattern (US_MR.ONEBIT = 0), both command and data delimiter are supported. If a valid sync is detected, the received character is written in RXCHR in the Receive Holding register (US_RHR) and RXSYNH is updated. RXSYNH is set to ‘1’ when the received character is a command, and to ‘0’ if the received character is a data. This alleviates and simplifies the direct memory access as the character contains its own sync field in the same register.

Value	Description
0	The USART does not filter the receive line.
1	The USART filters the receive line using a three-sample filter (1/16-bit clock) (2 over 3 majority).

Bits 26:24 – MAX_ITERATION[2:0] Maximum Number of Automatic Iteration

Value	Description
0-7	Defines the maximum number of iterations in ISO7816 mode, protocol T = 0.

Bit 23 – INVDATA Inverted Data

Value	Description
0	The data field transmitted on TXD line is the same as the one written in US_THR or the content read in US_RHR is the same as RXD line. Normal mode of operation.
1	The data field transmitted on TXD line is inverted (voltage polarity only) compared to the value written on US_THR or the content read in US_RHR is inverted compared to what is received on RXD line (or ISO7816 IO line). Inverted mode of operation, useful for contactless card application. To be used with configuration bit MSBF.

Bit 22 – VAR_SYNC Variable Synchronization of Command/Data Sync Start Frame Delimiter

Value	Description
0	User defined configuration of command or data sync field depending on MODSYNC value.
1	The sync field is updated when a character is written into US_THR.

Bit 21 – DSNACK Disable Successive NACK

Value	Description
0	NACK is sent on the ISO line as soon as a parity error occurs in the received character (unless INACK is set).
1	Successive parity errors are counted up to the value specified in the MAX_ITERATION field. These parity errors generate a NACK on the ISO line. As soon as this value is reached, no additional NACK is sent on the ISO line. The flag ITER is asserted. Note: MAX_ITERATION field must be set to 0 if DSNACK is cleared.

Bit 20 – INACK Inhibit Non Acknowledge

Value	Description
0	The NACK is generated.
1	The NACK is not generated.

Bit 19 – OVER Oversampling Mode

Value	Description
0	16X Oversampling
1	8X Oversampling

Bit 18 – CLKO Clock Output Select

Bit 21 – DSR Image of DSR Input

Value	Description
0	DSR input is driven low.
1	DSR input is driven high.

Bit 20 – RI Image of RI Input

Value	Description
0	RI input is driven low.
1	RI input is driven high.

Bit 19 – CTSIC Clear to Send Input Change Flag (cleared on read)

Value	Description
0	No input change has been detected on the CTS pin since the last read of US_CSR.
1	At least one input change has been detected on the CTS pin since the last read of US_CSR.

Bit 18 – DCDIC Data Carrier Detect Input Change Flag (cleared on read)

Value	Description
0	No input change has been detected on the DCD pin since the last read of US_CSR.
1	At least one input change has been detected on the DCD pin since the last read of US_CSR.

Bit 17 – DSRIC Data Set Ready Input Change Flag (cleared on read)

Value	Description
0	No input change has been detected on the DSR pin since the last read of US_CSR.
1	At least one input change has been detected on the DSR pin since the last read of US_CSR.

Bit 16 – RIIC Ring Indicator Input Change Flag (cleared on read)

Value	Description
0	No input change has been detected on the RI pin since the last read of US_CSR.
1	At least one input change has been detected on the RI pin since the last read of US_CSR.

Bit 13 – NACK Non Acknowledge Interrupt (cleared by writing a one to bit US_CR.RSTNACK)

Value	Description
0	Non acknowledge has not been detected since the last RSTNACK.
1	At least one non acknowledge has been detected since the last RSTNACK.

Bit 10 – ITER Max Number of Repetitions Reached (cleared by writing a one to bit US_CR.RSTIT)

Value	Description
0	Maximum number of repetitions has not been reached since the last RSTIT.
1	Maximum number of repetitions has been reached since the last RSTIT.

Bit 9 – TXEMPTY Transmitter Empty (cleared by writing US_THR)

49.6.34 MCAN Receive Buffer / FIFO Element Size Configuration

Name: MCAN_RXESC
Offset: 0xBC
Reset: 0x00000000
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Configures the number of data bytes belonging to a Receive Buffer / Receive FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Receive Buffer or Receive FIFO, only the number of bytes as configured by MCAN_RXESC are stored to the Receive Buffer resp. Receive FIFO element. The rest of the frame's data field is ignored.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access						RBDS[2:0]		
Reset						R/W	R/W	R/W
						0	0	0

Bit	7	6	5	4	3	2	1	0
Access		F1DS[2:0]				F0DS[2:0]		
Reset		R/W	R/W	R/W		R/W	R/W	R/W
		0	0	0		0	0	0

Bits 10:8 – RBDS[2:0] Receive Buffer Data Field Size

Value	Name	Description
0	8_BYTE	8-byte data field
1	12_BYTE	12-byte data field
2	16_BYTE	16-byte data field
3	20_BYTE	20-byte data field
4	24_BYTE	24-byte data field
5	32_BYTE	32-byte data field
6	48_BYTE	48-byte data field
7	64_BYTE	64-byte data field

Bits 6:4 – F1DS[2:0] Receive FIFO 1 Data Field Size

50. Timer Counter (TC)

50.1 Description

A Timer Counter (TC) module includes three identical TC channels. The number of implemented TC modules is device-specific.

Each TC channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each channel has three external clock inputs, five internal clock inputs and two multipurpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts.

The TC embeds a quadrature decoder (QDEC) connected in front of the timers and driven by TIOA0, TIOB0 and TIOB1 inputs. When enabled, the QDEC performs the input lines filtering, decoding of quadrature signals and connects to the timers/counters in order to read the position and speed of the motor through the user interface.

The TC block has two global registers which act upon all TC channels:

- Block Control register (TC_BCR)—allows channels to be started simultaneously with the same instruction
- Block Mode register (TC_BMR)—defines the external clock inputs for each channel, allowing them to be chained

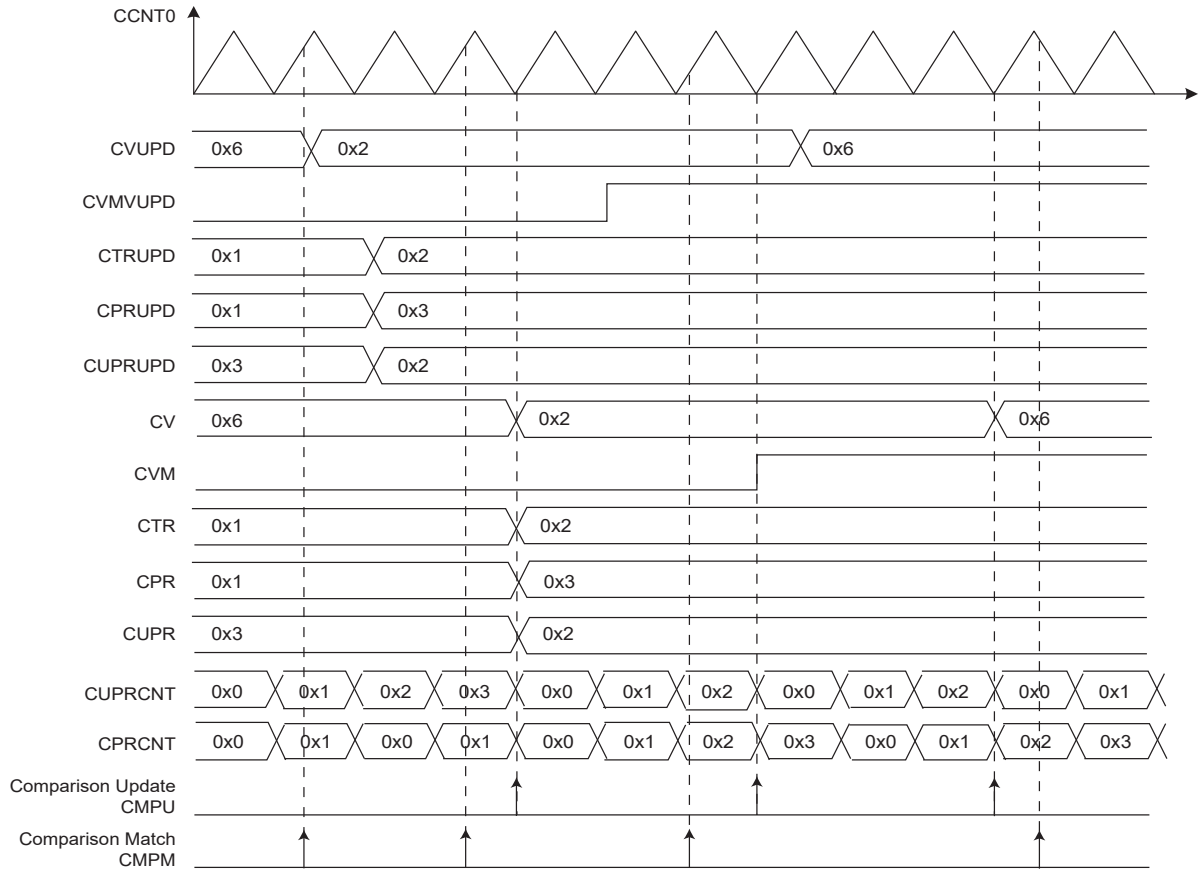
50.2 Embedded Characteristics

- Total of 12 Channels
- 16-bit Channel Size
- Wide Range of Functions Including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
  - Quadrature decoder
  - 2-bit Gray up/down count for stepper motor
- Each Channel is User-Configurable and Contains:
  - Three external clock inputs
  - Five Internal clock inputs
  - Two multipurpose input/output signals acting as trigger event
  - Trigger/capture events can be directly synchronized by PWM signals
- Internal Interrupt Signal

⚠ CAUTION The write of PWM_CMPVUPDx must be followed by a write of PWM_CMPMUPDx.

The comparison match and the comparison update can be source of an interrupt, but only if it is enabled and not masked. These interrupts can be enabled by the PWM Interrupt Enable Register 2 and disabled by the PWM Interrupt Disable Register 2. The comparison match interrupt and the comparison update interrupt are reset by reading the PWM Interrupt Status Register 2.

Figure 51-24. Comparison Waveform



51.6.4 PWM Event Lines

The PWM provides 2 independent event lines intended to trigger actions in other peripherals (e.g., for the Analog-to-Digital Converter (ADC)).

A pulse (one cycle of the peripheral clock) is generated on an event line, when at least one of the selected comparisons is matching. The comparisons can be selected or unselected independently by the CSEL bits in the PWM Event Line x Register (PWM_ELMRx for the Event Line x).

An example of event generation is provided in the figure Event Line Generation Waveform (Example).

Value	Name	Description
0	CLKB_POFF	CLKB clock is turned off
1	PREB	CLKB clock is clock selected by PREB
2-255	PREB_DIV	CLKB clock is clock selected by PREB divided by DIVB factor

Bits 11:8 – PREA[3:0] CLKA Source Clock Selection

Value	Name	Description
0	CLK	Peripheral clock
1	CLK_DIV2	Peripheral clock/2
2	CLK_DIV4	Peripheral clock/4
3	CLK_DIV8	Peripheral clock/8
4	CLK_DIV16	Peripheral clock/16
5	CLK_DIV32	Peripheral clock/32
6	CLK_DIV64	Peripheral clock/64
7	CLK_DIV128	Peripheral clock/128
8	CLK_DIV256	Peripheral clock/256
9	CLK_DIV512	Peripheral clock/512
10	CLK_DIV1024	Peripheral clock/1024
Other	–	Reserved

Bits 7:0 – DIVA[7:0] CLKA Divide Factor

Value	Name	Description
0	CLKA_POFF	CLKA clock is turned off
1	PREA	CLKA clock is clock selected by PREA
2-255	PREA_DIV	CLKA clock is clock selected by PREA divided by DIVA factor

52.7.12 AFEC Interrupt Mask Register

Name: AFEC_IMR
Offset: 0x2C
Reset: 0x00000000
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
		TEMPCHG				COMPE	GOVRE	DRDY
Access		R				R	R	R
Reset		0				0	0	0

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					EOC11	EOC10	EOC9	EOC8
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 30 – TEMPCHG Temperature Change Interrupt Mask

Bit 26 – COMPE Comparison Event Interrupt Mask

Bit 25 – GOVRE General Overrun Error Interrupt Mask

Bit 24 – DRDY Data Ready Interrupt Mask

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – EOCx End of Conversion Interrupt Mask x

57.5.9 AES Output Data Register x

Name: AES_ODATARx
Offset: 0x50 + x*0x04 [x=0..3]
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	ODATA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ODATA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

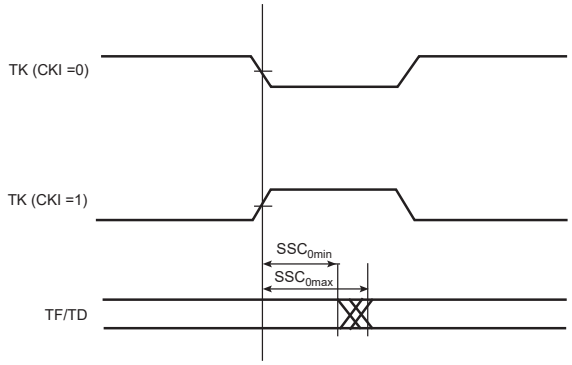
Bit	15	14	13	12	11	10	9	8
	ODATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ODATA[31:0] Output Data
The four 32-bit Output Data registers contain the 128-bit data block that has been encrypted/decrypted.

AES_ODATAR0 corresponds to the first word, AES_ODATAR3 to the last one.

Figure 58-41. Min and Max Access Time of Output Signals



58.13.1.15 ISI Timings

58.13.1.15.1 Timing Conditions

Timings are given assuming the load capacitance in the following table.

Table 58-76. Load Capacitance

Supply	C_L Max
3.3V	30 pF
1.7V	PBD

58.13.1.15.2 Timing Extraction

Table 58-77. ISI Timings with Peripheral Supply 3.3V

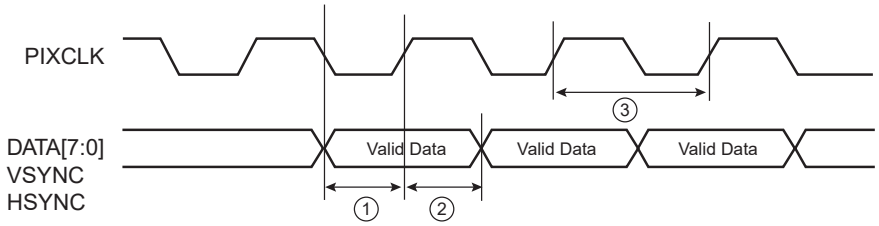
Symbol	Parameter	Min	Max	Unit
ISI_1	DATA/VSYNC/HSYNC setup time	1.5	–	ns
ISI_2	DATA/VSYNC/HSYNC hold time	-1.2	–	ns
ISI_3	PIXCLK frequency	–	75	MHz

Figure 58-42.

Table 58-78. ISI Timings with Peripheral Supply 1.8V

Symbol	Parameter	Min	Max	Unit
ISI_1	DATA/VSYNC/HSYNC setup time	1.8	–	ns
ISI_2	DATA/VSYNC/HSYNC hold time	-1.4	–	ns
ISI_3	PIXCLK frequency	–	75	MHz

Figure 58-43. ISI Timing Diagram



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Normal mode with one output on, DACC_ACR.IBCTLCHx =1 (see **Note 1**) FS = 500 KSps, no R_{LOAD}, V_{DDIN} = 3.3V	–	100	400	
		Bypass mode (output buffer off) with one output on, DACC_ACR.IBCTLCHx =0 (see **Note 1**) FS = 500 KSps, no R_{LOAD}, V_{DDIN} = 3.3V	–	10	30	
PSRR	Power Supply RejectionRatio (V_{DDIN})	V_{DDIN} ±10 mV Up to 10 kHz	–	70	–	dB

Note:

1. The maximum conversion rate versus the configuration of DACC_ACR.IBCTL is shown in the following table.

Table 59-44. Maximum Conversion Rate vs. Configuration of DACC_ACR.IBCTL

DACC_ACR.IBCTLCHx	Maximum Conversion Rate
0	Bypass
1	500 ks/s
2	N/A
3	1 Ms/s

Table 59-45. Voltage Reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VREFP}	Positive Voltage Reference	Externally decoupled 1 µF	1.7	–	V_{DDIN}	V
I_{VREFP}	DC Current on VREFP	–	–	2.5	–	µA

Note: V_{REFP} is the positive reference shared with AFE and may have a different value for AFE. Refer to the AFE electrical characteristics if AFE is used. The V_{REFN} pin must be connected to ground.

Table 59-46. DAC Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DAC}	DAC Clock Frequency	–	–	–	12	MHz
f_S	Sampling Frequency	–	–	f_{DAC} / 12	–	MHz