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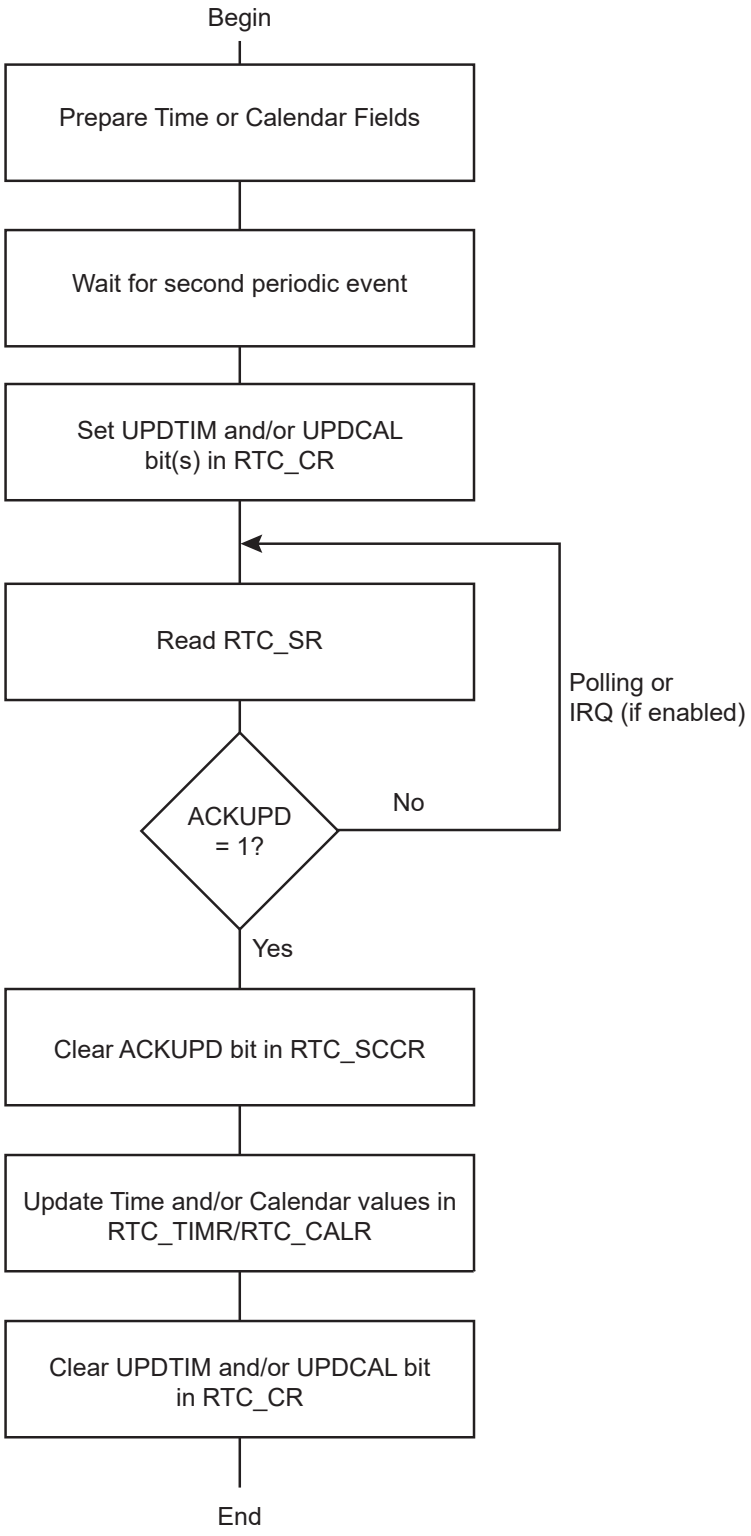
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70n21b-cnt

Figure 27-3. Gregorian and Persian Modes Update Sequence



27.5.7 RTC Accurate Clock Calibration

The crystal oscillator that drives the RTC may not be as accurate as expected mainly due to temperature variation. The RTC is equipped with circuitry able to correct slow clock crystal drift.

31.20.19 PMC Fast Startup Polarity Register

Name: PMC_FSPR
Offset: 0x0074
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FSTP15	FSTP14	FSTP13	FSTP12	FSTP11	FSTP10	FSTP9	FSTP8
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FSTP7	FSTP6	FSTP5	FSTP4	FSTP3	FSTP2	FSTP1	FSTP0
Access								
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 – FSTP Fast Startup Input Polarity x bits
Defines the active polarity of the corresponding wake-up input. If the corresponding wake-up input is enabled and at the FSTP level, it enables a fast restart signal.

When the I/O line is controlled by the PIO Controller, the pin can be configured to be driven. This is done by writing the Output Enable Register (PIO_OER) and Output Disable Register (PIO_ODR). The results of these write operations are detected in the Output Status Register (PIO_OSR). When a bit in this register is at zero, the corresponding I/O line is used as an input only. When the bit is at one, the corresponding I/O line is driven by the PIO Controller.

The level driven on an I/O line can be determined by writing in the Set Output Data Register (PIO_SODR) and the Clear Output Data Register (PIO_CODR). These write operations, respectively, set and clear the Output Data Status Register (PIO_ODSR), which represents the data driven on the I/O lines. Writing in PIO_OER and PIO_ODR manages PIO_OSR whether the pin is configured to be controlled by the PIO Controller or assigned to a peripheral function. This enables configuration of the I/O line prior to setting it to be managed by the PIO Controller.

Similarly, writing in PIO_SODR and PIO_CODR affects PIO_ODSR. This is important as it defines the first level driven on the I/O line.

32.5.5 Synchronous Data Output

Clearing one or more PIO line(s) and setting another one or more PIO line(s) synchronously cannot be done by using PIO_SODR and PIO_CODR. It requires two successive write operations into two different registers. To overcome this, the PIO Controller offers a direct control of PIO outputs by single write access to PIO_ODSR. Only bits unmasked by the Output Write Status Register (PIO_OWSR) are written. The mask bits in PIO_OWSR are set by writing to the Output Write Enable Register (PIO_OWER) and cleared by writing to the Output Write Disable Register (PIO_OWDR).

After reset, the synchronous data output is disabled on all the I/O lines as PIO_OWSR resets at 0x0.

32.5.6 Multi-Drive Control (Open Drain)

Each I/O can be independently programmed in open drain by using the multi-drive feature. This feature permits several drivers to be connected on the I/O line which is driven low only by each device. An external pullup resistor (or enabling of the internal one) is generally required to guarantee a high level on the line.

The multi-drive feature is controlled by the Multi-driver Enable Register (PIO_MDER) and the Multi-driver Disable Register (PIO_MDDR). The multi-drive can be selected whether the I/O line is controlled by the PIO Controller or assigned to a peripheral function. The Multi-driver Status Register (PIO_MDSR) indicates the pins that are configured to support external drivers.

After reset, the multi-drive feature is disabled on all pins, i.e., PIO_MDSR resets at value 0x0.

32.5.7 Output Line Timings

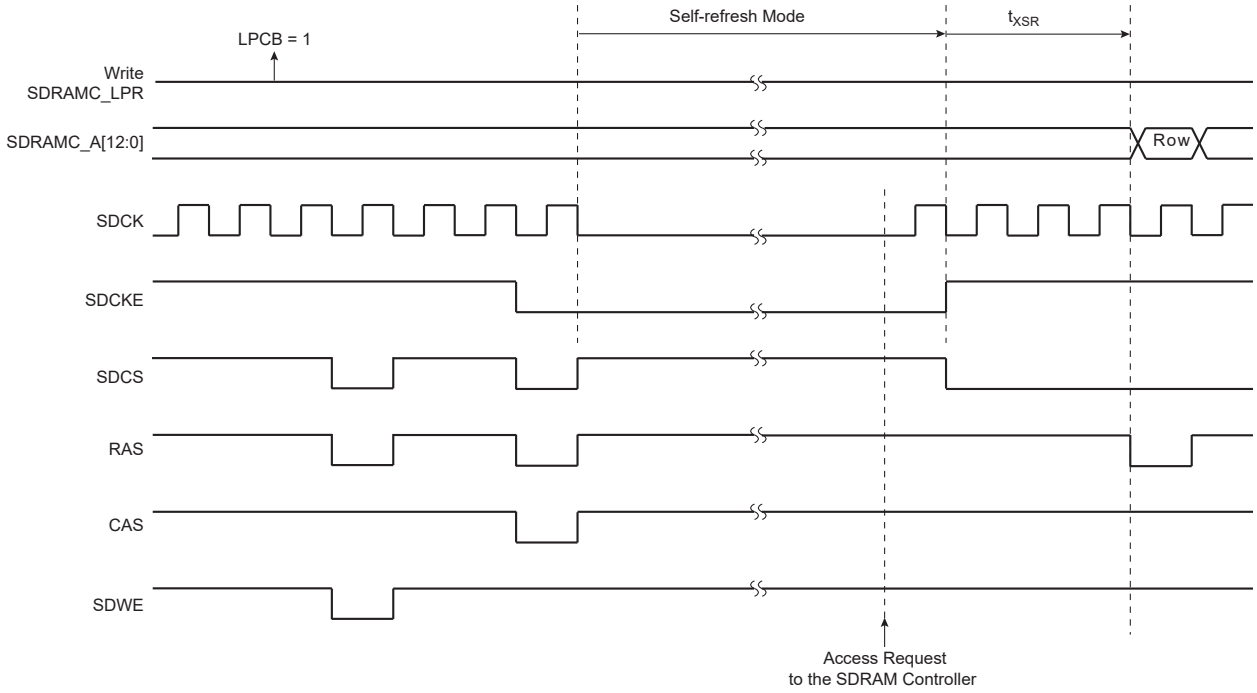
The following figure shows how the outputs are driven either by writing PIO_SODR or PIO_CODR, or by directly writing PIO_ODSR. This last case is valid only if the corresponding bit in PIO_OWSR is set. The Output Line Timings figure also shows when the feedback in the Pin Data Status Register (PIO_PDSR) is available.

After initialization, as soon as the PASR/DS/TCSR fields are modified and Self-refresh mode is activated, the Extended Mode register is accessed automatically and the PASR/DS/TCSR bits are updated before entry into Self-refresh mode. This feature is not supported when SDRAMC shares an external bus with another controller.

The SDRAM device must remain in Self-refresh mode for a minimum period of t_{RAS} and may remain in Self-refresh mode for an indefinite period. Refer to the following figure.

Note: Some SDRAM providers impose some cycles of burst autorefresh immediately before self-refresh entry and immediately after self-refresh exit. For example, a SDRAM with 4096 rows will impose 4096 cycles of burst autorefresh. This constraint is not supported.

Figure 34-6. Self-refresh Mode Behavior



34.6.5.2 Low-power Mode

This mode is selected by configuring SDRAMC_LPR.LPCB to 2. Power consumption is greater than in Self-refresh mode. All the input and output buffers of the SDRAM device are deactivated except SDCKE, which remains low. In contrast to Self-refresh mode, the SDRAM device cannot remain in Low-power mode longer than the refresh period (64 ms for a whole device refresh operation). As no autorefresh operations are performed by the SDRAM itself, the SDRAMC carries out the refresh operation. The exit procedure is faster than in Self-refresh mode.

Refer to the following figure.

38.8.53 GMAC Multiple Collision Frames Register

Name: GMAC_MCF
Offset: 0x13C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							MCOL[17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	MCOL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – MCOL[17:0] Multiple Collision
This register counts the number of frames experiencing between two and fifteen collisions prior to being successfully transmitted, i.e., no underrun and not too many retries.

Value	Name	Description
6	65536	CSTOCYC x 65536
7	1048576	CSTOCYC x 1048576

Bits 3:0 – CSTOCYC[3:0] Completion Signal Timeout Cycle Number
This field determines the maximum number of Master Clock cycles that the HSMCI waits between two data block transfers. Its value is calculated by (CSTOCYC x Multiplier).

41.8.6 SPI Interrupt Enable Register

Name: SPI_IER
Offset: 0x14
Reset: –
Property: Write-only

This register can only be written if the WPITEN bit is cleared in the SPI Write Protection Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						UNDES	TXEMPTY	NSSR
Access						W	W	W
Reset						–	–	–

Bit	7	6	5	4	3	2	1	0
					OVRES	MODF	TDRE	RDRF
Access					W	W	W	W
Reset					–	–	–	–

Bit 10 – UNDES Underrun Error Interrupt Enable

Bit 9 – TXEMPTY Transmission Registers Empty Enable

Bit 8 – NSSR NSS Rising Interrupt Enable

Bit 3 – OVRES Overrun Error Interrupt Enable

Bit 2 – MODF Mode Fault Error Interrupt Enable

Bit 1 – TDRE SPI Transmit Data Register Empty Interrupt Enable

Bit 0 – RDRF Receive Data Register Full Interrupt Enable

42.7.6 QSPI Interrupt Enable Register

Name: QSPI_IER
Offset: 0x14
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						INSTRE	CSS	CSR
Access						W	W	W
Reset						–	–	–

Bit	7	6	5	4	3	2	1	0
					OVRES	TXEMPTY	TDRE	RDRF
Access					W	W	W	W
Reset					–	–	–	–

Bit 10 – INSTRE Instruction End Interrupt Enable

Bit 9 – CSS Chip Select Status Interrupt Enable

Bit 8 – CSR Chip Select Rise Interrupt Enable

Bit 3 – OVRES Overrun Error Interrupt Enable

Bit 2 – TXEMPTY Transmission Registers Empty Enable

Bit 1 – TDRE Transmit Data Register Empty Interrupt Enable

Bit 0 – RDRF Receive Data Register Full Interrupt Enable

Source Clock (MHz)	Expected Baud Rate (bit/s)	Calculation Result	CD	Actual Baud Rate (bit/s)	Error
8,000,000	38,400	13.02	13	38,461.54	0.16%
12,000,000	38,400	19.53	20	37,500.00	2.40%
12,288,000	38,400	20.00	20	38,400.00	0.00%
14,318,180	38,400	23.30	23	38,908.10	1.31%
14,745,600	38,400	24.00	24	38,400.00	0.00%
18,432,000	38,400	30.00	30	38,400.00	0.00%
24,000,000	38,400	39.06	39	38,461.54	0.16%
24,576,000	38,400	40.00	40	38,400.00	0.00%
25,000,000	38,400	40.69	40	38,109.76	0.76%
32,000,000	38,400	52.08	52	38,461.54	0.16%
32,768,000	38,400	53.33	53	38,641.51	0.63%
33,000,000	38,400	53.71	54	38,194.44	0.54%
40,000,000	38,400	65.10	65	38,461.54	0.16%
50,000,000	38,400	81.38	81	38,580.25	0.47%
60,000,000	38,400	97.66	98	38,265.31	0.35%
70,000,000	38,400	113.93	114	38,377.19	0.06%

In this example, the baud rate is calculated with the following formula:

$$\text{Baud Rate} = \text{Selected Clock}/\text{CD} \times 16$$

The baud rate error is calculated with the following formula. It is not recommended to work with an error higher than 5%.

$$\text{Error} = 1 - \left(\frac{\text{Expected Baud Rate}}{\text{Actual Baud Rate}}\right)$$

46.6.1.2 Fractional Baud Rate in Asynchronous Mode

The baud rate generator is subject to the following limitation: the output frequency changes only by integer multiples of the reference frequency. An approach to this problem is to integrate a fractional N clock generator that has a high resolution. The generator architecture is modified to obtain baud rate changes by a fraction of the reference source clock. This fractional part is programmed using US_BRGR.FP. If FP is not 0, the fractional part is activated. The resolution is one-eighth of the clock divider. The fractional baud rate is calculated using the following formula:

$$\text{Baud Rate} = \frac{\text{Selected Clock}}{\left(8(2 - \text{OVER})\left(\text{CD} + \frac{\text{FP}}{8}\right)\right)}$$

The modified architecture is presented in the following figure.

Value	Description
0	Hardware clears interrupt after a MLB_ACSRn register read
1	Software writes a ‘1’ to clear

Table 49-9. Tx Event FIFO Element

	31			24	23						16	15	8	7	0
E0	ESI	XTD	RTR	ID[28:0]											
E1	MM[7:0]				ET [1:0]	FDF	BRS	DLC[3:0]				TXTS[15:0]			

• E0 Bit 31 ESI: Error State Indicator

0: Transmitting node is error active.

1: Transmitting node is error passive.

• E0 Bit 30 XTD: Extended Identifier

0: 11-bit standard identifier.

1: 29-bit extended identifier.

• E0 Bit 29 RTR: Remote Transmission Request

0: Data frame transmitted.

1: Remote frame transmitted.

• E0 Bits 28:0 ID[28:0]: Identifier

Standard or extended identifier depending on bit XTD. A standard identifier is stored into ID[28:18].

• E1 Bits 31:24 MM[7:0]: Message Marker

Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status.

• E1 Bit 23:22 ET[1:0]: Event Type

0: Reserved

1: Tx event

2: Transmission in spite of cancellation (always set for transmissions in DAR mode)

3: Reserved

• E1 Bit 21 FDF: FD Format

0: Standard frame format.

1: CAN FD frame format (new DLC-coding and CRC).

• E1 Bit 20 BRS: Bit Rate Switch

0: Frame transmitted without bit rate switching.

1: Frame transmitted with bit rate switching.

• E1 Bits 19:16 DLC[3:0]: Data Length Code

0-8: CAN + CAN FD: frame with 0-8 data bytes transmitted.

9-15: CAN: frame with 8 data bytes transmitted.

9-15: CAN FD: frame with 12/16/20/24/32/48/64 data bytes transmitted

• E1 Bits 15:0 TXTS[15:0]: Tx Timestamp

49.6.5 MCAN Test Register

Name: MCAN_TEST
Offset: 0x10
Reset: 0x00000000
Property: Read/Write

Write access to the Test Register has to be enabled by setting bit MCAN_CCCR.TEST to ‘1’.

All MCAN Test Register functions are set to their reset values when bit MCAN_CCCR.TEST is cleared.

Loop Back mode and software control of pin CANTX are hardware test modes. Programming of TX ≠ 0 disturbs the message transfer on the CAN bus.

The reset value for MCAN_TEST.RX is undefined.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RX	TX[1:0]		LBCK				
Access	R	R/W	R/W	R/W				
Reset	x	0	0	0				

Bit 7 – RX Receive Pin (read-only)
Monitors the actual value of pin CANRX.

The reset value for this bit is undefined.

Value	Description
0	The CAN bus is dominant (CANRX = ‘0’).
1	The CAN bus is recessive (CANRX = ‘1’).

Bits 6:5 – TX[1:0] Control of Transmit Pin (read/write)

Value	Name	Description
0	RESET	Reset value, CANTX controlled by the CAN Core, updated at the end of the CAN bit time.
1	SAMPLE_POINT_MONITORING	Sample Point can be monitored at pin CANTX.

50.7.2 TC Channel Mode Register: Capture Mode

Name: TC_CMRx
Offset: 0x04 + x*0x40 [x=0..2]
Reset: 0x00000000
Property: Read/Write

This register can be written only if the WPEN bit is cleared in the TC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		SBSMPLR[2:0]			LDRB[1:0]		LDRA[1:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WAVE	CPCTRG				ABETRG	ETRGEDG[1:0]	
Access	R/W	R/W				R/W	R/W	R/W
Reset	0	0				0	0	0

Bit	7	6	5	4	3	2	1	0
	LDBDIS	LDBSTOP	BURST[1:0]		CLKI	TCCLKS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:20 – SBSMPLR[2:0] Loading Edge Subsampling Ratio

Value	Name	Description
0	ONE	Load a Capture register each selected edge.
1	HALF	Load a Capture register every 2 selected edges.
2	FOURTH	Load a Capture register every 4 selected edges.
3	EIGHTH	Load a Capture register every 8 selected edges.
4	SIXTEENTH	Load a Capture register every 16 selected edges.

Bits 19:18 – LDRB[1:0] RB Loading Edge Selection

Value	Name	Description
0	NONE	None
1	RISING	Rising edge of TIOAx
2	FALLING	Falling edge of TIOAx
3	EDGE	Each edge of TIOAx

Bits 17:16 – LDRA[1:0] RA Loading Edge Selection

Bit 8 – QDEN Quadrature Decoder Enabled
Quadrature decoding (direction change) can be disabled using QDTRANS bit.

One of the POSEN or SPEEDEN bits must be also enabled.

Value	Description
0	Disabled.
1	Enables the QDEC (filter, edge detection and quadrature decoding).

Bits 5:4 – TC2XC2S[1:0] External Clock Signal 2 Selection

Value	Name	Description
0	TCLK2	Signal connected to XC2: TCLK2
1	–	Reserved
2	TIOA0	Signal connected to XC2: TIOA0
3	TIOA1	Signal connected to XC2: TIOA1

Bits 3:2 – TC1XC1S[1:0] External Clock Signal 1 Selection

Value	Name	Description
0	TCLK1	Signal connected to XC1: TCLK1
1	–	Reserved
2	TIOA0	Signal connected to XC1: TIOA0
3	TIOA2	Signal connected to XC1: TIOA2

Bits 1:0 – TC0XC0S[1:0] External Clock Signal 0 Selection

Value	Name	Description
0	TCLK0	Signal connected to XC0: TCLK0
1	–	Reserved
2	TIOA1	Signal connected to XC0: TIOA1
3	TIOA2	Signal connected to XC0: TIOA2

51.7.28 PWM Fault Protection Enable Register

Name: PWM_FPE
Offset: 0x6C
Reset: 0x00000000
Property: Read/Write

This register can only be written if bits WPSWS5 and WPHWS5 are cleared in the PWM Write Protection Status Register.

Only the first 8 bits (number of fault input pins) of the register fields are significant.

Refer to Section 6.4 “Fault Inputs” for details on fault generation.

Bit	31	30	29	28	27	26	25	24
	FPE3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	FPE2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FPE1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FPE0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

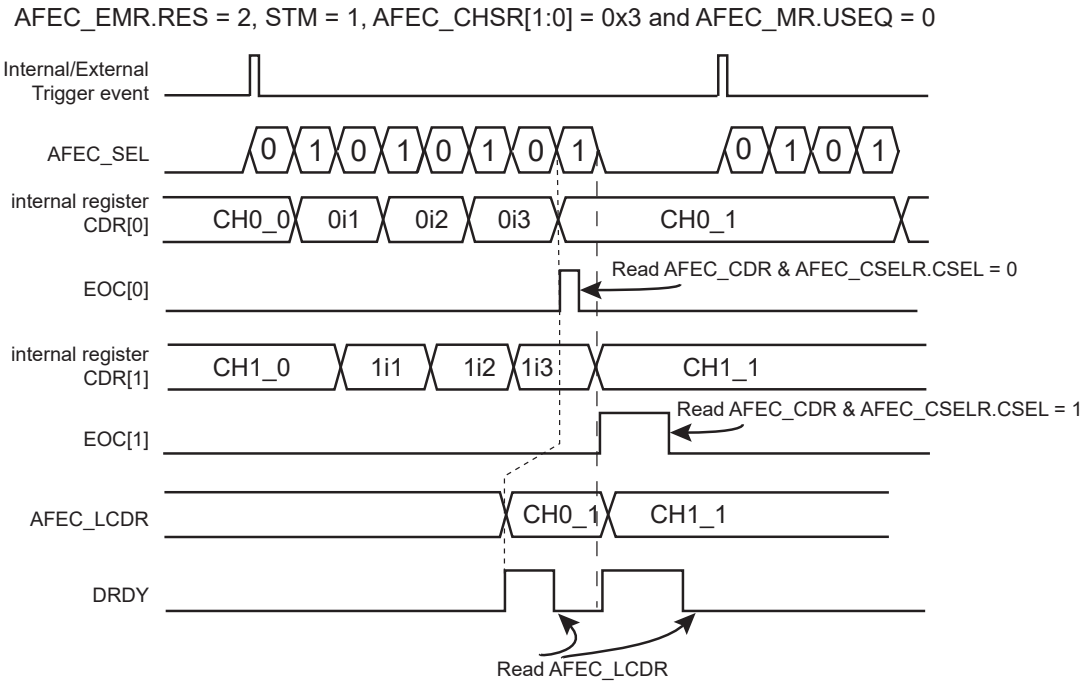
Bits 0:7, 8:15, 16:23, 24:31 – FPEx Fault Protection Enable for channel x
For each bit y of FPEx, where y is the fault input number:

0: Fault y is not used for the fault protection of channel x.

1: Fault y is used for the fault protection of channel x.

⚠ CAUTION To prevent an unexpected activation of the fault protection, the bit y of FPEx field can be set to ‘1’ only if the corresponding FPOL field has been previously configured to its final value in PWM Fault Mode Register.

Figure 52-12. Digital Averaging Function Waveforms on a Single Trigger Event



Note: 0i1, 0i2, 0i3, 1i1, 1i2, 1i3 are intermediate results and CH0/1_0/1 are final result of average function.

When USEQ is set, the user can define the channel sequence to be converted by configuring AFEC_SEQxR and AFEC_CHER so that channels are not interleaved during the averaging period. Under these conditions, a sample is defined for each end of conversion as described in the figure below.

Therefore, if the same channel is configured to be converted four times consecutively and AFEC_EMR.RES = 2, the averaging result is placed in the corresponding channel internal data register (read by means of the AFEC_CDR) and the AFEC_LCDR for each trigger event.

In this case, the AFE real sample rate remains the maximum AFE sample rate divided by 4.

When USEQ is set and the RES field enables the Enhanced Resolution mode, it is important to note that the user sequence must be a sequence being an integer multiple of 4 (i.e., the number of the enabled channel in the Channel Status register (AFEC_CHSR) must be an integer multiple of 4 and the AFEC_SEQxR must be a series of 4 times the same channel index).

Value	Name	Description
0	DISABLED	One data to convert is written to the FIFO per access to DACC.
1	ENABLED	Two data to convert are written to the FIFO per access to DACC (reduces the number of requests to DMA and the number of system bus accesses).

Bits 0, 1 – MAXSx Max Speed Mode for Channel x

Value	Name	Description
0	TRIG_EVENT	Trigger mode or Free-running mode enabled. (See TRGENx.DACC_TRIGR.)
1	MAXIMUM	Max speed mode enabled.

55.6.10 ICM Hash Area Start Address Register

Name: ICM_HASH
Offset: 0x34
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	HASA[24:17]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HASA[16:9]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HASA[8:1]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HASA[0:0]							
Access	R/W							
Reset	0							

Bits 31:7 – HASA[24:0] Hash Area Start Address
This field points at the Hash memory location. The address must be a multiple of 128 bytes.

24/12	9	6	8
12/12	5	4	5
8/8	4	3	4
4/4	2	2	2.5
4/2	2	1.5	2
4/1	1.5	1.5	1.5
2/2	1.5	1.5	1.5

Note: Flash Wait State (FWS) in EEFC_FMR is adjusted depending on core frequency.

58.4 Oscillator Characteristics

58.4.1 32 kHz RC Oscillator Characteristics

Table 58-18. 32 kHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	–	20	32	57	kHz
t_{START}	Startup Time	–	–	–	120	µs
I_{DDON}	Current Consumption	After startup time	–	540	–	nA

58.4.2 4/8/12 MHz RC Oscillator

The 4/8/12 MHz RC oscillator is calibrated in production. This calibration can be read through the Get CALIB Bit command (refer to 22. Enhanced Embedded Flash Controller (EEFC)) and the frequency can be trimmed by software through the PMC.

Table 58-19. 4/8/12 RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ACC_4	4 MHz Total Accuracy(2)	4 MHz output selected (see **Note 1**)	-35	–	46	%
		4 MHz output selected at 25°C (see **Notes 1, 3**)	-1.2	–	0.8	%
ACC_8	8 MHz Total Accuracy	8 MHz output selected at 25°C (see **Notes 1, 3**)	-1.2	–	0.8	%
ACC_{12}	12 MHz Total Accuracy	12 MHz output selected at 25°C (see **Notes 1, 3**)	-1.6	–	0.8	%
	Temp dependency	(see **Note 3**)	–	0.07	0.12	%/°C
t_{START}	Startup Time	–	–	–	20	µs

Note:

1. Frequency range can be configured in the Supply Controller registers.
2. Not trimmed from factory.

Symbol	Parameter	Conditions	Min	Max	Unit
SPI_{15}	NPCS hold after SPCK falling (slave)	3.3V domain	0	–	ns
		1.8V domain	0	–	ns

Timings are given for the 3.3V domain, with V_{DDIO} from 2.85V to 3.6V, maximum external capacitor = 40 pF.

Table 59-57. SPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
SPI_0	MISO Setup time before SPCK rises (master)	3.3V domain	12.4	–	ns
		1.7V domain	14.6	–	ns
SPI_1	MISO Hold time after SPCK rises (master)	3.3V domain	0	–	ns
		1.7V domain	0	–	ns
SPI_2	SPCK rising to MOSI Delay (master)	3.3V domain	-3.7	2.2	ns
		1.7V domain	-3.8	2.4	ns
SPI_3	MISO Setup time before SPCK falls (master)	3.3V domain	12.6	–	ns
		1.7V domain	15.13	–	ns
SPI_4	MISO Hold time after SPCK falls (master)	3.3V domain	0	–	ns
		1.7V domain	0	–	ns
SPI_5	SPCK falling to MOSI Delay (master)	3.3V domain	-3.6	2.0	ns
		1.7V domain	-3.3	2.8	ns
SPI_6	SPCK falling to MISO Delay (slave)	3.3V domain	3.0	11.9	ns
		1.7V domain	3.5	13.9	ns
SPI_7	MOSI Setup time before SPCK rises (slave)	3.3V domain	1.2	–	ns
		1.7V domain	1.5	–	ns
SPI_8	MOSI Hold time after SPCK rises (slave)	3.3V domain	0.6	–	ns
		1.7 domain	0.8	–	ns
SPI_9	SPCK rising to MISO Delay (slave)	3.3V domain	3.0	12.0	ns
		1.7V domain	3.4	13.7	ns
SPI_{10}	MOSI Setup time before SPCK falls (slave)	3.3V domain	1.2	–	ns
		1.7V domain	1.5	–	ns
SPI_{11}	MOSI Hold time after SPCK falls (slave)	3.3V domain	0.6	–	ns
		1.7V domain	0.8	–	ns
SPI_{12}	NPCS setup to SPCK rising (slave)	3.3V domain	3.9	–	ns
		1.7V domain	4.4	–	ns