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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q19a-cn

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LQFP Pin	LFBGA/ TFBGA Ball	UFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
					Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
77	K12	L12	VDDIO	GPIO	PA4	I/O	WKUP3/ PIODC1(3)	I	TWCK0	O	TCLK0	I	UTXD1	O	–	–	PIO, I, PU, ST
73	M11	N13	VDDIO	GPIO_AD	PA5	I/O	WKUP4/ PIODC2(3)	I	PWMC1_PWML3	O	ISI_D4	I	URXD1	I	–	–	PIO, I, PU, ST
114	B9	B11	VDDIO	GPIO_AD	PA6	I/O	–	–	–	–	PCK0	O	UTXD1	O	–	–	PIO, I, PU, ST
35	L2	N1	VDDIO	CLOCK	PA7	I/O	XIN32(4)	I	–	–	PWMC0_PWMH3	O	–	–	–	–	PIO, HiZ
36	M2	N2	VDDIO	CLOCK	PA8	I/O	XOUT32(4)	O	PWMC1_PWMH3	O	AFE0_ADTRG	I	–	–	–	–	PIO, HiZ
75	M12	L11	VDDIO	GPIO_AD	PA9	I/O	WKUP6/ PIODC3(3)	I	URXD0	I	ISI_D3	I	PWMC0_PWMFI0	I	–	–	PIO, I, PU, ST
66	L9	M10	VDDIO	GPIO_AD	PA10	I/O	PIODC4(2)	I	UTXD0	O	PWMC0_PWMEXTRG0	I	RD	I	–	–	PIO, I, PU, ST
64	J9	N10	VDDIO	GPIO_AD	PA11	I/O	WKUP7/ PIODC5(3)	I	QCS	O	PWMC0_PWMH0	O	PWMC1_PWML0	O	–	–	PIO, I, PU, ST
68	L10	N11	VDDIO	GPIO_AD	PA12	I/O	PIODC6(2)	I	QIO1	I/O	PWMC0_PWMH1	O	PWMC1_PWMH0	O	–	–	PIO, I, PU, ST
42	M3	M4	VDDIO	GPIO_AD	PA13	I/O	PIODC7(2)	I	QIO0	I/O	PWMC0_PWMH2	O	PWMC1_PWML1	O	–	–	PIO, I, PU, ST
51	K6	M6	VDDIO	GPIO_CLK	PA14	I/O	WKUP8/ PIODCEN1(3)	I	QSCK	O	PWMC0_PWMH3	O	PWMC1_PWMH1	O	–	–	PIO, I, PU, ST
49	L5	N6	VDDIO	GPIO_AD	PA15	I/O	–	–	D14	I/O	TIOA1	I/O	PWMC0_PWML3	O	I2SC0_WS	I/O	PIO, I, PU, ST
45	K5	L4	VDDIO	GPIO_AD	PA16	I/O	–	–	D15	I/O	TIOB1	I/O	PWMC0_PWML2	O	I2SC0_DI	I	PIO, I, PU, ST
25	J1	J4	VDDIO	GPIO_AD	PA17	I/O	AFE0_AD6(5)	I	QIO2	I/O	PCK1	O	PWMC0_PWMH3	O	–	–	PIO, I, PU, ST
24	H2	J3	VDDIO	GPIO_AD	PA18	I/O	AFE0_AD7(5)	I	PWMC1_PWMEXTRG1	I	PCK2	O	A14	O	–	–	PIO, I, PU, ST
23	H1	J2	VDDIO	GPIO_AD	PA19	I/O	AFE0_AD8/ WKUP9(6)	I	–	–	PWMC0_PWML0	O	A15	O	I2SC1_MCK	O	PIO, I, PU, ST
22	H3	J1	VDDIO	GPIO_AD	PA20	I/O	AFE0_AD9/ WKUP10(6)	I	–	–	PWMC0_PWML1	O	A16/BA0	O	I2SC1_CK	I/O	PIO, I, PU, ST
32	K2	M1	VDDIO	GPIO_AD	PA21	I/O	AFE0_AD1/ PIODCEN2(8)	I	RXD1	I	PCK1	O	PWMC1_PWMFI0	I	–	–	PIO, I, PU, ST
37	K3	M2	VDDIO	GPIO_AD	PA22	I/O	PIODCCLK(2)	I	RK	I/O	PWMC0_PWMEXTRG1	I	NCS2	O	–	–	PIO, I, PU, ST
46	L4	N5	VDDIO	GPIO_AD	PA23	I/O	–	–	SCK1	I/O	PWMC0_PWMH0	O	A19	O	PWMC1_PWML2	O	PIO, I, PU, ST
56	L7	N8	VDDIO	GPIO_AD	PA24	I/O	–	–	RTS1	O	PWMC0_PWMH1	O	A20	O	ISI_PCK	I	PIO, I, PU, ST
59	K8	L8	VDDIO	GPIO_AD	PA25	I/O	–	–	CTS1	I	PWMC0_PWMH2	O	A23	O	MCCK	O	PIO, I, PU, ST
62	J8	M9	VDDIO	GPIO	PA26	I/O	–	–	DCD1	I	TIOA2	O	MCDA2	I/O	PWMC1_PWMFI1	I	PIO, I, PU, ST
70	J10	N12	VDDIO	GPIO_AD	PA27	I/O	–	–	DTR1	O	TIOB2	I/O	MCDA3	I/O	ISI_D7	I	PIO, I, PU, ST
112	C9	C11	VDDIO	GPIO	PA28	I/O	–	–	DSR1	I	TCLK1	I	MCCDA	I/O	PWMC1_PWMFI2	I	PIO, I, PU, ST

Table 18-12. Get GP NVM Bit Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	GGPB
2	Read handshaking	DATA	GP NVM Bit Mask Status 0 = GP NVM bit is cleared 1 = GP NVM bit is set

18.3.5.6 Flash Security Bit Command

A security bit can be set using the Set Security Bit command (SSE). Once the security bit is active, the Fast Flash programming is disabled. No other command can be run. An event on the Erase signal can erase the security bit once the contents of the Flash have been erased.

Table 18-13. Set Security Bit Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	SSE
2	Write handshaking	DATA	0

Once the security bit is set, it is not possible to access FFPI. The only way to erase the security bit is to erase the Flash.

To erase the Flash, perform the following steps:

1. Power off the chip.
2. Power on the chip with TST = 0.
3. Assert the ERASE signal for at least the ERASE pin assertion time as defined in the section “Electrical Characteristics”.
4. Power off the chip.

Return to FFPI mode to check that the Flash is erased.

18.3.5.7 Memory Write Command

This command is used to perform a write access to any memory location.

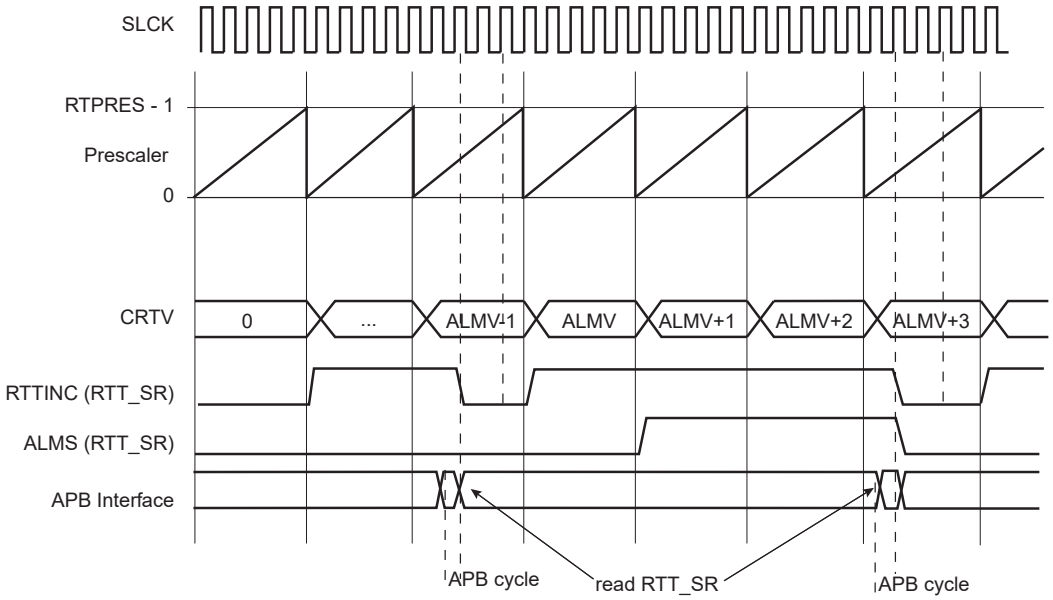
The Memory Write command (WRAM) is optimized for consecutive writes. Write handshaking can be chained; an internal address buffer is automatically increased.

Table 18-14. Write Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	WRAM
2	Write handshaking	ADDR0	Memory Address LSB
3	Write handshaking	ADDR1	Memory Address
4	Write handshaking	DATA	*Memory Address++
5	Write handshaking	DATA	*Memory Address++
...	...	...	...

Offset	Name	Bit Pos.								
		15:8				SYSIO12				
		23:16	CAN1DMABA[7:0]							
		31:24	CAN1DMABA[15:8]							
0x0118	CCFG_PCCR	7:0								
		15:8								
		23:16		I2SC1CC	I2SC0CC	TC0CC				
		31:24								
0x011C	CCFG_DYNCKG	7:0						EFCCKG	BRIDCKG	MATCKG
		15:8								
		23:16								
		31:24								
0x0120 ... 0x0123	Reserved									
0x0124	CCFG_SMCNFCS	7:0				SDRAMEN	SMC_NFCS3	SMC_NFCS2	SMC_NFCS1	SMC_NFCS0
		15:8								
		23:16								
		31:24								
0x0128 ... 0x01E3	Reserved									
0x01E4	MATRIX_WPMR	7:0								WPEN
		15:8	WPKEY[7:0]							
		23:16	WPKEY[15:8]							
		31:24	WPKEY[23:16]							
0x01E8	MATRIX_WPSR	7:0								WPVS
		15:8	WPVSRC[7:0]							
		23:16	WPVSRC[15:8]							
		31:24								

Figure 28-2. RTT Counting

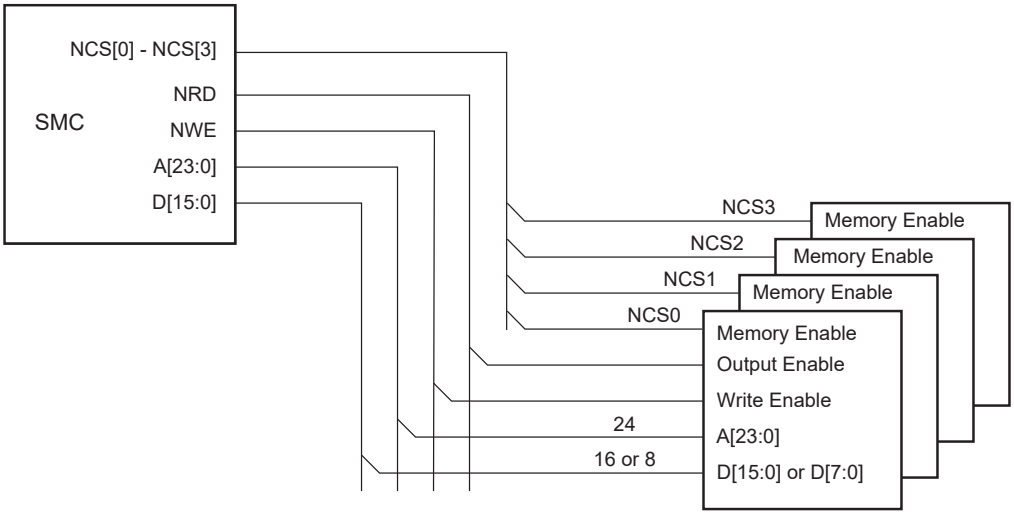


35.6 External Memory Mapping

The SMC provides up to 24 address lines, A[23:0]. This allows each chip select line to address up to 16 Mbytes of memory.

If the physical memory device connected on one chip select is smaller than 16 Mbytes, it wraps around and appears to be repeated within this space. The SMC correctly handles any valid access to the memory device within the page (see the following figure).

Figure 35-1. Memory Connections for Four External Devices



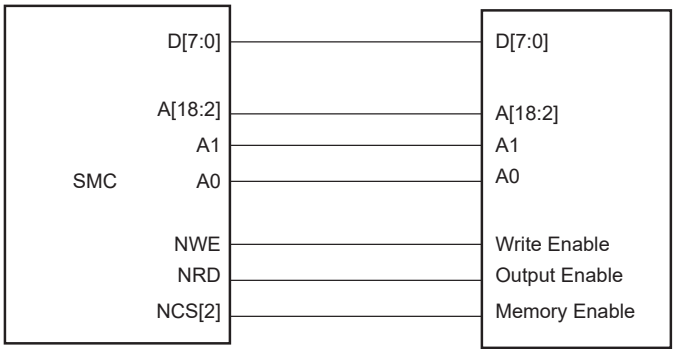
35.7 Connection to External Devices

35.7.1 Data Bus Width

A data bus width of 8 or 16 bits can be selected for each chip select. This option is controlled by the bit DBW in the Mode register (SMC_MODE) for the corresponding chip select.

Figure 35-2 shows how to connect a 512-Kbyte × 8-bit memory on NCS2. Figure 35-3 shows how to connect a 512-Kbyte × 16-bit memory on NCS2.

Figure 35-2. Memory Connection for an 8-bit Data Bus



38.8.72 GMAC Oversized Frames Received Register

Name: GMAC_OFR
Offset: 0x188
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							OFRX[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	OFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – OFRX[9:0] Oversized Frames Received
This pit field counts the number of frames received exceeding 1518 Bytes in length (1536 Bytes if GMAC_NCFGR.MAXFS is written to '1') but do not have either a CRC error, an alignment error, nor a receive symbol error.

38.8.107 GMAC Credit-Based Shaping IdleSlope Register for Queue B

Name: GMAC_CBSISQB
Offset: 0x4C4
Reset: 0x00000000
Property: Read/Write

Credit-based shaping must be disabled in the GMAC_CBSCR before updating this register.

Bit	31	30	29	28	27	26	25	24
	IS[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	IS[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IS[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IS[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – IS[31:0] IdleSlope
IdleSlope value for queue B in bytes/second.

The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the port transmit rate which is dependent on the speed of operation, e.g., 100 Mb/second = 32'h017D7840.

If 50% of bandwidth was to be allocated to a particular queue in 100 Mb/sec mode, then the IdleSlope value for that queue would be calculated as 32'h017D7840 / 2

Offset	Name	Bit Pos.								
		31:24		BYCT[10:4]						
0x0144	USBHS_DEVEPTISR5	7:0	SHORTPACKET	STALLEDI	OVERFI	NAKINI	NAKOUTI	RXSTPI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK	CTRLDIR	RWALL
		31:24		BYCT[10:4]						
0x0144	USBHS_DEVEPTISR5 (ISOENPT)	7:0	SHORTPACKET	CRCERRI	OVERFI	HBISOFLUSHI	HBISOINERRI	UNDERFI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]			ERRORTRANS	DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK		RWALL
		31:24		BYCT[10:4]						
0x0148	USBHS_DEVEPTISR6	7:0	SHORTPACKET	STALLEDI	OVERFI	NAKINI	NAKOUTI	RXSTPI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK	CTRLDIR	RWALL
		31:24		BYCT[10:4]						
0x0148	USBHS_DEVEPTISR6 (ISOENPT)	7:0	SHORTPACKET	CRCERRI	OVERFI	HBISOFLUSHI	HBISOINERRI	UNDERFI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]			ERRORTRANS	DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK		RWALL
		31:24		BYCT[10:4]						
0x014C	USBHS_DEVEPTISR7	7:0	SHORTPACKET	STALLEDI	OVERFI	NAKINI	NAKOUTI	RXSTPI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK	CTRLDIR	RWALL
		31:24		BYCT[10:4]						
0x014C	USBHS_DEVEPTISR7 (ISOENPT)	7:0	SHORTPACKET	CRCERRI	OVERFI	HBISOFLUSHI	HBISOINERRI	UNDERFI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]			ERRORTRANS	DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK		RWALL
		31:24		BYCT[10:4]						
0x0150	USBHS_DEVEPTISR8	7:0	SHORTPACKET	STALLEDI	OVERFI	NAKINI	NAKOUTI	RXSTPI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK	CTRLDIR	RWALL
		31:24		BYCT[10:4]						
0x0150	USBHS_DEVEPTISR8 (ISOENPT)	7:0	SHORTPACKET	CRCERRI	OVERFI	HBISOFLUSHI	HBISOINERRI	UNDERFI	RXOUTI	TXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]			ERRORTRANS	DTSEQ[1:0]	
		23:16	BYCT[3:0]					CFGOK		RWALL
		31:24		BYCT[10:4]						
0x0154	USBHS_DEVEPTISR9	7:0	SHORTPACKET	STALLEDI	OVERFI	NAKINI	NAKOUTI	RXSTPI	RXOUTI	TXINI

Bit 16 – RWALL Read/Write Allowed
For an OUT pipe, this bit is set when the current bank is not full, i.e., the software can write further data into the FIFO.

For an IN pipe, this bit is set when the current bank is not empty, i.e., the software can read further data from the FIFO.

This bit is cleared otherwise.

This bit is also cleared when RXSTALLDI or PERRI = 1.

Bits 15:14 – CURRBK[1:0] Current Bank
For a non-control pipe, this field indicates the number of the current bank.

This field may be updated 1 clock cycle after the RWALL bit changes, so the user should not poll it as an interrupt bit.

Value	Name	Description
0	BANK0	Current bank is bank0
1	BANK1	Current bank is bank1
2	BANK2	Current bank is bank2
3	Reserved	

Bits 13:12 – NBUSYBK[1:0] Number of Busy Banks
This field indicates the number of busy banks.

For an OUT pipe, this field indicates the number of busy banks, filled by the user, ready for an OUT transfer. When all banks are busy, this triggers a PEP_x interrupt if USBHS_HSTPIPIMRx.NBUSYBKE = 1.

For an IN pipe, this field indicates the number of busy banks filled by IN transaction from the device. When all banks are free, this triggers a PEP_x interrupt if USBHS_HSTPIPIMRx.NBUSYBKE = 1.

Value	Name	Description
0	0_BUSY	0 busy bank (all banks free)
1	1_BUSY	1 busy bank
2	2_BUSY	2 busy banks
3	3_BUSY	3 busy banks

Bits 9:8 – DTSEQ[1:0] Data Toggle Sequence
This field indicates the data PID of the current bank.

For an OUT pipe, this field indicates the data toggle of the next packet that is to be sent.

For an IN pipe, this field indicates the data toggle of the received packet stored in the current bank.

Value	Name	Description
0	DATA0	Data0 toggle sequence
1	DATA1	Data1 toggle sequence
2	Reserved	
3	Reserved	

Bit 7 – SHORTPACKETI Short Packet Interrupt

42.7.3 QSPI Receive Data Register

Name: QSPI_RDR
Offset: 0x08
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RD[15:0] Receive Data
Data received by the QSPI is stored in this register right-justified. Unused bits read zero.

44.9.7 SSC Receive Holding Register

Name: SSC_RHR
Offset: 0x20
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	RDAT[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

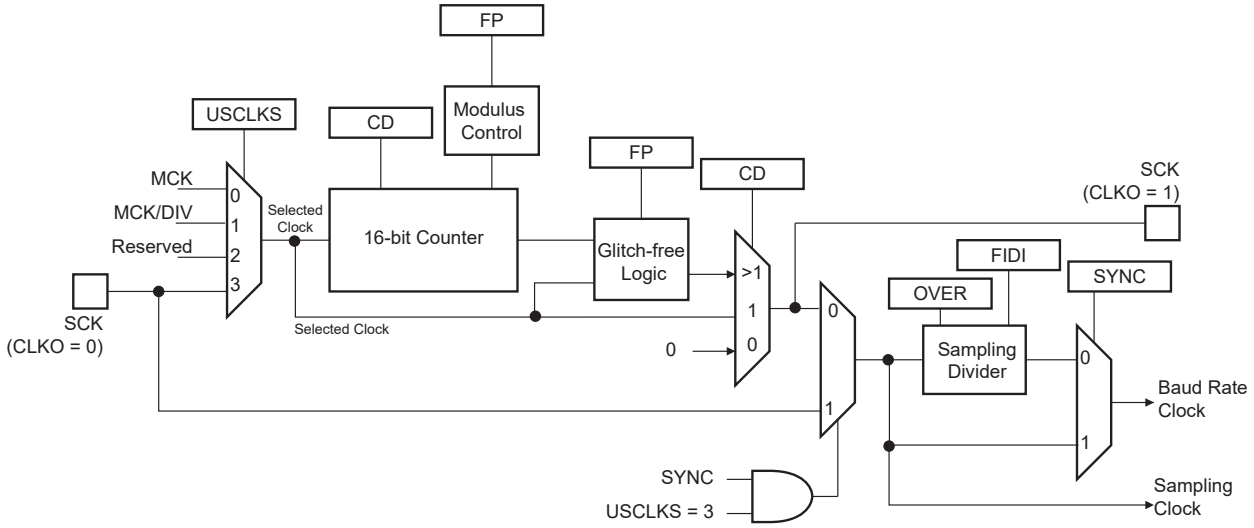
Bit	23	22	21	20	19	18	17	16
	RDAT[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RDAT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RDAT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RDAT[31:0] Receive Data
Right aligned regardless of the number of data bits defined by DATLEN in SSC_RFMR.

Figure 46-3. Fractional Baud Rate Generator



WARNING When the value of US_BRGR.FP is greater than '0', the SCK (oversampling clock) generates non-constant duty cycles. The SCK high duration is increased by “selected clock” period from time to time. The duty cycle depends on the value of USART_BRGR.CD.

46.6.1.3 Baud Rate in Synchronous Mode or SPI Mode

If the USART is programmed to operate in Synchronous mode, the selected clock is divided by the value of US_BRGR.CD.

$$\text{Baud Rate} = \frac{\text{Selected Clock}}{\text{CD}}$$

In Synchronous mode, if the external clock is selected (USCLKS = 3), the clock is provided directly by the signal on the USART SCK pin. No division is active. The value written in US_BRGR has no effect. The external clock frequency must be at least 3 times lower than the system clock. In Master mode, Synchronous mode (USCLKS = 0 or 1, CLKO set to 1), the receive part limits the SCK maximum frequency to Selected Clock/3 in USART mode, or Selected Clock/6 in SPI mode.

When either the external clock SCK or the internal clock divided (peripheral clock/DIV) is selected, the value of CD must be even if the user has to ensure a 50:50 mark/space ratio on the SCK pin. When the peripheral clock is selected, the baud rate generator ensures a 50:50 duty cycle on the SCK pin, even if the value of CD is odd.

46.6.1.4 Baud Rate in ISO 7816 Mode

The ISO7816 specification defines the bit rate with the following formula:

$$B = \frac{\text{Di}}{\text{Fi}} \times f$$

where:

- B is the bit rate
- Di is the bit-rate adjustment factor
- Fi is the clock frequency division factor
- f is the ISO7816 clock frequency (Hz)

NACT(slave1)=PUBLISH

NACT(slave2)=SUBSCRIBE

- Data transfer from the slave2 to the master and to the slave1:

NACT(master)=SUBSCRIBE

NACT(slave1)=SUBSCRIBE

NACT(slave2)=PUBLISH

46.6.9.11 Response Data Length

The LIN response data length is the number of data fields (bytes) of the response excluding the checksum.

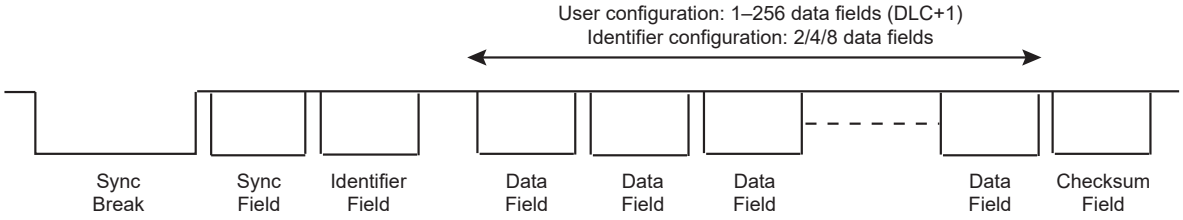
The response data length can either be configured by the user or be defined automatically by bits 4 and 5 of the Identifier (compatibility to LIN Specification 1.1). The user can choose between these two modes using the US_LINMR.DLM:

- DLM = 0: The response data length is configured by the user via US_LINMR.DLC. The response data length is equal to (DLC + 1) bytes. DLC can be programmed from 0 to 255, so the response can contain from 1 data byte up to 256 data bytes.
- DLM = 1: The response data length is defined by the Identifier (US_LINIR.IDCHR) according to the table below. The US_LINMR.DLC is discarded. The response can contain 2 or 4 or 8 data bytes.

Table 46-13. Response Data Length if DLM = 1

IDCHR[5]	IDCHR[4]	Response Data Length [Bytes]
0	0	2
0	1	2
1	0	4
1	1	8

Figure 46-43. Response Data Length



46.6.9.12 Checksum

The last field of a frame is the checksum. The checksum contains the inverted 8-bit sum with carry, over all data bytes or all data bytes and the protected identifier. Checksum calculation over the data bytes only is called classic checksum and it is used for communication with LIN 1.3 slaves. Checksum calculation over the data bytes and the protected identifier byte is called enhanced checksum and it is used for communication with LIN 2.0 slaves.

The USART can be configured to:

- Send/Check an Enhanced checksum automatically (CHKDIS = 0 & CHKTYP = 0)
- Send/Check a Classic checksum automatically (CHKDIS = 0 & CHKTYP = 1)

46.6.10.9 LON Errors

All these flags can be read in the Channel Status register (LON_MODE) (US_CSR) and will generate interrupts if configured in the Interrupt Enable register (LON_MODE) (US_IER).

These flags can be reset through US_CR.RSTSTA.

46.6.10.9.1 Underrun Error

If the USART is in LON mode and if a character is sent while the Transmit Holding register (US_THR) is empty, the UNRE bit flag is set.

46.6.10.9.2 Collision Detection

The LCOL flag is set whenever a valid collision has been detected and the LON node is configured to report it (see “Collision Detection”).

46.6.10.9.3 LON Frame Early Termination

The LFET flag is set whenever a LON frame has been terminated early due to collision detection.

46.6.10.9.4 Reception Error

The LCRCE flag is set if the received frame has an erroneous CRC and the flag LSFE is set if the received frame is too short (LON frames must be at least 8 bytes long).

These flags can be read in US_CSR.

46.6.10.9.5 Backlog Overflow

The LBLOVFE flag is set if the LON node backlog estimation goes over 63 which is the maximum backlog value.

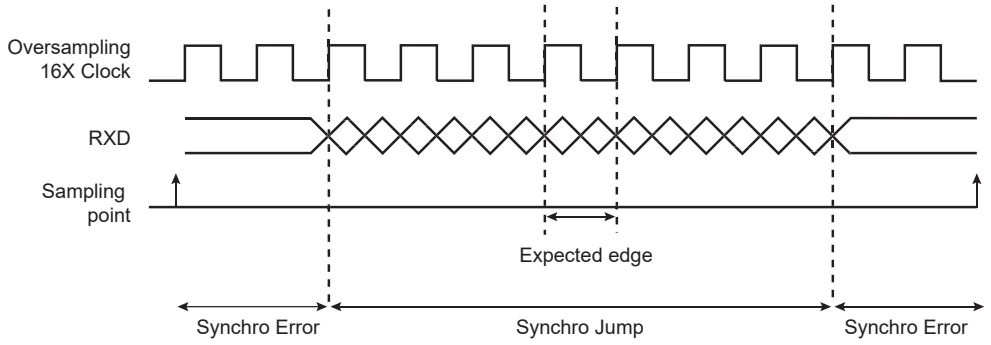
46.6.10.10 Drift Compensation

While receiving a frame, the baud rate used by the sender may not be exactly the one expected. In this case, the hardware drift compensation algorithm recovers up to 16% clock drift (expected baud rate ±16% will be supported).

Drift compensation is available only in 16X Oversampling mode. To enable the hardware system, US_MAN.DRIFT must be set. If the RXD edge is between one and three 16X clock cycles far from the expected edge, then the period is shortened or lengthened accordingly, to center the RXD edge.

The drift compensation hardware feature allows up to 16% clock drift to be handled, provided the system clock is fast enough compared to the selected baud rate.

Figure 46-60. Bit Resynchronization



46.6.10.11 LON Frame Handling

46.6.10.11.1 Sending A Frame

1. Write TXEN and RXEN in US_CR to enable both the transmitter and the receiver.
2. Write USART_MODE in US_MR to select the LON mode configuration.

Value	Description
0	No complete character has been received since the last read of US_RHR or the receiver is disabled. If characters were being received when the receiver was disabled, RXRDY changes to 1 when the receiver is enabled.
1	At least one complete character has been received and US_RHR has not yet been read.

51.7.41 PWM Channel Duty Cycle Register

Name: PWM_CDTYx
Offset: 0x0204 + x*0x20 [x=0..3]
Reset: 0x00000000
Property: Read/Write

Only the first 16 bits (channel counter size) are significant.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CDTY[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CDTY[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CDTY[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – CDTY[23:0] Channel Duty-Cycle
Defines the waveform duty-cycle. This value must be defined between 0 and CPRD (PWM_CPRDx).

Offset	Name	Bit Pos.								
		31:24		TEMPCHG				COMPE	GOVRE	DRDY
0x2C	AFEC_IMR	7:0	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
		15:8					EOC11	EOC10	EOC9	EOC8
		23:16								
		31:24		TEMPCHG				COMPE	GOVRE	DRDY
0x30	AFEC_ISR	7:0	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
		15:8					EOC11	EOC10	EOC9	EOC8
		23:16								
		31:24		TEMPCHG				COMPE	GOVRE	DRDY
0x34 ... 0x4B	Reserved									
0x4C	AFEC_OVER	7:0	OVRE7	OVRE6	OVRE5	OVRE4	OVRE3	OVRE2	OVRE1	OVRE0
		15:8					OVRE11	OVRE10	OVRE9	OVRE8
		23:16								
		31:24								
0x50	AFEC_CWR	7:0	LOWTHRES[7:0]							
		15:8	LOWTHRES[15:8]							
		23:16	HIGHTHRES[7:0]							
		31:24	HIGHTHRES[15:8]							
0x54	AFEC_CGR	7:0	GAIN3[1:0]		GAIN2[1:0]		GAIN1[1:0]		GAIN0[1:0]	
		15:8	GAIN7[1:0]		GAIN6[1:0]		GAIN5[1:0]		GAIN4[1:0]	
		23:16	GAIN11[1:0]		GAIN10[1:0]		GAIN9[1:0]		GAIN8[1:0]	
		31:24								
0x58 ... 0x5F	Reserved									
0x60	AFEC_DIFFR	7:0	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0
		15:8					DIFF11	DIFF10	DIFF9	DIFF8
		23:16								
		31:24								
0x64	AFEC_CSELR	7:0					CSEL[3:0]			
		15:8								
		23:16								
		31:24								
0x68	AFEC_CDR	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16								
		31:24								
0x6C	AFEC_COCR	7:0	AOFF[7:0]							
		15:8							AOFF[9:8]	
		23:16								
		31:24								
0x70	AFEC_TEMPMR	7:0			TEMPCMPMOD[1:0]					RTCT
		15:8								
		23:16								

Table 58-59. SMC Read Signals - NCS Controlled (READ_MODE = 0)

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
NO HOLD Settings (NCS_RD_HOLD = 0)						
SMC_8	Data Setup before NCS High	24.9	21.4	–	–	ns
SMC_9	Data Hold after NCS High	0	0	–	–	ns
HOLD Settings (NCS_RD_HOLD ≠ 0)						
SMC_{10}	Data Setup before NCS High	13.4	11.7	–	–	ns
SMC_{11}	Data Hold after NCS High	0	0	–	–	ns
HOLD or NO HOLD Settings (NCS_RD_HOLD ≠ 0, NCS_RD_HOLD = 0)						
SMC_{12}	A0–A22 valid before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE) × t_{CPMCK} - 4.0	(NCS_RD_SETUP + NCS_RD_PULSE) × t_{CPMCK} - 3.9	–	–	ns
SMC_{13}	NRD low before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE - NRD_SETUP) × t_{CPMCK} - 2.8	(NCS_RD_SETUP + NCS_RD_PULSE - NRD_SETUP) × t_{CPMCK} - 4.2	–	–	ns
SMC_{14}	NCS Pulse Width	NCS_RD_PULSE length × t_{CPMCK} - 0.9	NCS_RD_PULSE length × t_{CPMCK} - 0.2	–	–	ns

58.13.1.9.2 Read Timings

Table 58-60. SMC Read Signals - NRD Controlled (READ_MODE = 1)

Symbol		VDDIO Supply		Unit
	Parameter	Min	Max	
NO HOLD Settings (NRD_HOLD = 0)				
SMC_1	Data Setup before NRD High	14.3	–	ns
SMC_2	Data Hold after NRD High	0	–	ns
HOLD Settings (NRD_HOLD ≠ 0)				
SMC_3	Data Setup before NRD High	12.1	–	ns
SMC_4	Data Hold after NRD High	0	–	ns
HOLD or NO HOLD Settings (NRD_HOLD ≠ 0, NRD_HOLD = 0)				

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{SHUNT}	Shunt capacitance	–	–	–	7	pF
$C_{CRYSTAL}$	Allowed Crystal Capacitance Load	From crystal specification	12.5	–	17.5	pF
P_{ON}	Drive Level	3 MHz	–	–	15	µW
		8 MHz	–	–	30	
		12 MHz, 20 MHz	–	–	50	

59.4.8 3 to 20 MHz XIN Clock Input Characteristics in Bypass Mode

Table 59-25. 3 to 20 MHz XIN Clock Input Characteristics in Bypass Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN Clock Frequency	(see **Note 1**)	–	–	20	MHz
t_{CHXIN}	XIN Clock High Half-period	(see **Note 1**)	25	–	–	ns
t_{CLXIN}	XIN Clock Low Half-period	(see **Note 1**)	25	–	–	ns
V_{XIN_IL}	V_{XIN} Input Low-level Voltage	(see **Note 1**)	Min of V_{IL} for CLOCK pad	–	Max of V_{IL} for CLOCK pad	V
V_{XIN_IH}	V_{XIN} Input High-level Voltage	(see **Note 1**)	Min of V_{IH} for CLOCK pad	–	Max of V_{IH} for CLOCK pad	V

Note:

1. These characteristics apply only when the 3–20 MHz crystal oscillator is in Bypass mode.

59.4.9 Crystal Oscillator Design Considerations

59.4.9.1 Choosing a Crystal

When choosing a crystal for the 32768 Hz Slow Clock Oscillator or for the 3–20 MHz oscillator, several parameters must be taken into account. Important parameters between crystal and product specifications are as follows:

- Crystal Load Capacitance
  - The total capacitance loading the crystal, including the oscillator's internal parasitics and the PCB parasitics, must match the load capacitance for which the crystal's frequency is specified. Any mismatch in the load capacitance with respect to the crystal's specification will lead to inaccurate oscillation frequency
- Drive Level
  - Crystal drive level ≥ Oscillator Drive Level. Having a crystal drive level number lower than the oscillator specification may damage the crystal.
- Equivalent Series Resistor (ESR)
  - Crystal ESR ≤ Oscillator ESR Max. Having a crystal with ESR value higher than the oscillator may cause the oscillator to not start.
- Shunt Capacitance
  - Max. crystal shunt capacitance ≤ Oscillator Shunt Capacitance (C_{SHUNT}). Having a crystal with C_{SHUNT} value higher than the oscillator may cause the oscillator to not start.