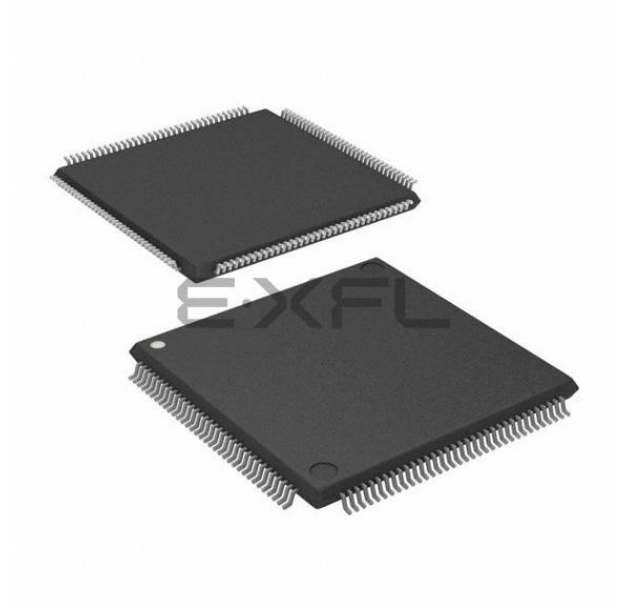

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q20b-an

16.7.4 Embedded Trace Module (ETM) Pins

The Embedded Trace Module (ETM) uses the Trace Port Interface Unit (TPIU) to export data out of the system.

The TPUI features the pins:

- TRACECLK–always exported to enable synchronization back with the data. PCK3 is used internally.
- TRACED0–3–the instruction trace stream.

16.7.5 Flash Patch Breakpoint (FPB)

The FPB implements hardware breakpoints.

16.7.6 Data Watchpoint and Trace (DWT)

The DWT contains four comparators which can be configured to generate:

- PC sampling packets at set intervals
- PC or Data watchpoint packets
- Watchpoint event to halt core

The DWT contains counters for:

- Clock cycle (CYCCNT)
- Folded instructions
- Load Store Unit (LSU) operations
- Sleep cycles
- CPI (all instruction cycles except for the first cycle)
- Interrupt overhead

16.7.7 Instrumentation Trace Macrocell (ITM)

The ITM is an application driven trace source that supports `printf` style debugging to trace Operating System (OS) and application events, and emits diagnostic system information. The ITM emits trace information as packets which can be generated by three different sources with several priority levels:

- Software trace: Software can write directly to ITM stimulus registers. This can be done using the `printf` function. For more information, refer to 16.7.5 Flash Patch Breakpoint (FPB).
- Hardware trace: The ITM emits packets generated by the DWT.
- Timestamping: Timestamps are emitted relative to packets. The ITM contains a 21-bit counter to generate the timestamp.

16.7.7.1 How to Configure the ITM

The following example describes how to output trace data in asynchronous trace mode.

Configure the TPIU for asynchronous trace mode. Refer to 16.7.7.3 How to Configure the TPIU.

1. Enable the write accesses into the ITM registers by writing “0xC5ACCE55” into the Lock Access Register (Address: 0xE0000FB0)
2. Write 0x00010015 into the Trace Control register:
   - Enable ITM.
   - Enable Synchronization packets.
   - Enable SWO behavior.
   - Fix the ATB ID to 1.

Table 18-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIO	I/O Lines Power Supply	Power	–	–
VDDCORE	Core Power Supply	Power	–	–
VDDPLL	PLL Power Supply	Power	–	–
GND	Ground	Ground	–	–
Clocks				
XIN	Main Clock Input	Input	–	–
Test				
TST	Test Mode Select	Input	High	Must be connected to VDDIO
PGMEN0	Test Mode Select	Input	Low	Must be connected to GND
PGMEN1	Test Mode Select	Input	High	Must be connected to VDDIO
PIO				
PGMNCMD	Valid command available	Input	Low	Pulled-up input at reset
PGMRDY	0: Device is busy 1: Device is ready for a new command	Output	High	Pulled-up input at reset
PGMNOE	Output Enable (active high)	Input	Low	Pulled-up input at reset
PGMNVALID	0: DATA[15:0] is in input mode 1: DATA[15:0] is in output mode	Output	Low	Pulled-up input at reset
PGMM[3:0]	Specifies DATA type (see Table 18-2)	Input	–	Pulled-up input at reset
PGMD[15:0]	Bidirectional data bus	Input/Output	–	Pulled-up input at reset

18.3.2 Signal Names

Depending on the MODE settings, DATA is latched in different internal registers.

Table 18-2. Mode Coding

MODE[3:0]	Symbol	Data
0000	CMDE	Command Register
0001	ADDR0	Address Register LSBs
0010	ADDR1	–
0011	ADDR2	–

19.4.4 Bus Matrix Priority Registers B For Slaves

Name: MATRIX_PRBSx
Offset: 0x84 + x*0x08 [x=0..8]
Reset: 0x00000222
Property: Read/Write

This register can only be written if the WPE bit is cleared in the Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							M12PR[1:0]	
Access							R/W	R/W
Reset							0	0

Bit	15	14	13	12	11	10	9	8
			M11PR[1:0]				M10PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			1	0

Bit	7	6	5	4	3	2	1	0
			M9PR[1:0]				M8PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			1	0			1	0

Bits 0:1, 4:5, 8:9, 12:13, 16:17 – MxPR Master 8 Priority
Fixed priority of Master x for accessing the selected slave. The higher the number, the higher the priority.

All the masters programmed with the same MxPR value for the slave make up a priority pool.

Round-robin arbitration is used in the lowest (MxPR = 0) and highest (MxPR = 3) priority pools.

Fixed priority is used in intermediate priority pools (MxPR = 1) and (MxPR = 2).

See “Arbitration Priority Scheme” for details.

31.20.12 PMC USB Clock Register

Name: PMC_USB
Offset: 0x0038
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access					USBDIV[3:0]			
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								USBS
Reset								0

Bits 11:8 – USBDIV[3:0] Divider for USB_48M
USB_48M is input clock divided by USBDIV+1.

Bit 0 – USBS USB Input Clock Selection

Value	Description
0	USB_48M input is PLLA.
1	USB_48M input is UPLL.

32.6.1.26 PIO Input Filter Slow Clock Disable Register

Name: PIO_IFSCDR
Offset: 0x0080
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Peripheral Clock Glitch Filtering Select

Value	Description
0	No effect.
1	The glitch filter is able to filter glitches with a duration < $t_{peripheral\ clock}/2$.

- "SMC Cycle Register"
- "SMC Mode Register"
- "SMC Off-chip Memory Scrambling Register"

35.9.6 Coding Timing Parameters

All timing parameters are defined for one chip select and are grouped together in one register according to their type.

The SMC_SETUP register groups the definition of all setup parameters:

- NRD_SETUP
- NCS_RD_SETUP
- NWE_SETUP
- NCS_WR_SETUP

The SMC_PULSE register groups the definition of all pulse parameters:

- NRD_PULSE
- NCS_RD_PULSE
- NWE_PULSE
- NCS_WR_PULSE

The SMC_CYCLE register groups the definition of all cycle parameters:

- NRD_CYCLE
- NWE_CYCLE

The following table shows how the timing parameters are coded and their permitted range.

Table 35-4. Coding and Range of Timing Parameters

Coded Value	Number of Bits	Effective Value	Permitted Range	
			Coded Value	Effective Value
setup [5:0]	6	128 × setup[5] + setup[4:0]	0 ≤ 31	0 ≤ 128+31
pulse [6:0]	7	256 × pulse[6] + pulse[5:0]	0 ≤ 63	0 ≤ 256+63
cycle [8:0]	9	256 × cycle[8:7] + cycle[6:0]	0 ≤ 127	0 ≤ 256+127 0 ≤ 512+127 0 ≤ 768+127

35.9.7 Reset Values of Timing Parameters

The following table provides the default value of timing parameters at reset.

Table 35-5. Reset Values of Timing Parameters

Parameter	Reset Value	Definition
SMC_SETUP	0x01010101	All setup timings are set to 1.
SMC_PULSE	0x01010101	All pulse timings are set to 1.
SMC_CYCLE	0x00030003	The read and write operations continue for 3 Master Clock cycles and provide one hold cycle.

In any packet buffer mode, writing a '1' to the Flush Next Package bit in the NCR register (GMAC_NCR.FNP) will force a packet from the external SRAM-based receive packet buffer to be flushed. This feature is only acted upon when the RX DMA is not currently writing packet data out to AHB, i.e., it is in an IDLE state. If the RX DMA is active, GMAC_NCR.FNP=1 is ignored.

38.6.3.4 Transmit AHB Buffers

Frames to transmit are stored in one or more transmit AHB buffers. Transmit frames can be between 1 and 16384 Bytes long, so it is possible to transmit frames longer than the maximum length specified in the IEEE 802.3 standard. It should be noted that zero length AHB buffers are allowed and that the maximum number of buffers permitted for each transmit frame is 128.

The start location for each transmit AHB buffer is stored in memory in a list of transmit buffer descriptors at a location pointed to by the transmit buffer queue pointer. The base address for this queue pointer is set in software using the Transmit Buffer Queue Base Address register. Each list entry consists of two words. The first is the Byte address of the transmit buffer and the second containing the transmit control and status. For the packet buffer DMA, the start location for each AHB buffer is a Byte address, the bottom bits of the address being used to offset the start of the data from the data-word boundary (i.e., bits 2,1 and 0 are used to offset the address for 64-bit data paths).

Frames can be transmitted with or without automatic Cyclic Redundancy Checksum (CRC) generation. If CRC is automatically generated, pad will also be automatically generated to take frames to a minimum length of 64 Bytes. When CRC is not automatically generated (as defined in word 1 of the transmit buffer descriptor), the frame is assumed to be at least 64 Bytes long and pad is not generated.

An entry in the transmit buffer descriptor list is described in this table:

Table 38-3. Transmit Buffer Descriptor Entry

Bit	Function
Word 0	
31:0	Byte address of buffer
Word 1	
31	Used—must be zero for the GMAC to read data to the transmit buffer. The GMAC sets this to one for the first buffer of a frame once it has been successfully transmitted. Software must clear this bit before the buffer can be used again.
30	Wrap—marks last descriptor in transmit buffer descriptor list. This can be set for any buffer within the frame.
29	Retry limit exceeded, transmit error detected
28	Reserved.
27	Transmit frame corruption due to AHB error—set if an error occurs while midway through reading transmit frame from the AHB, including HRESP errors and buffers exhausted mid frame (if the buffers run out during transmission of a frame then transmission stops, FCS shall be bad and GTXER asserted). Also set if single frame is too large for configured packet buffer memory size.
26	Late collision, transmit error detected.
25:23	Reserved

38.8.36 GMAC PTP Peer Event Frame Transmitted Seconds High Register

Name: GMAC_PEFTSH
Offset: 0x0F0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RUD[15:0] Register Update
The register is updated with the value that the IEEE 1588 timer seconds register held when the SFD of a PTP transmit peer event crosses the MII interface. An interrupt is issued when the register is updated.

Bit 2 – RXSTPIS Received SETUP Interrupt Set

Bit 1 – RXOUTIS Received OUT Data Interrupt Set

Bit 0 – TXINIS Transmitted IN Data Interrupt Set

39.6.32 Host Global Interrupt Status Register

Name: USBHS_HSTISR
Offset: 0x0404
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
Access								
Reset	0	0	0	0	0	0	0	

Bit	23	22	21	20	19	18	17	16
							PEP_9	PEP_8
Access								
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		HWUPI	HSOFI	RXRSMI	RSMEDI	RSTI	DDISCI	DCONNI
Access								
Reset		0	0	0	0	0	0	0

Bits 25, 26, 27, 28, 29, 30, 31 – DMA_ DMA Channel x Interrupt

Value	Description
0	Cleared when the USBHS_HSTDMASTATUSx interrupt source is cleared.
1	Set when an interrupt is triggered by the DMA channel x. This triggers a USB interrupt if the corresponding bit in USBHS_HSTIMR = 1.

Bits 8, 9, 10, 11, 12, 13, 14, 15, 16, 17 – PEP_ Pipe x Interrupt

Value	Description
0	Cleared when the interrupt source is served.
1	Set when an interrupt is triggered by pipe x (USBHS_HSTPIPISRx). This triggers a USB interrupt if the corresponding bit in USBHS_HSTIMR = 1.

Bit 6 – HWUPI Host Wakeup Interrupt
This bit is set when the host controller is in Suspend mode (SOFE = 0) and an upstream resume from the peripheral is detected.

This bit is set when the host controller is in Suspend mode (SOFE = 0) and a peripheral disconnection is detected.

This interrupt is generated even if the clock is frozen by the USBHS_CTRL.FRZCLK bit.

40.14.6 HSMCI Command Register

Name: HSMCI_CMDR
Offset: 0x14
Property: Write-only

This register is write-protected while CMDRDY is 0 in HSMCI_SR. If an Interrupt command is sent, this register is only writable by an interrupt response (field SPCMD). This means that the current command execution cannot be interrupted or modified.

Bit	31	30	29	28	27	26	25	24
					BOOT_ACK	ATACS	IOSPCMD[1:0]	
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			TRTYP[2:0]			TRDIR	TRCMD[1:0]	
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				MAXLAT	OPDCMD	SPCMD[2:0]		
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RSPTYP[1:0]		CMDNB[5:0]					
Access								
Reset								

Bit 27 – BOOT_ACK Boot Operation Acknowledge
The master can choose to receive the boot acknowledge from the slave when a Boot Request command is issued. When set to one this field indicates that a Boot acknowledge is expected within a programmable amount of time defined with DTOMUL and DTOCYC fields located in the HSMCI_DTOR. If the acknowledge pattern is not received then an acknowledge timeout error is raised. If the acknowledge pattern is corrupted then an acknowledge pattern error is set.

Bit 26 – ATACS ATA with Command Completion Signal
0 (NORMAL): Normal operation mode.

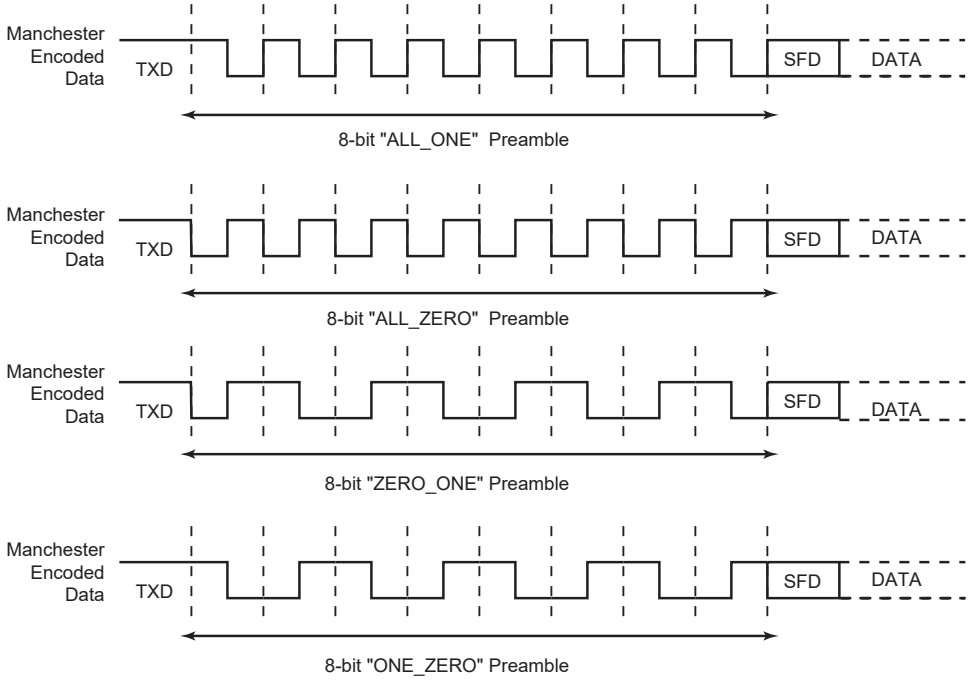
1 (COMPLETION): This bit indicates that a completion signal is expected within a programmed amount of time (HSMCI_CSTOR).

Bits 25:24 – IOSPCMD[1:0] SDIO Special Command

Value	Name	Description
0	STD	Not an SDIO Special Command
1	SUSPEND	SDIO Suspend Command
2	RESUME	SDIO Resume Command

is chosen among the following sequences: ALL_ONE, ALL_ZERO, ONE_ZERO or ZERO_ONE by configuring US_MAN.TX_PP. US_MAN.TX_PL is used to configure the preamble length. Figure 46-8 illustrates and defines the valid patterns. To improve flexibility, the encoding scheme can be configured using US_MAN.TX_MPOL. If TX_MPOL is set to '0' (default), a logic zero is encoded with a zero-to-one transition and a logic one is encoded with a one-to-zero transition. If TX_MPOL is set to '1', a logic one is encoded with a one-to-zero transition and a logic zero is encoded with a zero-to-one transition.

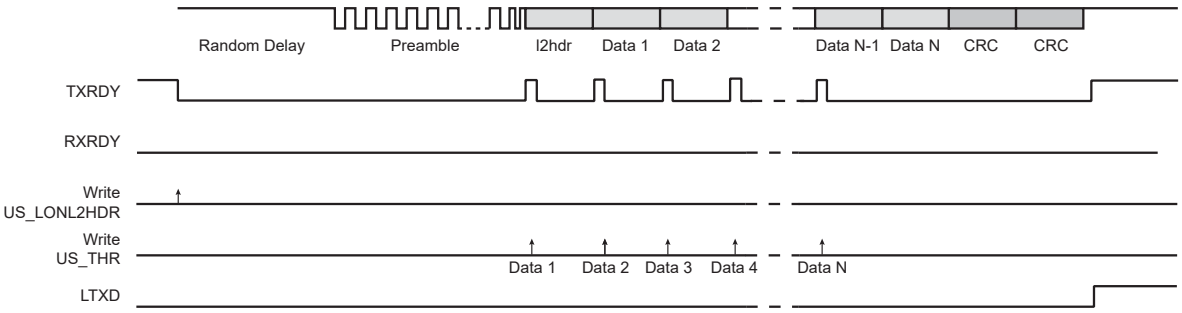
Figure 46-8. Preamble Patterns, Default Polarity Assumed



A start frame delimiter is configured using US_MR.ONEBIT. It consists of a user-defined pattern that indicates the beginning of a valid data. Figure 46-9 illustrates these patterns. If the start frame delimiter, also known as the start bit, is one bit, (ONEBIT = 1), a logic zero is Manchester encoded and indicates that a new character is being sent serially on the line. If the start frame delimiter is a synchronization pattern also referred to as sync (ONEBIT = 0), a sequence of three bit times is sent serially on the line to indicate the start of a new character. The sync waveform is in itself an invalid Manchester waveform as the transition occurs at the middle of the second bit time. Two distinct sync patterns are used: the command sync and the data sync. The command sync has a logic one level for one and a half bit times, then a transition to logic zero for the second one and a half bit times. If US_MR.MODSYNC is written to '1', the next character is a command. If it is written to '0', the next character is a data. When direct memory access is used, MODSYNC can be immediately updated with a modified character located in memory. To enable this mode, US_MR.VAR_SYNC must be written to '1'. In this case, MODSYNC is bypassed and the sync configuration is held in US_THR.TXSYNH. The USART character format is modified and includes sync information.

3. Write CD and FP in US_BRGR to configure the baud rate.
4. Write COMMT, COLDET, TCOL, CDTAIL, RDMNBM and DMAM in US_LONMR to configure the LON operating mode.
5. Write BETA2, BETA1TX, BETA1RX, PCYCLE, PSNB, NPS, IDTTX and ITDRX respectively in US_FIDI, US_LONB1TX, US_LONB1RX, US_TTGR, US_LONPRIO, US_LONIDTTX and US_LONIDTRX to set the LON network configuration.
6. Write TX_PL in US_MAN to select the preamble pattern to use.
7. Write LONPL and LONDL in US_LONPR and US_LONDL to set the frame transfer.
8. Check that TXRDY in US_CSR is set to 1.
9. Write US_LONL2HDR register to send the header.
10. Wait until TXRDY in US_CSR rises.
11. Write TCHR in US_THR to send a byte.
12. If all the data have not been written, redo the two previous steps.
13. Wait until LTXD in US_CSR rises.
14. Check the LON errors.

Figure 46-61. Tx Frame



46.6.10.11.2 Receiving A Frame

1. Write TXEN and RXEN in US_CR to enable both the transmitter and the receiver.
2. Write USART_MODE in US_MR to select the LON mode configuration.
3. Write CD and FP in US_BRGR to configure the baud rate.
4. Write COMMT, COLDET, TCOL, CDTAIL, RDMNBM and DMAM in US_LONMR to configure the LON operating mode.
5. Write BETA2, BETA1TX, BETA1RX, PCYCLE, PSNB, NPS, IDTTX and ITDRX respectively in US_FIDI, US_LONB1TX, US_LONB1RX, US_TTGR, US_LONPRIO, US_LONIDTTX and US_LONIDTRX to set the LON network configuration.
6. Write RXIDLEV and RX_PL in US_MAN to indicate the receiver line value and select the preamble pattern to use.
7. Wait until RXRDY in US_CSR rises.
8. Read RCHR in US_RHR.
9. If all the data and the two CRC bytes have not been read, redo the two previous steps.
10. Wait until LRXD in US_CSR rises.
11. Check the LON errors.
12.

46.7.14 USART Interrupt Mask Register (SPI_MODE)

Name: US_IMR (SPI_MODE)
Offset: 0x0010
Reset: 0x0
Property: Read-only

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset					0			

Bit	15	14	13	12	11	10	9	8
Access								
Reset						0	0	

Bit	7	6	5	4	3	2	1	0
Access								
Reset			0				0	0

Bit 19 – NSSE NSS Line (Driving CTS Pin) Rising or Falling Edge Event Interrupt Mask

Bit 10 – UNRE SPI Underrun Error Interrupt Mask

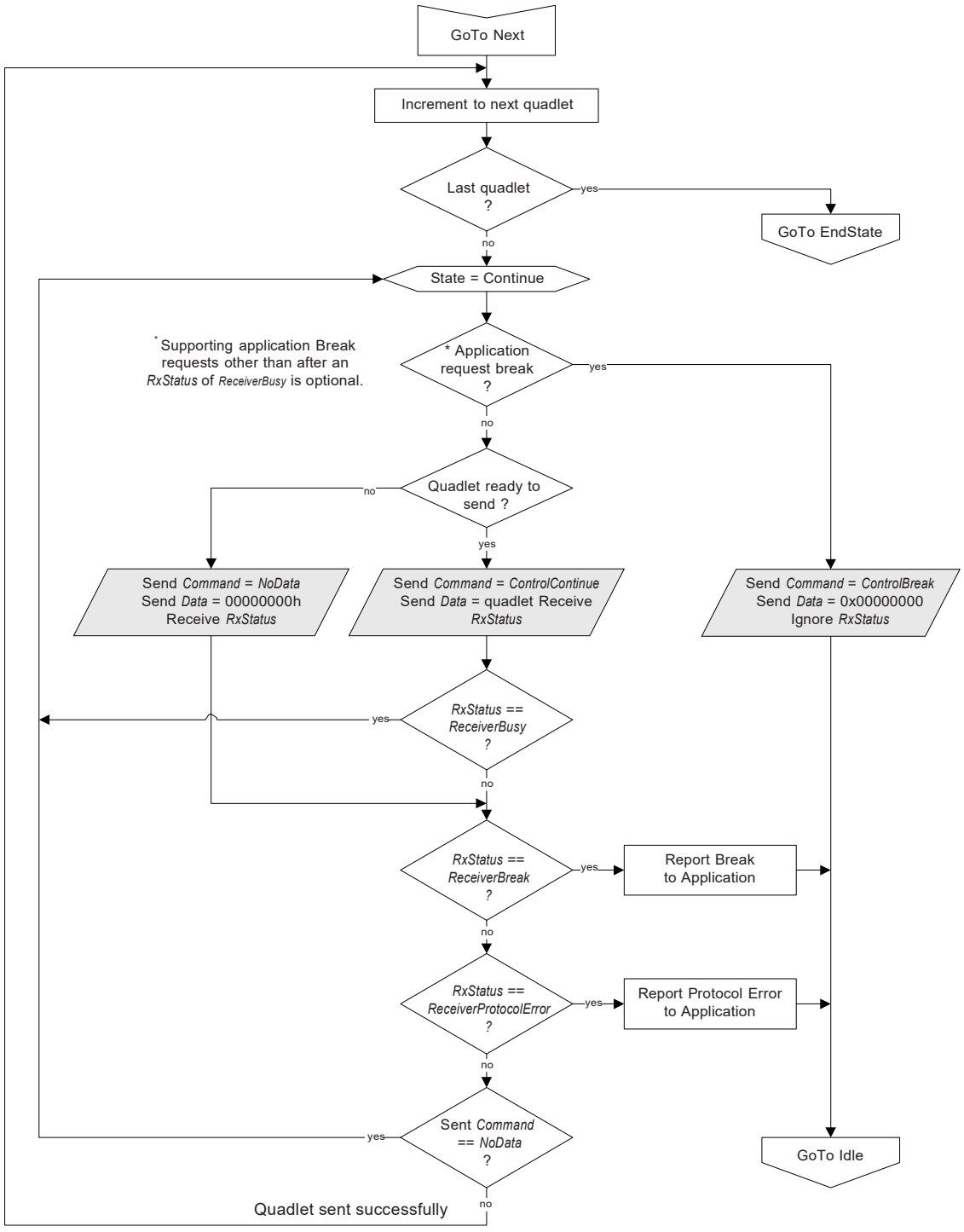
Bit 9 – TXEMPTY TXEMPTY Interrupt Mask

Bit 5 – OVRE Overrun Error Interrupt Mask

Bit 1 – TXRDY TXRDY Interrupt Mask

Bit 0 – RXRDY RXRDY Interrupt Mask

Figure 48-7. Control Packet Tx Device Protocol: Middle



Bit 0 – IDX Index

Value	Description
0	No Index input change since the last read of TC_QISR.
1	The IDX input has changed since the last read of TC_QISR.

51.7.31 PWM Spread Spectrum Update Register

Name: PWM_SSPUP
Offset: 0xA4
Reset: –
Property: Write-only

This register can only be written if bits WPSWS3 and WPHWS3 are cleared in the PWM Write Protection Status Register.

This register acts as a double buffer for the SPRD value. This prevents an unexpected waveform when modifying the spread spectrum limit value.

Only the first 16 bits (channel counter size) are significant.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	SPRDUP[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SPRDUP[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SPRDUP[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bits 23:0 – SPRDUP[23:0] Spread Spectrum Limit Value Update
The spread spectrum limit value defines the range for the spread spectrum counter. It is introduced in order to achieve constant varying period for the output waveform.

Operating Mode	Input Data Registers to Write
OFB	All
128-bit CFB	All
64-bit CFB	AES_IDATAR0 and AES_IDATAR1
32-bit CFB	AES_IDATAR0
16-bit CFB	AES_IDATAR0
8-bit CFB	AES_IDATAR0
CTR	All
GCM	All

Note:

1. In 64-bit CFB mode, writing to AES_IDATAR2 and AES_IDATAR3 is not allowed and may lead to errors in processing.
2. In 32, 16, and 8-bit CFB modes, writing to AES_IDATAR1, AES_IDATAR2 and AES_IDATAR3 is not allowed and may lead to errors in processing.

57.4.6.2 Auto Mode

The Auto Mode is similar to the manual one, except that in this mode, as soon as the correct number of AES_IDATARx is written, processing is automatically started without any action in AES_CR.

57.4.6.3 DMA Mode

The DMA Controller can be used in association with the AES to perform an encryption/decryption of a buffer without any action by software during processing.

AES_MR.SMOD must be configured to 2 and the DMA must be configured with non-incremental addresses.

The start address of any transfer descriptor must be configured with the address of AES_IDATAR0.

The DMA chunk size configuration depends on the AES mode of operation and is listed in the table below.

When writing data to AES with a first DMA channel, data are first fetched from a memory buffer (source data). It is recommended to configure the size of source data to “words” even for CFB modes. On the contrary, the destination data size depends on the mode of operation. When reading data from the AES with the second DMA channel, the source data is the data read from AES and data destination is the memory buffer. In this case, the source data size depends on the AES mode of operation and is listed in the table below.

Table 57-3. DMA Data Transfer Type for the Different Operating Modes

Operating Mode	Chunk Size	Destination/Source Data Transfer Type
ECB	4	Word
CBC	4	Word
OFB	4	Word
CFB 128-bit	4	Word

2. In Sleep mode, the AFE core, the Sample and Hold and the internal reference operational amplifer are off.
3. In Fast Wake-up mode, only the AFE core is off.

58.8.1.2 ADC Bias Current

AFEC_ACR.IBCTL controls the ADC bias current, with the nominal setting IBCTL = 10.

IBCTL = 10 is the mandatory configuration suitable for a sampling frequency of up to 1 MHz. If the sampling frequency is below 500 kHz, IBCTL = 01 can also be used to reduce the current consumption.

If the sampling frequency is more than 1 MHz, then the setting must be IBCTL=11.

Note: The default value in the register is 01 and must be modified according to the defined sampling frequency.

58.8.2 External Reference Voltage

V_{VREFP} is an external reference voltage applied on the pin VREFP. The quality of the reference voltage V_{VREFP} is critical to the performance of the AFE. A DC variation of the reference voltage V_{VREFP} is converted to a gain error by the AFE. The noise generated by V_{VREFP} is converted by the AFE to count noise.

Table 58-30. VREFP Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VREFP}	Voltage Range	Full operational	1.7	–	VDDIN	V
	RMS Noise (see **Note 2**)	Bandwidth up to 1.74MHz VREFP=1.7V	–	–	120	µV
R_{VREFP}	Input DC Impedance	AFE reference resistance bridge (see **Note 1**)	–	4.7	–	kOhm
Vin	Input Linear Range (see **Note 3**)	Operational Range	2	-	98	%VVREFP
I_{VREFP}	Current	V_{VREFP} = 3.3V	–	0.8	–	mA

Note:

1. When the AFE is in Sleep mode, the VREFP impedance has a minimum of 10 MOhm.
2. Requested noise on VREFP.
3. Electrical parameters specified inside the operational range. Exceeding this range can introduce additional INL error up to +/- 5 LSB and temperature dependency up to +/-10 LSB.

58.8.3 AFE Timings

Table 58-31. AFE Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{AFE\ Clock}$	Clock Frequency	–	4	20	40	MHz
$t_{AFE\ Clock}$	Clock Period	–	25	50	250	ns
f_S	Sampling Frequency (see **Note 1**)	–	–	–	1.74	MHz

where:

- Z_{IN} is input impedance in Single-ended or Differential mode
- C_{IN} = 2 to 8 pF ±20% depending on the gain value and mode (SE or DIFF); temperature dependency is negligible
- R_{ON} is typical 2 kΩ and 8 kΩ max (worst case process and high temperature)

The following formula is used to calculate input impedance:

$$Z_{\mathrm{IN}} = \frac{1}{f_S \times C_{\mathrm{IN}}}$$

where:

- f_S is the sampling frequency of the AFE channel
- Typ values are used to compute AFE input impedance Z_{IN}

Table 59-37. Input Capacitance (C_{IN}) Values

Gain Selection	Single-ended	Differential	Unit
1	2	2	pF
2	4	4	
4	8	8	

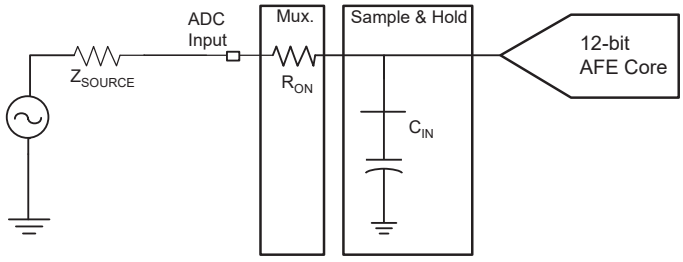
Table 59-38. Z_{IN} Input Impedance

f_S (MHz)	1	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.007813
C_{IN} = 2 pF								
Z_{IN} (MΩ)	0.5	1	2	4	8	16	32	64
C_{IN} = 4 pF								
Z_{IN} (MΩ)	0.25	0.5	1	2	4	8	16	32
C_{IN} = 8 pF								
Z_{IN} (MΩ)	0.125	0.25	0.5	1	2	4	8	16

59.8.6.1 Track and Hold Time versus Source Output Impedance

The figure below shows a simplified acquisition path.

Figure 59-16. Simplified Acquisition Path



During the tracking phase, the AFE tracks the input signal during the tracking time shown below:

$t_{TRACK} = n \times C_{IN} \times (R_{ON}+Z_{SOURCE})/1000$

- Tracking time expressed in ns and Z_{SOURCE} expressed in Ω.