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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q20b-cn

11. Memories

11.1 Embedded Memories

11.1.1 Internal SRAM

SAM E70/S70/V70/V71 devices embed 384 Kbytes or 256 Kbytes of high-speed SRAM.

The SRAM is accessible over the system Cortex-M bus at address 0x2040 0000.

SAM E70/S70/V70/V71 devices embed a Multi-Port SRAM with four ports to optimize the bandwidth and latency. The priorities, defined in the Bus Matrix for each SRAM port slave are propagated, for each request, up to the SRAM slaves.

The Bus Matrix supports four priority levels: Normal, Bandwidth-sensitive, Latency-sensitive and Latency-critical in order to increase the overall processor performance while securing the high-priority latency-critical requests from the peripherals.

The SRAM controller manages interleaved addressing of SRAM blocks to minimize access latencies. It uses Bus Matrix priorities to give the priority to the most urgent request. The less urgent request is performed no later than the next cycle.

Two SRAM slave ports are dedicated to the Cortex-M7 while two ports are shared by the AHB masters.

11.1.2 Tightly Coupled Memory (TCM) Interface

SAM E70/S70/V70/V71 devices embed Tightly Coupled Memory (TCM) running at processor speed.

- ITCM is a single 64-bit interface, based at 0x0000 0000 (code region).
- DTCM is composed of dual 32-bit interfaces interleaved, based at 0x2000 0000 (data region).

ITCM and DTCM are enabled/disabled in the ITCMR and DTCMR registers in ARM SCB.

DTCM is enabled by default at reset. ITCM is disabled by default at reset.

There are four TCM configurations controlled by software. When enabled, ITCM is located at 0x0000 0000, overlapping ROM or Flash depending on the general-purpose NVM bit 1 (GPNVM). The configuration is done with GPNVM bits [8:7].

Table 11-1. TCM Configurations in Kbytes

ITCM	DTCM	SRAM for 384K RAM-based	SRAM for 256K RAM-based	GPNVM Bits [8:7]
0	0	384	256	0
32	32	320	192	1
64	64	256	128	2
128	128	128	0	3

Accesses made to TCM regions when the relevant TCM is disabled and accesses made to the Code and SRAM region above the TCM size limit are performed on the AHB matrix, i.e., on internal Flash or on ROM depending on remap GPNVM bit.

Accesses made to the SRAM above the size limit will not generate aborts.

The Memory Protection Unit (MPU) can to be used to protect these areas.

19.3.3.2.1 Fixed Priority Arbitration

The fixed priority arbitration algorithm is the first and only arbitration algorithm applied between masters from distinct priority pools. It is also used in priority pools other than the highest and lowest priority pools (intermediate priority pools).

Fixed priority arbitration is used by the MATRIX arbiters to dispatch the requests from different masters to the same slave by using the fixed priority defined by the user. If requests from two or more masters are active at the same time, the master with the highest priority number is serviced first. If requests from two or more masters with the same priority are active at the same time, the master with the highest number is serviced first.

For each slave, the priority of each master is defined in the MxPR field in the Priority Registers, MATRIX_PRAS and MATRIX_PRBS.

19.3.3.2.2 Round-Robin Arbitration

Round-robin arbitration is only used in the highest and lowest priority pools. It allows the MATRIX arbiters to properly dispatch requests from different masters to the same slave. If two or more master requests are active at the same time in the priority pool, they are serviced in a round-robin increasing master number order.

19.3.4 System I/O Configuration

The System I/O Configuration register (CCFG_SYSIO) configures I/O lines in System I/O mode (such as JTAG, ERASE, USB, etc.) or as general purpose I/O lines. Enabling or disabling the corresponding I/O lines in peripheral mode or in PIO mode (PIO_PER or PIO_PDR registers) in the PIO controller as no effect. However, the direction (input or output), pull-up, pull-down and other mode control is still managed by the PIO controller.

19.3.5 SMC NAND Flash Chip Select Configuration

The SMC Nand Flash Chip Select Configuration Register (CCFG_SMCNFCS) manages the chip select signal (NCSx) and its assignment to NAND Flash.

Each NCSx may or may not be individually assigned to NAND Flash. When the NCSx is assigned to NAND Flash, the signals NANDOE and NANDWE are used for the NCSx signals selected.

19.3.6 Configuration of Automatic Clock-off Mode

To reduce power consumption, MATRIX, Bridge and EFC automatic clock gating can be enabled by writing a ‘1’ to bits MATCKG, BRIDCKG and EFCCKG, respectively, in the Dynamic Clock Gating register (CCFG_DYNCKG).

19.3.7 Register Write Protection

To prevent any single software error from corrupting MATRIX behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the Write Protection Mode Register (MATRIX_WPMR).

If a write access to a write-protected register is detected, the WPVS flag in the Write Protection Status Register (MATRIX_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS flag is reset by writing the Bus Matrix Write Protect Mode Register (MATRIX_WPMR) with the appropriate access key WPKEY.

The following registers can be write-protected:

- Bus Matrix Master Configuration Registers

Figure 27-2. Time/Calendar Update Timing Diagram

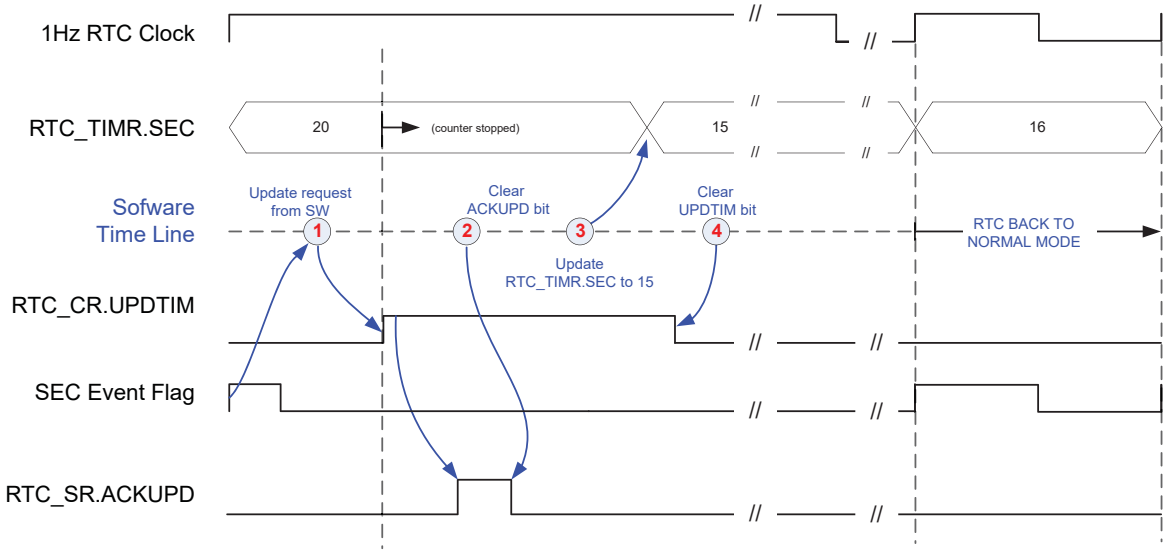


Figure 35-32. Read/Write Cycles in Slow Clock Mode

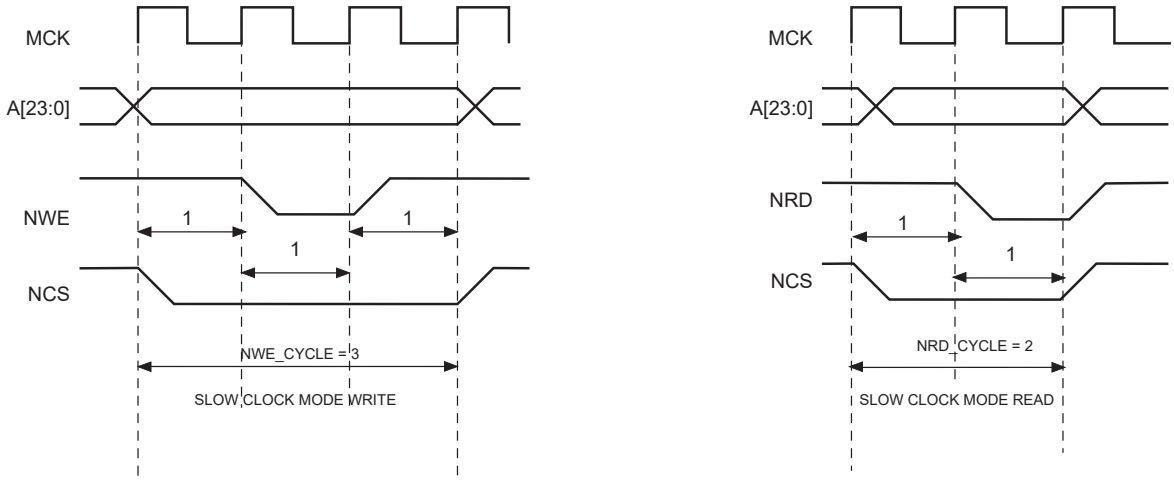


Table 35-6. Read and Write Timing Parameters in Slow Clock Mode

Read Parameters	Duration (cycles)	Write Parameters	Duration (cycles)
NRD_SETUP	1	NWE_SETUP	1
NRD_PULSE	1	NWE_PULSE	1
NCS_RD_SETUP	0	NCS_WR_SETUP	0
NCS_RD_PULSE	2	NCS_WR_PULSE	3
NRD_CYCLE	2	NWE_CYCLE	3

35.14.2 Switching from (to) Slow Clock Mode to (from) Normal Mode

When switching from Slow clock mode to Normal mode, the current Slow clock mode transfer is completed at a high clock rate, with the set of Slow clock mode parameters (see Figure 35-33). The external device may not be fast enough to support such timings.

Figure 35-34 illustrates the recommended procedure to switch from one mode to the other.

39.6.5 Device General Control Register

Name: USBHS_DEVCTRL
Offset: 0x0000
Reset: 0x00000100
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								OPMODE2
Access								
Reset								0

Bit	15	14	13	12	11	10	9	8
	TSTPCKT	TSTK	TSTJ	LS	SPDCONF[1:0]		RMWKUP	DETACH
Access								
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
	ADDEN	UADD[6:0]						
Access								
Reset	0	0	0	0	0	0	0	0

Bit 16 – OPMODE2 Specific Operational mode

Value	Description
0	The UTMI transceiver is in Normal operating mode.
1	The UTMI transceiver is in the “Disable bit stuffing and NRZI encoding” operational mode for test purposes.

Bit 15 – TSTPCKT Test packet mode

Value	Description
0	The UTMI transceiver is in Normal operating mode.
1	The UTMI transceiver generates test packets for test purposes.

Bit 14 – TSTK Test mode K

Value	Description
0	The UTMI transceiver is in Normal operating mode.
1	The UTMI transceiver generates high-speed K state for test purposes.

Bit 13 – TSTJ Test mode J

Bit 10 – AUTOSW Automatic Switch
This bit is cleared upon sending a USB reset.

Value	Description
0	The automatic bank switching is disabled.
1	The automatic bank switching is enabled.

Bits 9:8 – PTOKEN[1:0] Pipe Token
This field contains the pipe token.

Value	Name	Description
0	SETUP	SETUP
1	IN	IN
2	OUT	OUT
3	Reserved	

Bits 6:4 – PSIZE[2:0] Pipe Size
This field contains the size of each pipe bank.

This field is cleared upon sending a USB reset.

Value	Name	Description
0	8_BYTE	8 bytes
1	16_BYTE	16 bytes
2	32_BYTE	32 bytes
3	64_BYTE	64 bytes
4	128_BYTE	128 bytes
5	256_BYTE	256 bytes
6	512_BYTE	512 bytes
7	1024_BYTE	1024 bytes

Bits 3:2 – PBK[1:0] Pipe Banks
This field contains the number of banks for the pipe.

For control pipes, a single-bank pipe (0b00) should be selected.

This field is cleared upon sending a USB reset.

Value	Name	Description
0	1_BANK	Single-bank pipe
1	2_BANK	Double-bank pipe
2	3_BANK	Triple-bank pipe
3	Reserved	

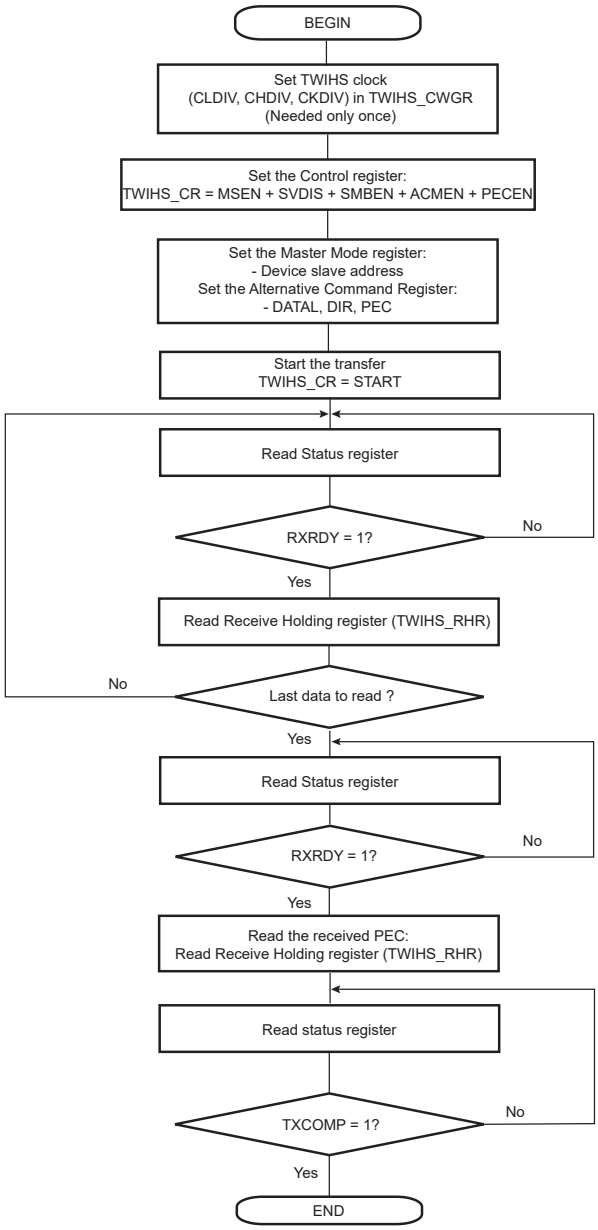
Bit 1 – ALLOC Pipe Memory Allocate
This bit is cleared when a USB Reset is requested.

Refer to ”DPRAM Management” for more details.

Value	Description
0	Frees the pipe memory.
1	Allocates the pipe memory.

Value	Description
0	SPI is in Slave mode
1	SPI is in Master mode

Figure 43-25. TWIHS Read Operation with Multiple Data Bytes with Alternative Command Mode with PEC



US_MR.MAX_ITERATION. As soon as MAX_ITERATION is reached, no error signal is driven on the I/O line and US_CSR.ITER is set.

46.6.4.3 Protocol T = 1

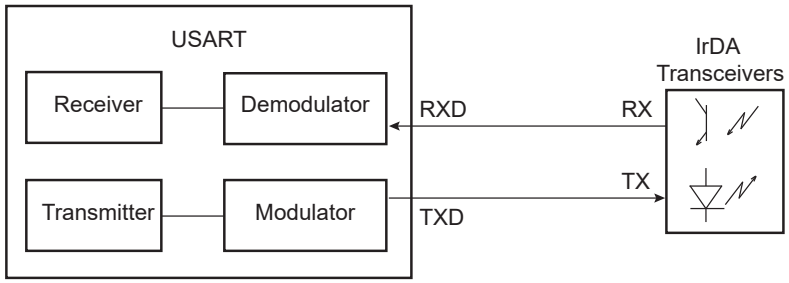
When operating in ISO7816 protocol T = 1, the transmission is similar to an asynchronous format with only one stop bit. The parity is generated when transmitting and checked when receiving. Parity error detection sets US_CSR.PARE.

46.6.5 IrDA Mode

The USART features an IrDA mode supplying half-duplex point-to-point wireless communication. It embeds the modulator and demodulator which allows a glueless connection to the infrared transceivers, as shown in the following figure. The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 kbit/s to 115.2 kbit/s.

The IrDA mode is enabled by writing the value 0x8 to US_MR.USART_MODE. The IrDA Filter register (US_IF) is used to configure the demodulator filter. The USART transmitter and receiver operate in a normal Asynchronous mode and all parameters are accessible. Note that the modulator and the demodulator are activated.

Figure 46-32. Connection to IrDA Transceivers



The receiver and the transmitter must be enabled or disabled depending on the direction of the transmission to be managed.

To receive IrDA signals, the following needs to be done:

- Disable TX and Enable RX
- Configure the TXD pin as PIO and set it as an output to 0 (to avoid LED emission). Disable the internal pull-up (better for power consumption).
- Receive data

46.6.5.1 IrDA Modulation

For baud rates up to and including 115.2 kbit/s, the RZI modulation scheme is used. “0” is represented by a light pulse of 3/16th of a bit time. Some examples of signal pulse duration are shown in the following table.

Table 46-9. IrDA Pulse Duration

Baud Rate	Pulse Duration (3/16)
2.4 kbit/s	78.13 µs
9.6 kbit/s	19.53 µs
19.2 kbit/s	9.77 µs
38.4 kbit/s	4.88 µs

- Not send/check a checksum (CHKDIS = 1)

This configuration is made by the Checksum Type (CHKTYP) and Checksum Disable (CHKDIS) fields of US_LINMR.

If the checksum feature is disabled, the user can send it manually all the same, by considering the checksum as a normal data byte and by adding 1 to the response data length (see Response Data Length).

46.6.9.13 Frame Slot Mode

This mode is useful only for master nodes. It complies with the following rule: each frame slot should be longer than or equal to $t_{Frame\_Maximum}$.

If the Frame Slot mode is enabled (FSDIS = 0) and a frame transfer has been completed, the TXRDY flag is set again only after $t_{Frame\_Maximum}$ delay, from the start of frame. So the master node cannot send a new header if the frame slot duration of the previous frame is inferior to $t_{Frame\_Maximum}$.

If the Frame Slot mode is disabled (FSDIS = 1) and a frame transfer has been completed, the TXRDY flag is set again immediately.

The $t_{Frame\_Maximum}$ is calculated as below:

If the Checksum is sent (CHKDIS = 0):

$t_{Header\_Nominal} = 34 \times t_{bit}$

$t_{Response\_Nominal} = 10 \times (NData + 1) \times t_{bit}$

$t_{Frame\_Maximum} = 1.4 \times (t_{Header\_Nominal} + t_{Response\_Nominal} + 1)$(1)

$t_{Frame\_Maximum} = 1.4 \times (34 + 10 \times (DLC + 1 + 1) + 1) \times t_{bit}$

$t_{Frame\_Maximum} = (77 + 14 \times DLC) \times t_{bit}$

If the Checksum is not sent (CHKDIS = 1):

$t_{Header\_Nominal} = 34 \times t_{bit}$

$t_{Response\_Nominal} = 10 \times NData \times t_{bit}$

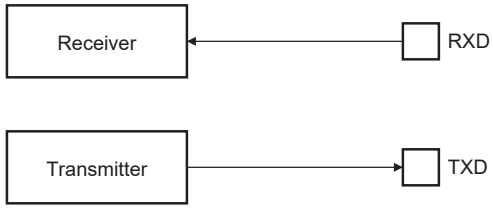
$t_{Frame\_Maximum} = 1.4 \times (t_{Header\_Nominal} + t_{Response\_Nominal} + 1)$(1)

$t_{Frame\_Maximum} = 1.4 \times (34 + 10 \times (DLC + 1) + 1) \times t_{bit}$

$t_{Frame\_Maximum} = (63 + 14 \times DLC) \times t_{bit}$

Note: 1. The term “+1” leads to an integer result for $t_{Frame\_Maximum}$ (LIN Specification 1.3).

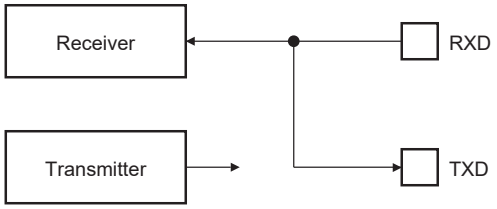
Figure 46-66. Normal Mode Configuration



46.6.11.2 Automatic Echo Mode

Automatic Echo mode allows bit-by-bit retransmission. When a bit is received on the RXD pin, it is sent to the TXD pin, as shown in the following figure. Programming the transmitter has no effect on the TXD pin. The RXD pin is still connected to the receiver input, thus the receiver remains active.

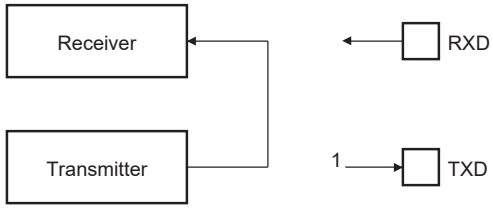
Figure 46-67. Automatic Echo Mode Configuration



46.6.11.3 Local Loopback Mode

Local Loopback mode connects the output of the transmitter directly to the input of the receiver, as shown in the following figure. The TXD and RXD pins are not used. The RXD pin has no effect on the receiver and the TXD pin is continuously driven high, as in idle state.

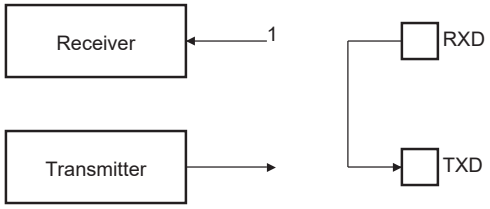
Figure 46-68. Local Loopback Mode Configuration



46.6.11.4 Remote Loopback Mode

Remote Loopback mode directly connects the RXD pin to the TXD pin, as shown in the following figure. The transmitter and the receiver are disabled and have no effect. This mode allows bit-by-bit retransmission.

Figure 46-69. Remote Loopback Mode Configuration

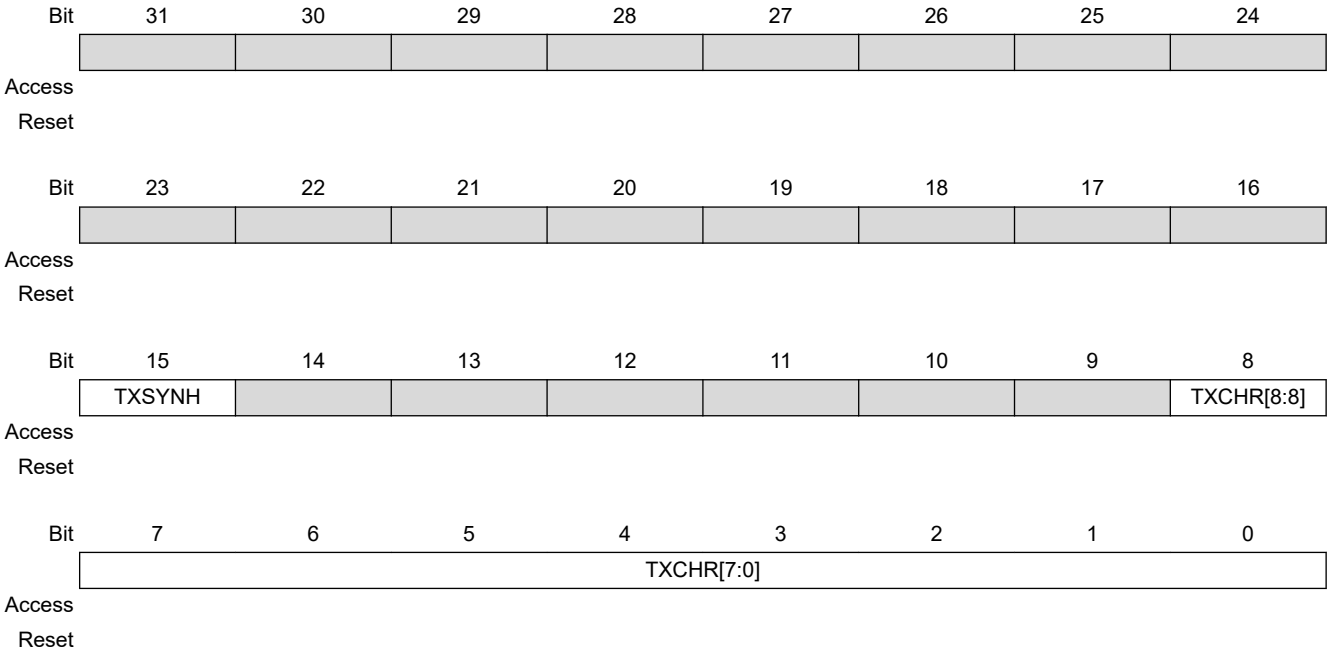


46.6.12 Register Write Protection

To prevent any single software error from corrupting USART behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the USART Write Protection Mode Register (US_WPMR).

46.7.22 USART Transmit Holding Register

Name: US_THR
Offset: 0x001C
Property: Write-only



Bit 15 – TXSYNH Sync Field to be Transmitted

Value	Description
0	The next character sent is encoded as a data. Start frame delimiter is DATA SYNC.
1	The next character sent is encoded as a command. Start frame delimiter is COMMAND SYNC.

Bits 8:0 – TXCHR[8:0] Character to be Transmitted
Next character to be transmitted after the current character if TXRDY is not set.

46.7.46 USART Write Protection Mode Register

Name: US_WPMR
Offset: 0x00E4
Reset: 0x0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x555341	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See Section 7.12 “Register Write Protection” for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x555341 (“USA” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x555341 (“USA” in ASCII).

49.6.2 MCAN Endian Register

Name: MCAN_ENDN
Offset: 0x04
Reset: 0x87654321
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	ETV[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	0	1	1	1

Bit	23	22	21	20	19	18	17	16
	ETV[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	1	1	0	0	1	0	1

Bit	15	14	13	12	11	10	9	8
	ETV[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	1	0	0	0	0	1	1

Bit	7	6	5	4	3	2	1	0
	ETV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	0	1

Bits 31:0 – ETV[31:0] Endianness Test Value
The endianness test value is 0x87654321.

Figure 50-14. WAVSEL = 11 without Trigger

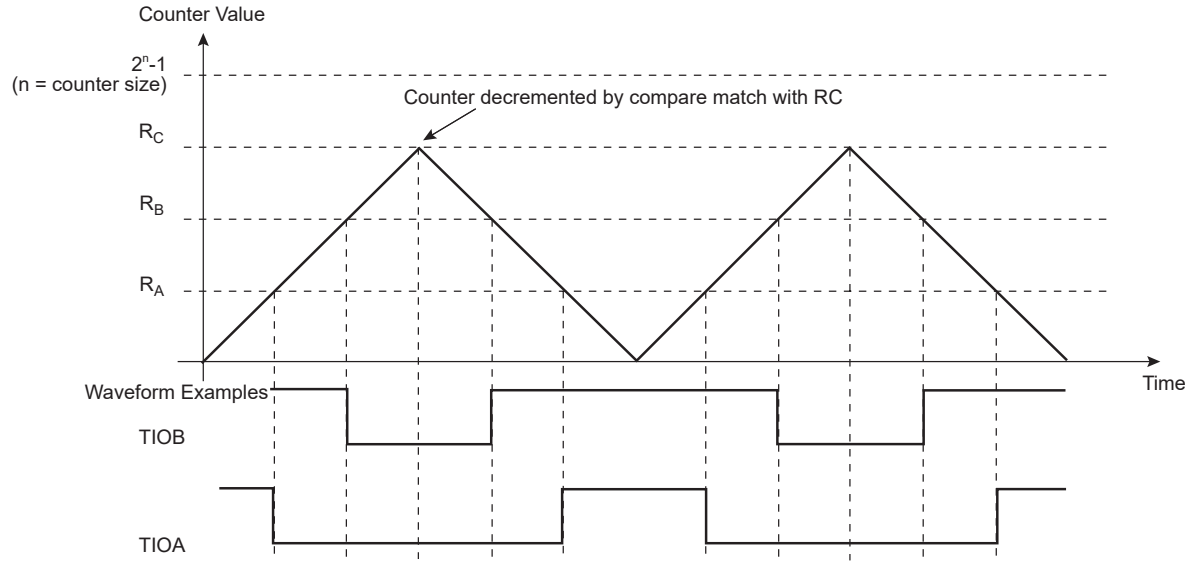
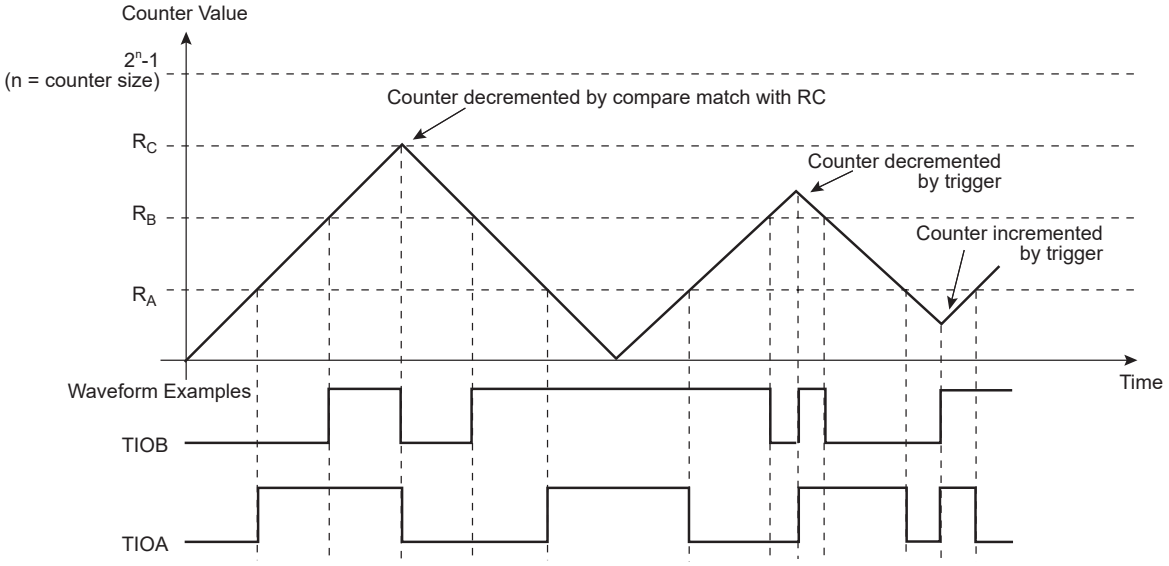


Figure 50-15. WAVSEL = 11 with Trigger



50.6.13 External Event/Trigger Conditions

An external event can be programmed to be detected on one of the clock sources (XC0, XC1, XC2) or TIOBx. The external event selected can then be used as a trigger.

The event trigger is selected using TC_CMR.EEVT. The trigger edge (rising, falling or both) for each of the possible external triggers is defined in TC_CMR.EEVTEDG. If EEVTEDG is cleared (none), no external event is defined.

If TIOBx is defined as an external event signal (EEVT = 0), TIOBx is no longer used as an output and the compare register B is not used to generate waveforms and subsequently no IRQs. In this case, the TC channel can only generate a waveform on TIOAx.

When an external event is defined, it can be used as a trigger by setting TC_CMR.ENETRG.

50.7.15 TC Block Control Register

Name: TC_BCR
Offset: 0xC0
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								SYNC
Access								W
Reset								–

Bit 0 – SYNC Synchro Command

Value	Description
0	No effect.
1	Asserts the SYNC signal which generates a software trigger simultaneously for each of the channels.

50.7.16 TC Block Mode Register

Name: TC_BMR
Offset: 0xC4
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
			MAXCMP[3:0]				MAXFILT[5:4]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MAXFILT[3:0]					AUTOC	IDXPHB	SWAP
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
	INVIDX	INVB	INVA	EDGPHA	QDTRANS	SPEEDEN	POSEN	QDEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TC2XC2S[1:0]		TC1XC1S[1:0]		TC0XC0S[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 29:26 – MAXCMP[3:0] Maximum Consecutive Missing Pulses

Value	Description
0	The flag MPE in TC_QISR never rises.
1–15	Defines the number of consecutive missing pulses before a flag report.

Bits 25:20 – MAXFILT[5:0] Maximum Filter
Pulses with a period shorter than MAXFILT+1 peripheral clock cycles are discarded. For more details on MAXFILT constraints, see "Input Preprocessing"

Value	Description
1–63	Defines the filtering capabilities.

Bit 18 – AUTOC AutoCorrection of missing pulses
0 (DISABLED): The detection and autocorrection function is disabled.

1 (ENABLED): The detection and autocorrection function is enabled.

Bit 17 – IDXPHB Index Pin is PHB Pin

51.6.2.7.1 Recoverable Fault

The PWM provides a Recoverable Fault mode on fault 1 and 2 (see figure *Fault Protection*).

The recoverable fault signal is an internal signal generated as soon as an external trigger event occurs (see PWM External Trigger Mode).

When the fault 1 or 2 is defined as a recoverable fault, the corresponding fault input pin is ignored and bits FFIL1/2, FMOD1/2 and FFIL1/2 are not taken into account.

The fault 1 is managed as a recoverable fault by the PWMEXTRG1 input trigger when PWM_ETRG1.RFEN = 1, PWM_ENA.CHID1 = 1, and PWM_ETRG1.TRGMODE ≠ 0.

The fault 2 is managed as a recoverable fault by the PWMEXTRG2 input trigger when PWM_ETRG2.RFEN = 1, PWM_ENA.CHID2 = 1, and PWM_ETRG2.TRGMODE ≠ 0.

Recoverable fault 1 and 2 can be taken into account by all channels by enabling the bit FPEx[1/2] in the PWM Fault Protection Enable registers (PWM_FPEx). However the synchronous channels (see Synchronous Channels) do not use their own fault enable bits, but those of the channel 0 (bits FPE0[1/2]).

When a recoverable fault is triggered (according to the PWM_ETRGx.TRGMODE setting), the PWM counter of the affected channels is not cleared (unlike in the classic fault protection mechanism) but the channel outputs are forced to the values defined by the fields FPVHx and FPVLx in the PWM Fault Protection Value Register 1 (PWM_FPV), as per table *Forcing Values of PWM Outputs by Fault Protection*. The output forcing is made asynchronously to the channel counter and lasts from the recoverable fault occurrence to the end of the next PWM cycle (if the recoverable fault is no longer present) (see the figure below).

The recoverable fault does not trigger an interrupt. The Fault Status FSy (with y = 1 or 2) is not reported in the PWM Fault Status Register when the fault y is a recoverable fault.

51.7.34 PWM Write Protection Control Register

Name: PWM_WPCR
Offset: 0xE4
Reset: –
Property: Write-only

See Register Write Protection for the list of registers that can be write-protected.

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	7	6	5	4	3	2	1	0
	WPRG5	WPRG4	WPRG3	WPRG2	WPRG1	WPRG0	WPCMD[1:0]	
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	–	0	–

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x50574D	PASSWD	Writing any other value in this field aborts the write operation of the WPCMD field. Always reads as 0

Bits 2, 3, 4, 5, 6, 7 – WPRGx Write Protection Register Group x

Value	Description
0	The WPCMD command has no effect on the register group x.
1	The WPCMD command is applied to the register group x.

Bits 1:0 – WPCMD[1:0] Write Protection Command
This command is performed only if the WPKEY corresponds to 0x50574D (“PWM” in ASCII).

58.4.5 XIN32 Clock Characteristics in Bypass Mode

Table 58-22. XIN32 Clock Characteristics in Bypass Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN32 Clock Frequency	(see **Note**)	–	–	32	kHz
t_{CHXIN}	XIN32 Clock High Half-period	(see **Note**)	15	–	–	ns
t_{CLXIN}	XIN32 Clock Low Half-period	(see **Note**)	15	–	–	ns
V_{XIN_IL}	V_{XIN} Input Low-level Voltage	(see **Note**)	Min of V_{IL} for CLOCK pad	–	Max of V_{IL} for CLOCK pad	V
V_{XIN_IH}	V_{XIN} Input High-level Voltage	(see **Note**)	Min of V_{IH} for CLOCK pad	–	Max of V_{IH} for CLOCK pad	V

Note:

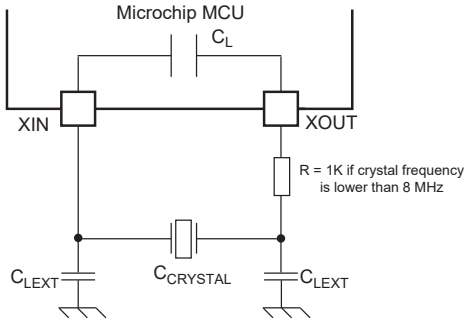
1. These characteristics apply only when the 32.768 kHz crystal oscillator is in Bypass mode.

58.4.6 3 to 20 MHz Crystal Oscillator Characteristics

Table 58-23. 3 to 20 MHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	Normal mode with crystal	3	–	20	MHz
t_{START}	Startup Time	3 MHz, C_{SHUNT} = 3 pF	–	–	40	ms
		12 MHz, C_{SHUNT} = 7 pF with C_M = 1.6 fF	–	–	6	ms
		20 MHz, C_{SHUNT} = 7 pF with C_M = 1.6 fF	–	–	5.7	ms
I_{DDON}	Current Consumption (on VDDIO)	3 MHz	–	230	–	µA
		12 MHz	–	390	–	µA
		20 MHz	–	450	–	µA
C_L	Internal Equivalent Load Capacitance	Integrated Load Capacitance	7.5	9	10.5	pF
		(X_{IN} and X_{OUT} in series)				

Figure 58-10. 3 to 20 MHz Crystal Oscillator Schematics



$C_{LEXT} = 2 \times (C_{CRYSTAL} - C_L - C_{PCB})$